

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.


J95 MLB SKL EMERALD

LAST MODIFICATION=Thu Feb 12 14:48:08 2015

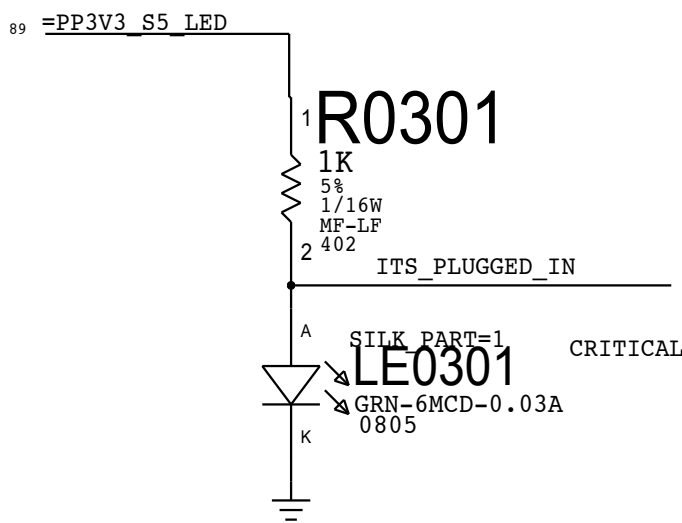
REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
			2015-02-12

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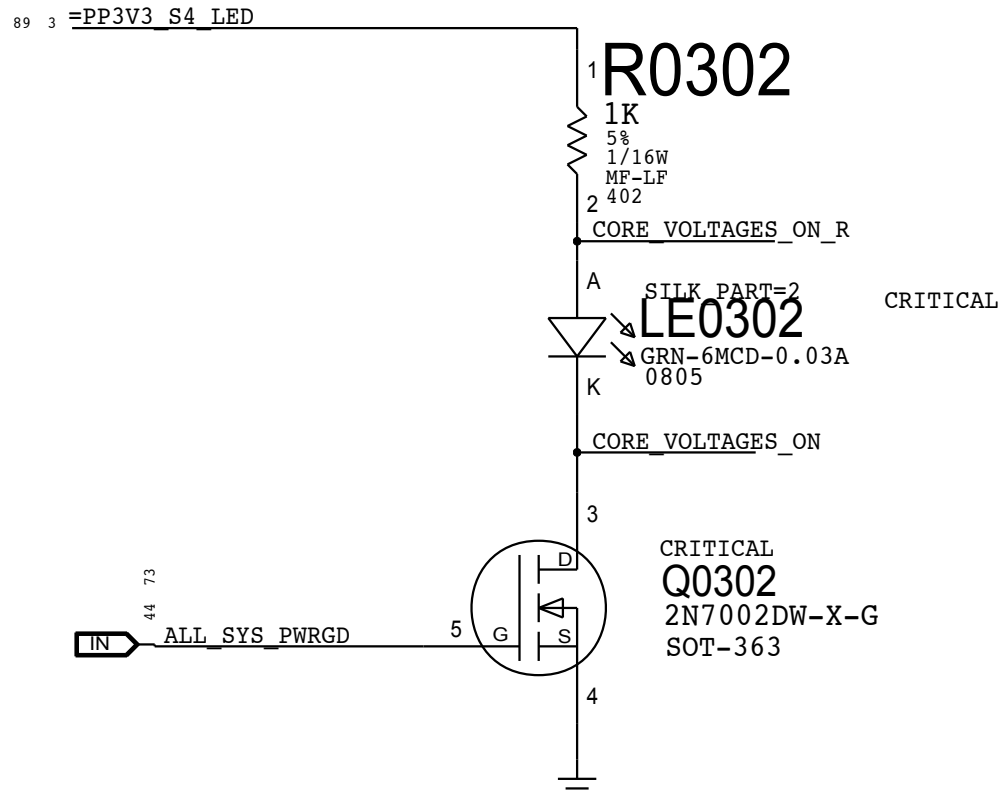
[illegible]

SCHEM, J95, m1b_skl_EM			
DRAWING TITLE			
SCHEM, MLB, SKYLAKE, EMERALD, J95			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-00673		D
	REVISION		
	0.24.0		
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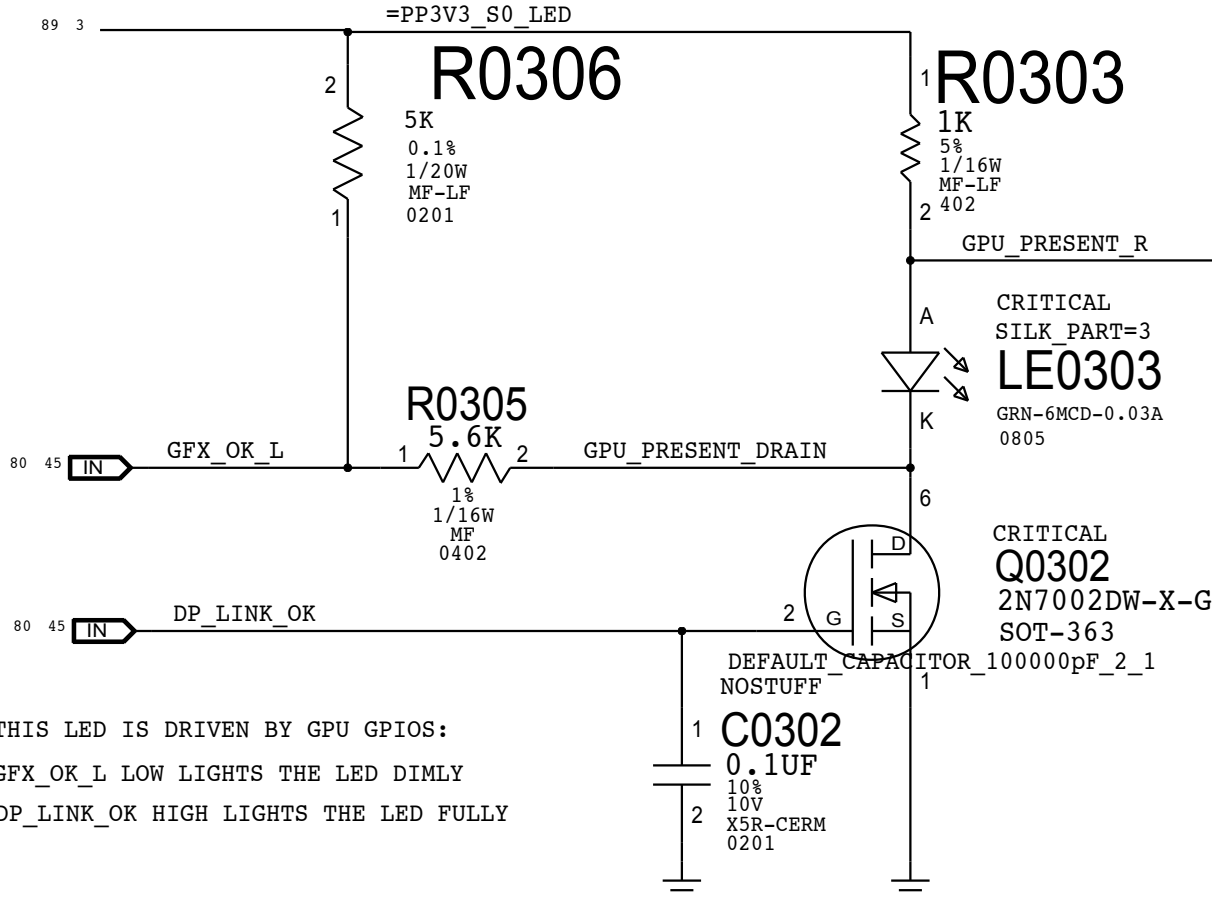
S5 Led



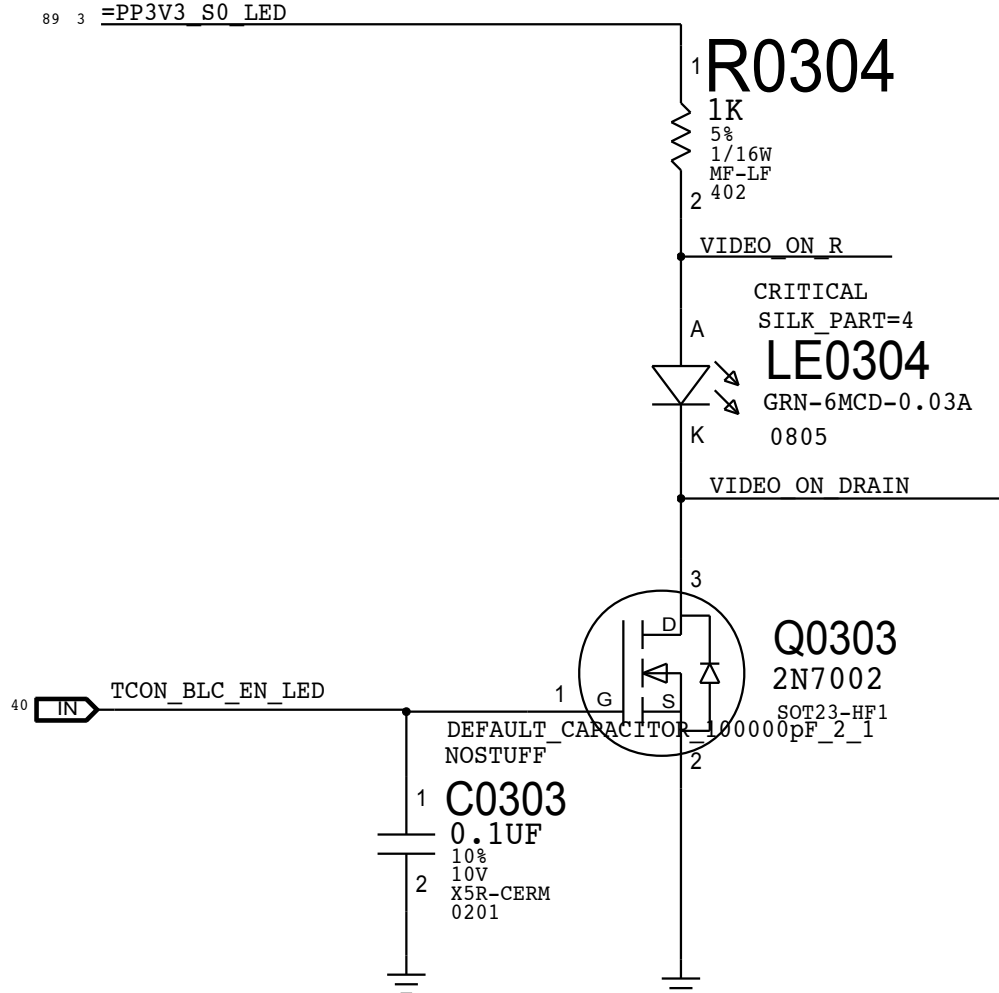
ALL_SYS_PWRGD Led



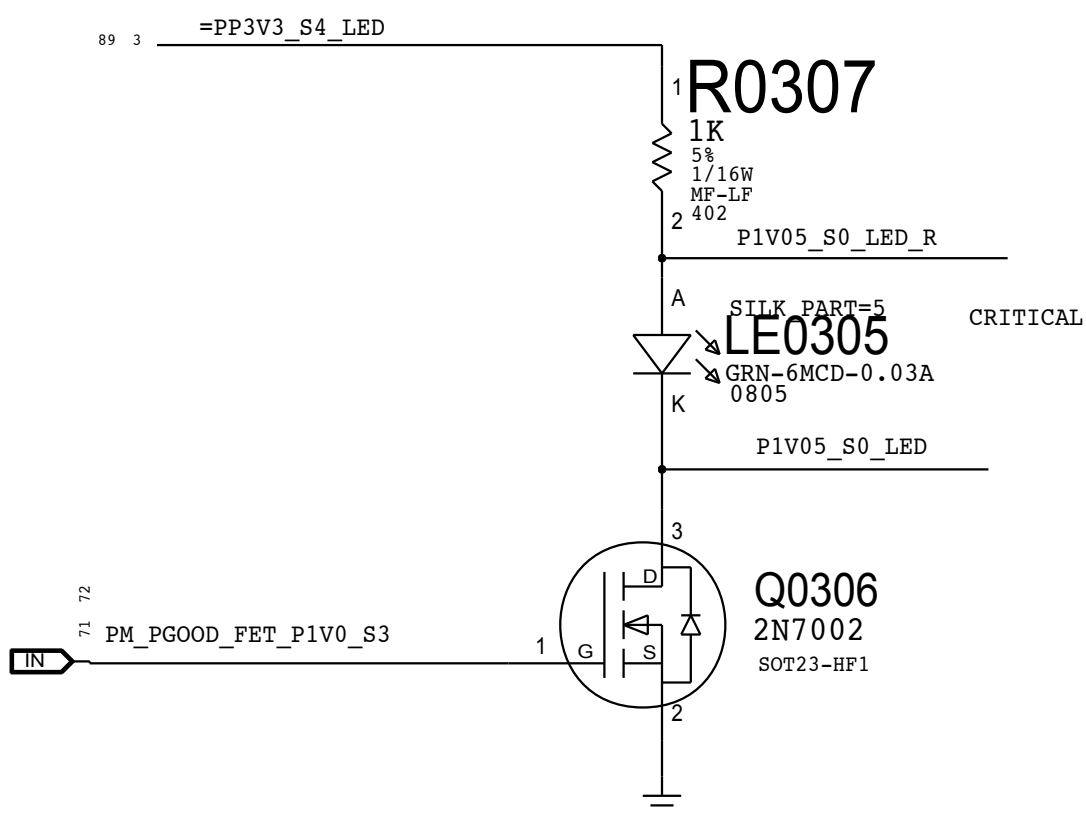
GPU GOOD Led



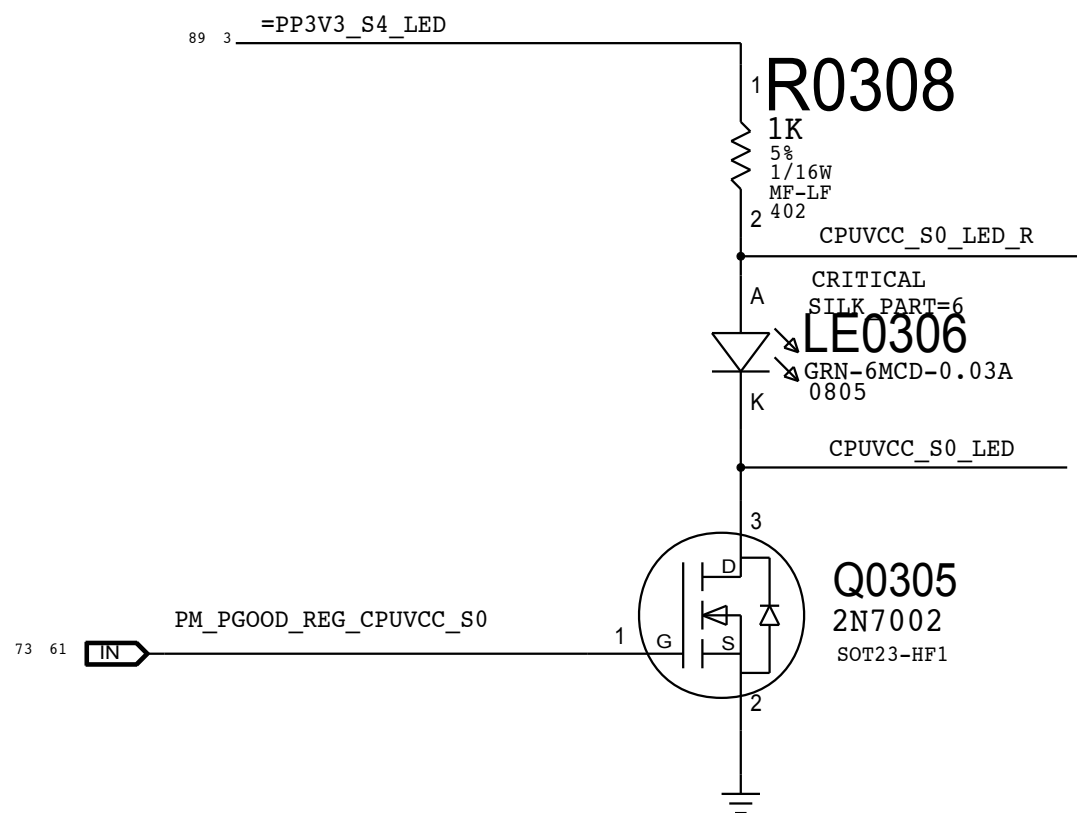
VIDEO ON Led



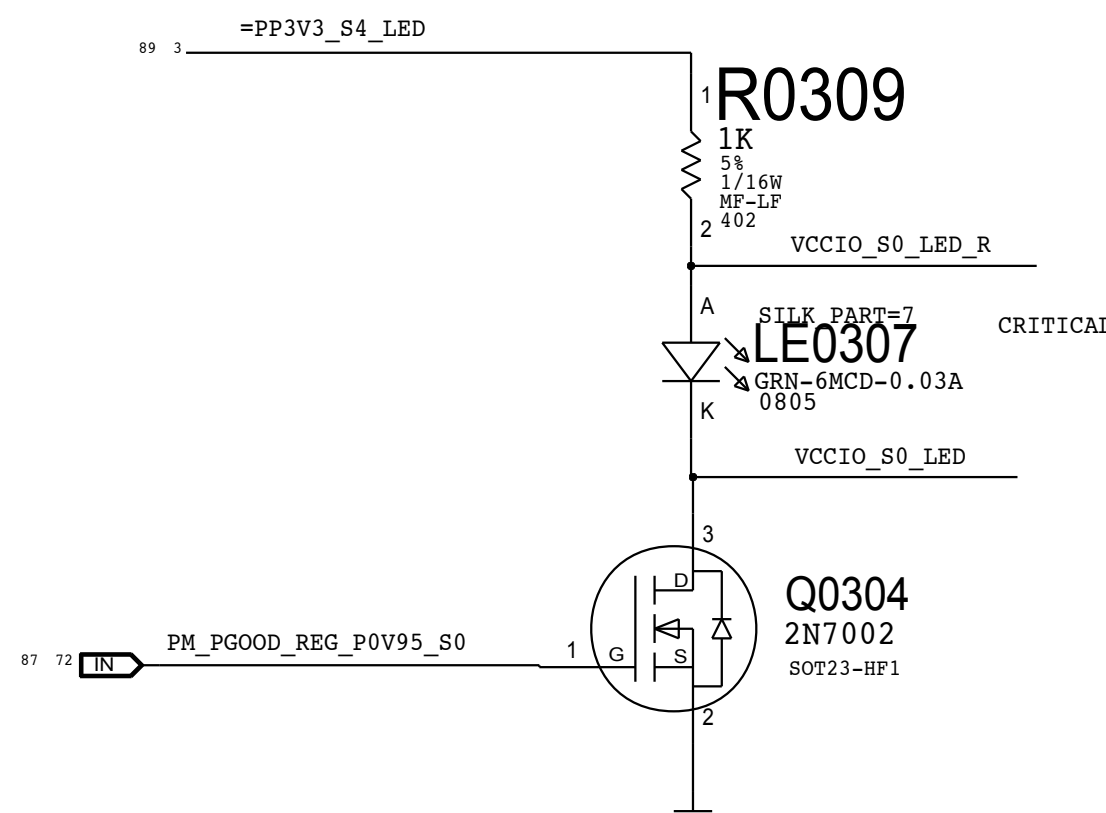
P1V0_S3_PWRGD Led

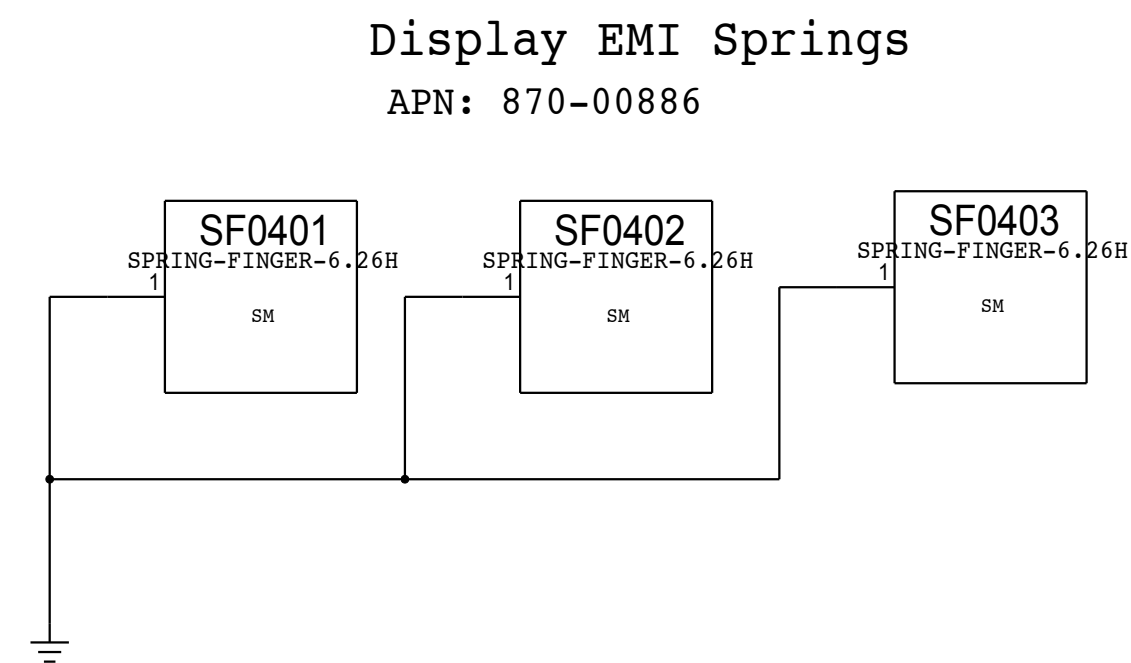
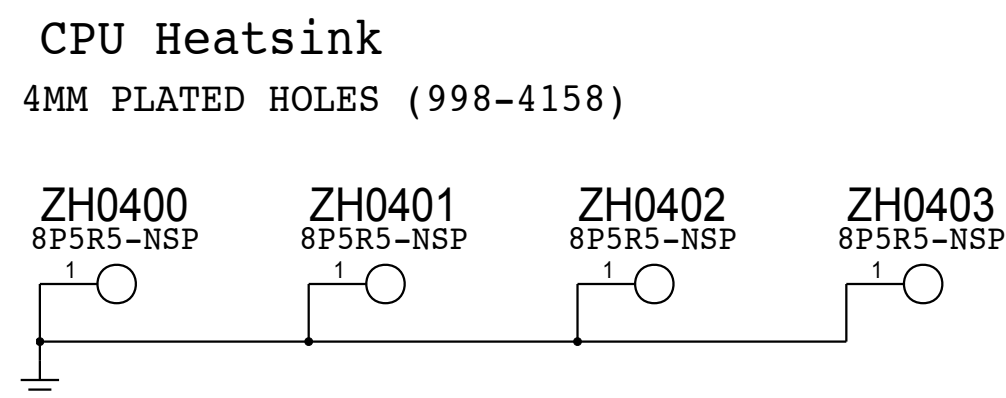


CPUVCC_S0_PWRGD Led



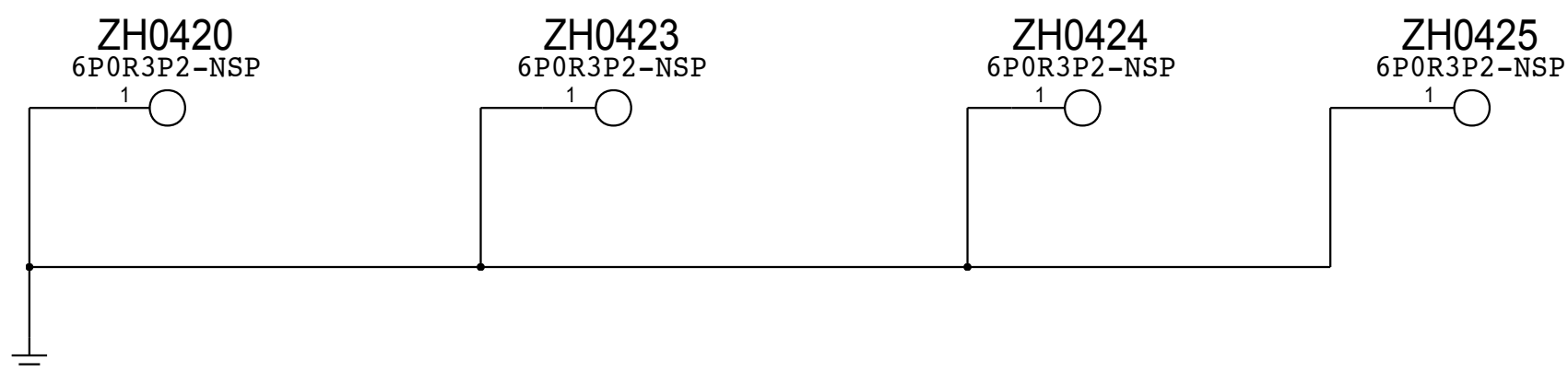
VCCIO_S0_PWRGD Led





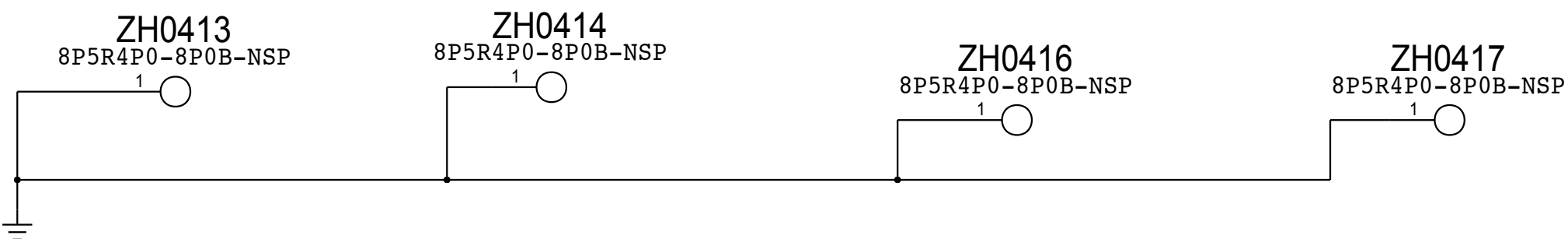
GPU HEATSINK MOUNTING FEATURES

(998-5013. PLATED HOLE, 3.2MM DIA, 6MM PAD TOP/BOT)



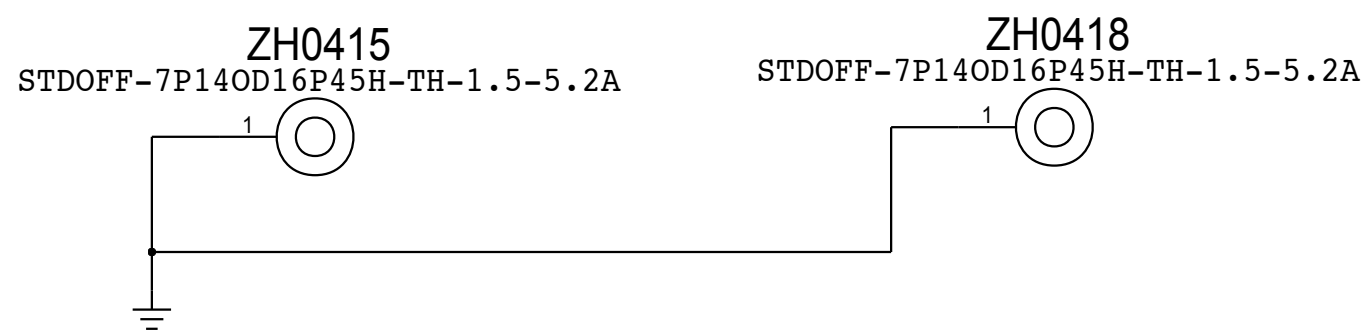
Rear Cover

998-5014 (PLATED HOLES, 4MM DRILL, 8.5MM TOP, 8MM BOT)



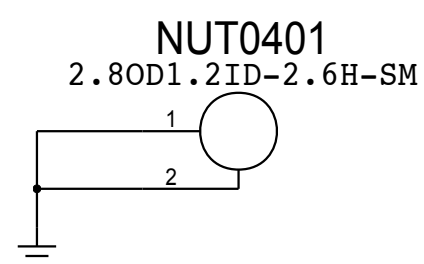
Rear Cover

860-5674 (PCB STANDOFF)



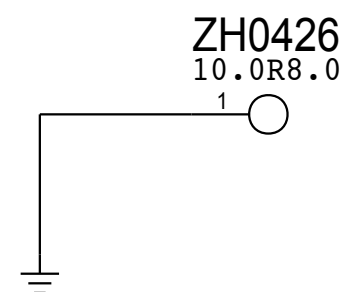
T29 BUMPER

APN: 860-00201



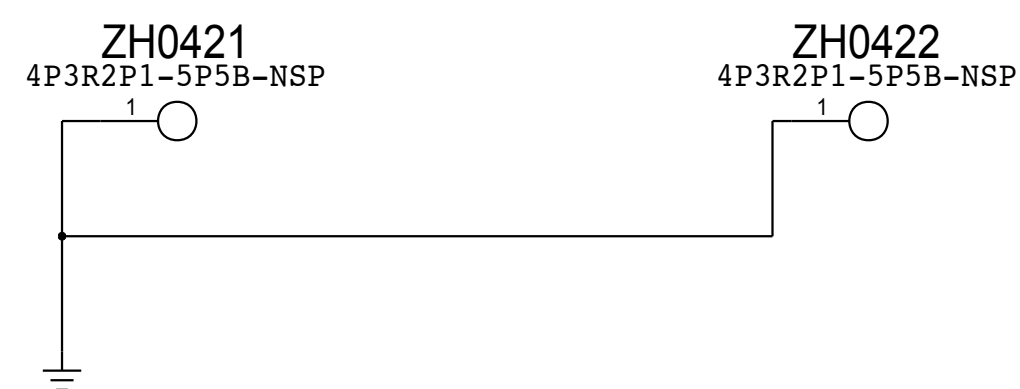
HEATPIPE MTG HOLES

998-5527 (PLATED HOLES, 8MM DIA, 10MM PAD)



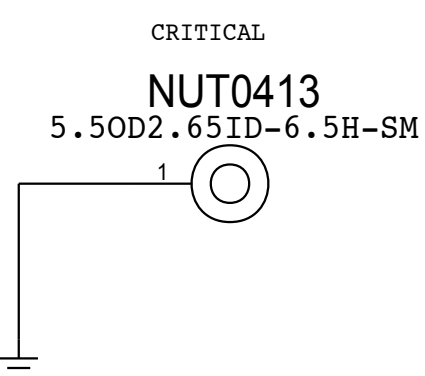
X238D WIRELESS CARD MTG HOLES

998-01489 (PLATED HOLES, 2.1MM INNER DIAMETER, 5.5MM PAD)



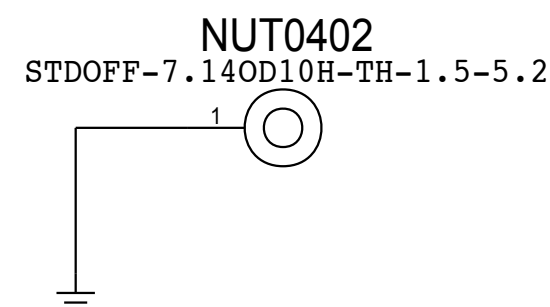
SSD STANDOFF

APN: 860-00198




LOL BOSS

860-5675 (PLATED HOLE, 8.41mm pad Top, 8mm pad Bot)



EMERALD EMI FENCE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
860-02579	1	FENCE, GPU, EMERALD, 90, J95	SF0404	CRITICAL	GPU_Emerald

SYNC MASTER=J17 MAX PAGE TITLE		SYNC DATE=02/11/2013	
MECHANICAL: Holes/PD parts			
 Apple Inc.		DRAWING NUMBER 051-00673	SIZE D
		REVISION 0.24.0	
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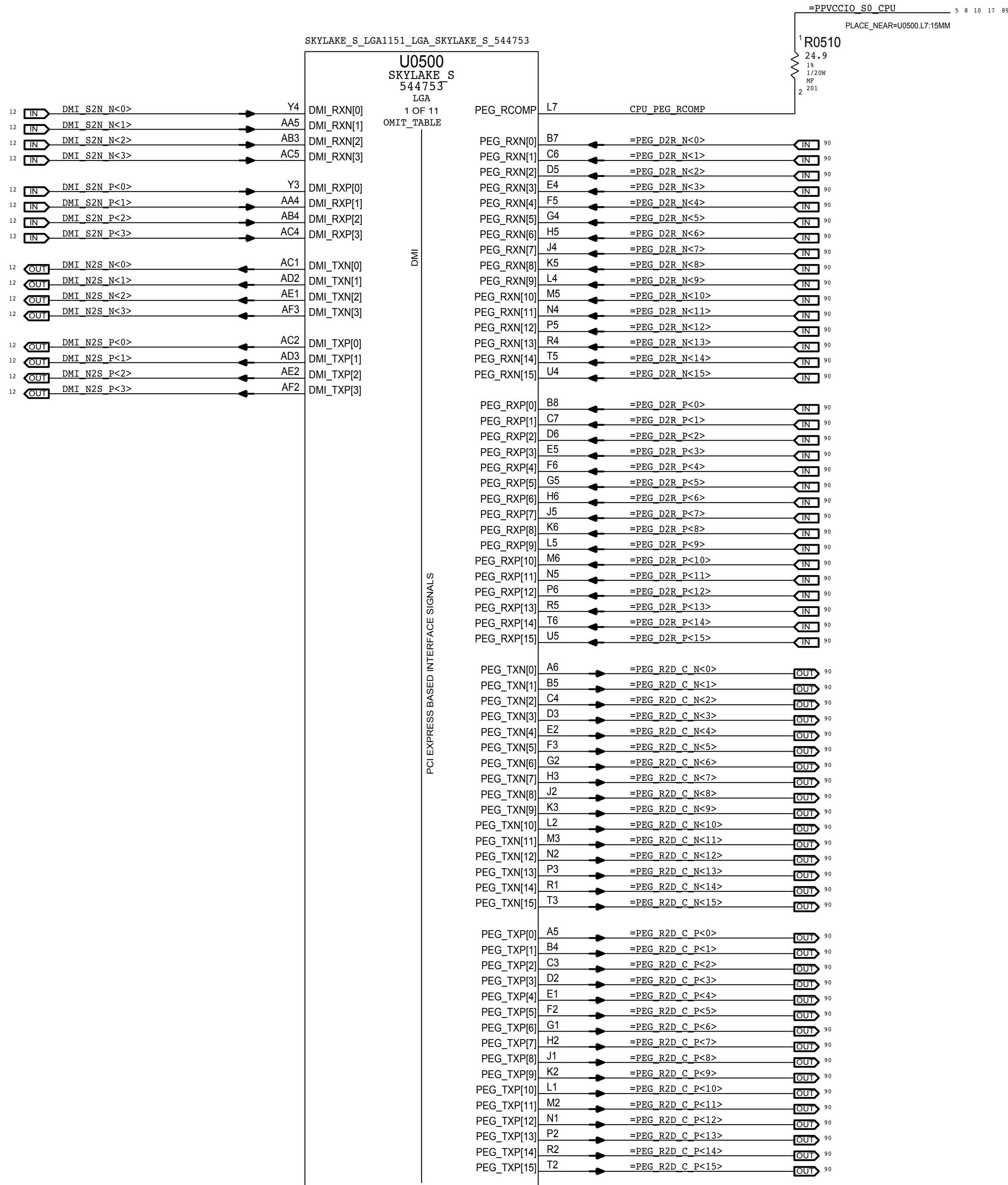
A

D

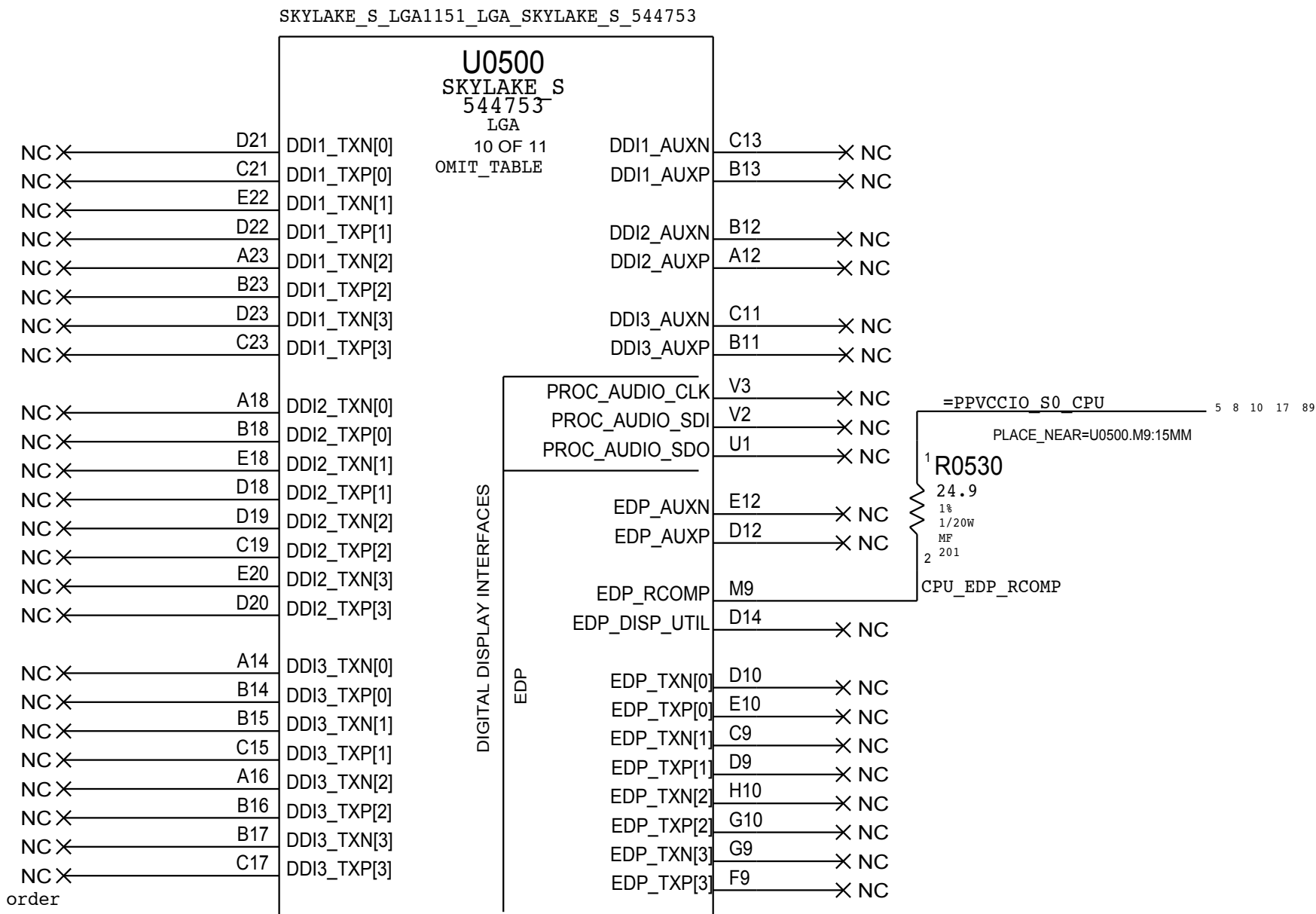
C


B

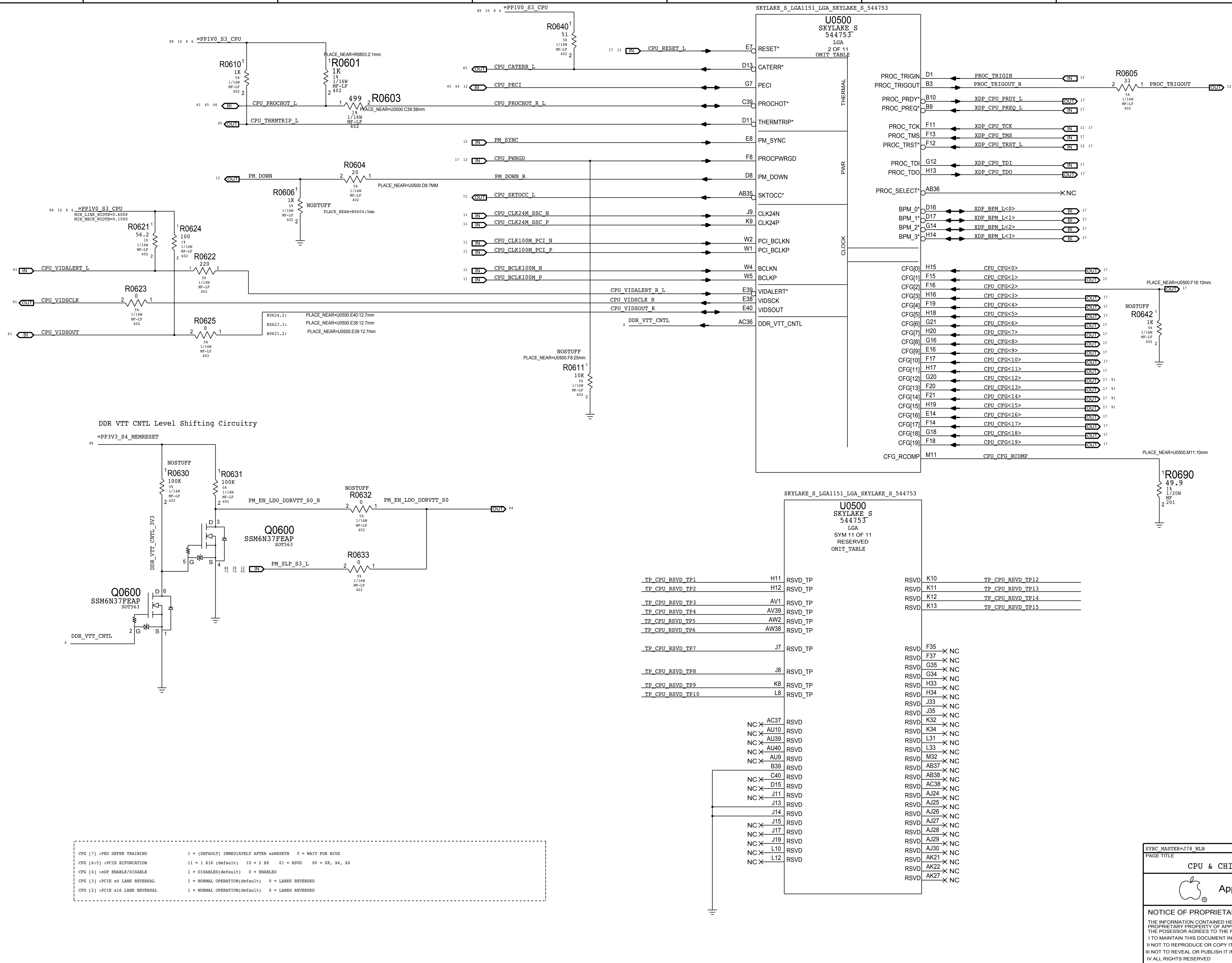
A



Port D pins out of order
to match Intel symbol.




SYNC_MASTER=J78_MLB		SYNC_DATE=06/30/2014	
PAGE TITLE			
CPU & CHIPSET: CPU DMI/PEG/FDI/RSVD			
	Apple Inc.	DRAWING NUMBER	SIZE
		051-00673	D
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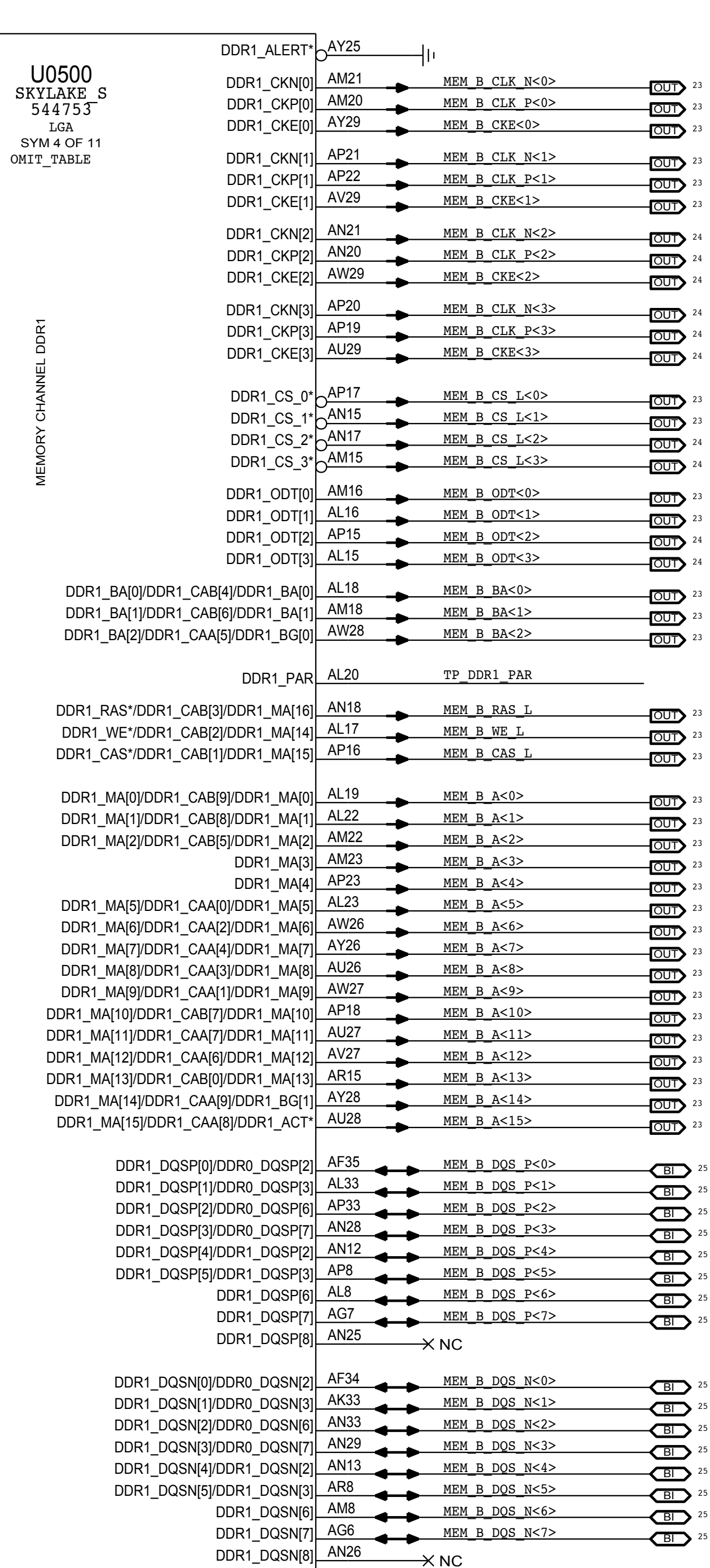
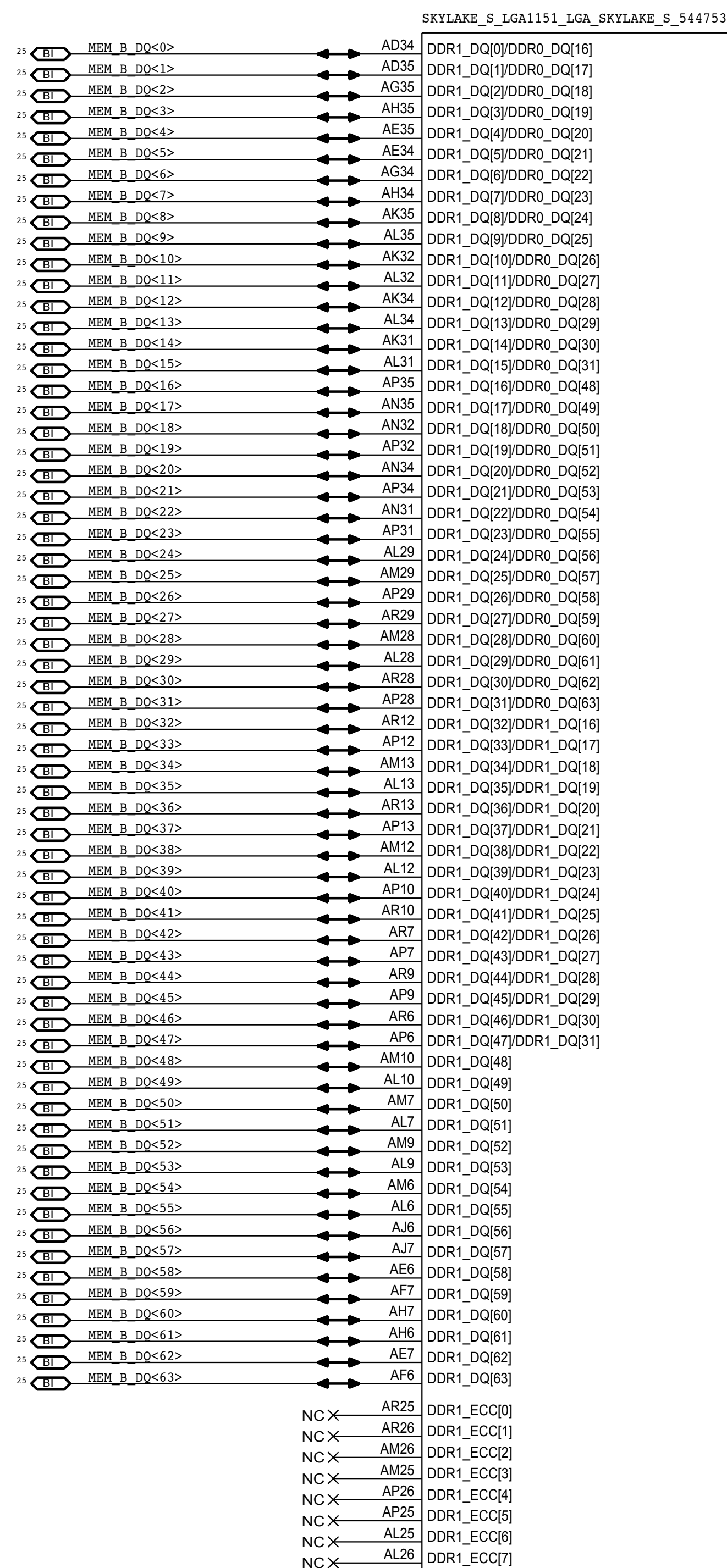
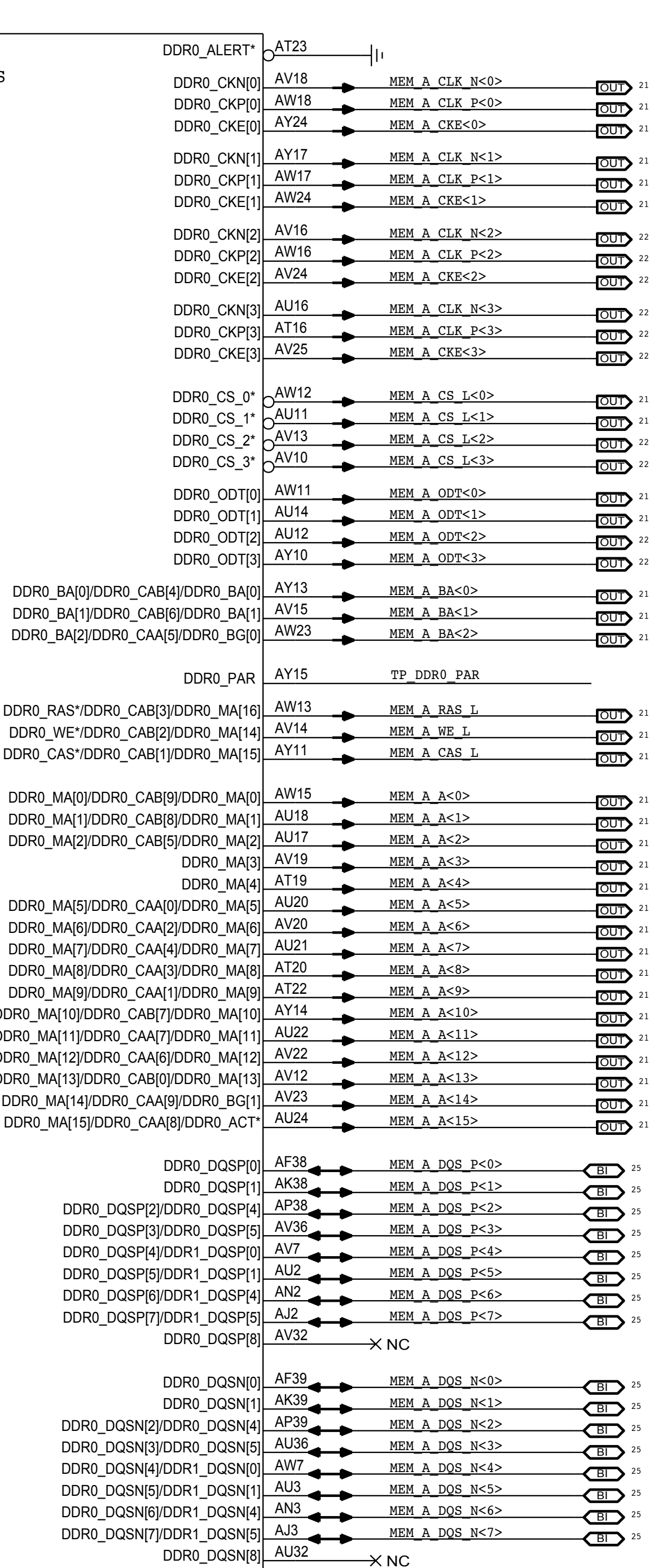
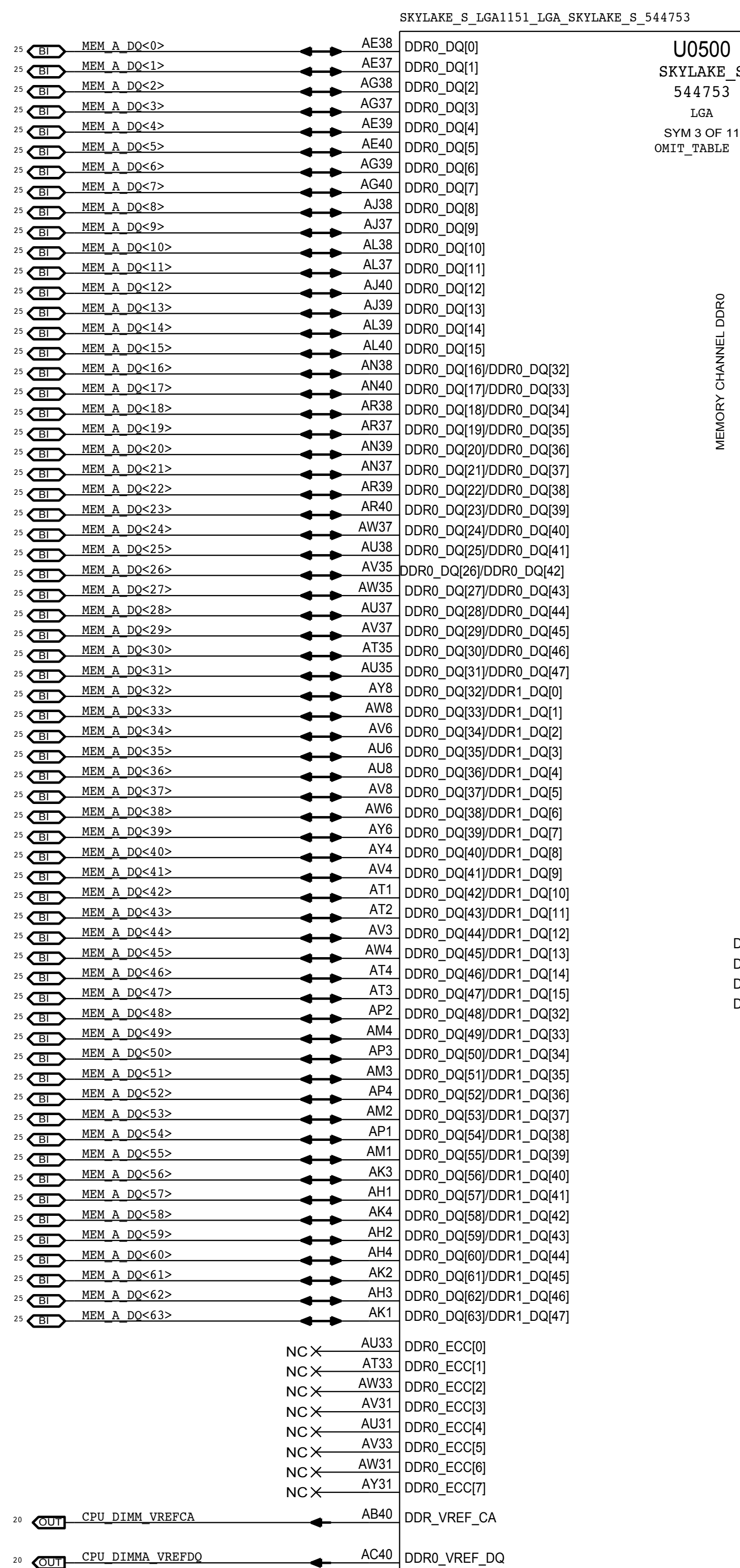


TP CPU RSVD TP1	H11	RSVD_TP
TP CPU RSVD TP2	H12	RSVD_TP
TP CPU RSVD TP3	AV1	RSVD_TP
TP CPU RSVD TP4	AV39	RSVD_TP
TP CPU RSVD TP5	AW2	RSVD_TP
TP CPU RSVD TP6	AW38	RSVD_TP
TP CPU RSVD TP7	J7	RSVD_TP
TP CPU RSVD TP8	J8	RSVD_TP
TP CPU RSVD TP9	K8	RSVD_TP
TP CPU RSVD TP10	L8	RSVD_TP

RSVD	K10	TP CPU RSVD TP12
RSVD	K11	TP CPU RSVD TP13
RSVD	K12	TP CPU RSVD TP14
RSVD	K13	TP CPU RSVD TP15

RSDV	<u>F35</u>	✗ NC
RSDV	<u>F37</u>	✗ NC
RSDV	<u>G35</u>	✗ NC
RSDV	<u>G34</u>	✗ NC
RSDV	<u>H33</u>	✗ NC
RSDV	<u>H34</u>	✗ NC
RSDV	<u>J33</u>	✗ NC
RSDV	<u>J35</u>	✗ NC
RSDV	<u>K32</u>	✗ NC
RSDV	<u>K34</u>	✗ NC
RSDV	<u>L31</u>	✗ NC
RSDV	<u>L33</u>	✗ NC
RSDV	<u>M32</u>	✗ NC
RSDV	<u>AB37</u>	✗ NC
RSDV	<u>AB38</u>	✗ NC
RSDV	<u>AC38</u>	✗ NC
RSDV	<u>AJ24</u>	✗ NC
RSDV	<u>AJ25</u>	✗ NC
RSDV	<u>AJ26</u>	✗ NC
RSDV	<u>AJ27</u>	✗ NC
RSDV	<u>AJ28</u>	✗ NC
RSDV	<u>AJ29</u>	✗ NC
RSDV	<u>AJ30</u>	✗ NC
RSDV	<u>AK21</u>	✗ NC
RSDV	<u>AK22</u>	✗ NC
RSDV	<u>AK27</u>	✗ NC

SYNC MASTER=J78 MLB PAGE TITLE		SYNC DATE=06/30/2014	
CPU & CHIPSET: CPU Clock/Misc/JTAG/CFG			
	DRAWING NUMBER 051-00673		SIZE D
	REVISION 0.24.0		
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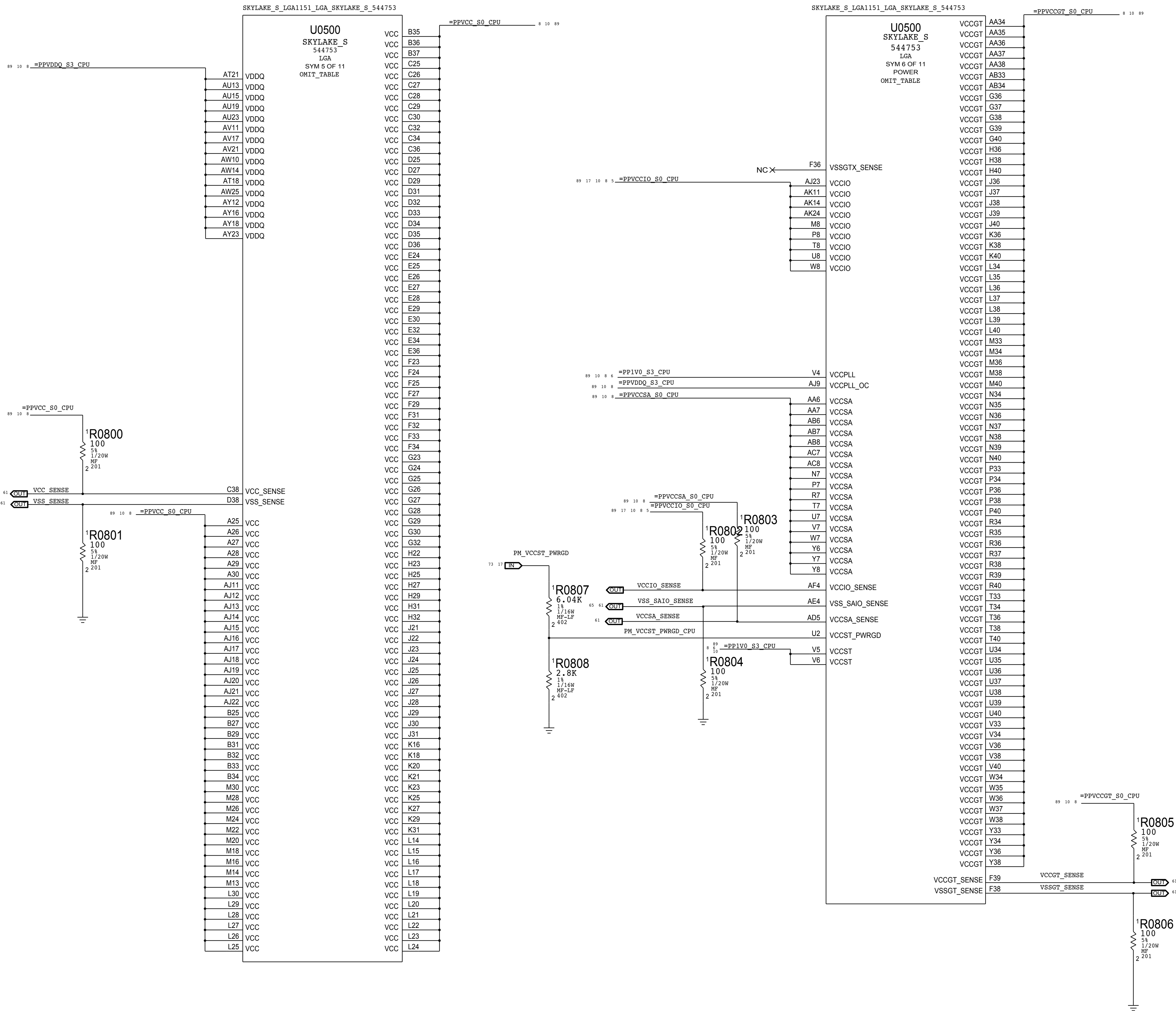
D


C

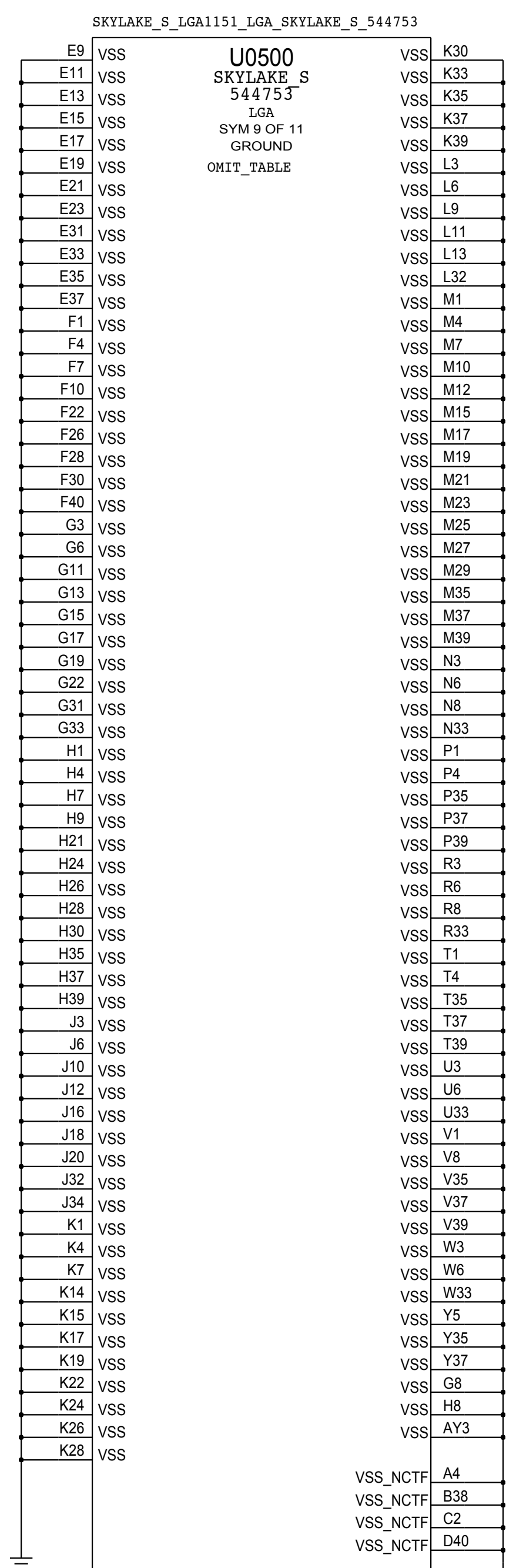
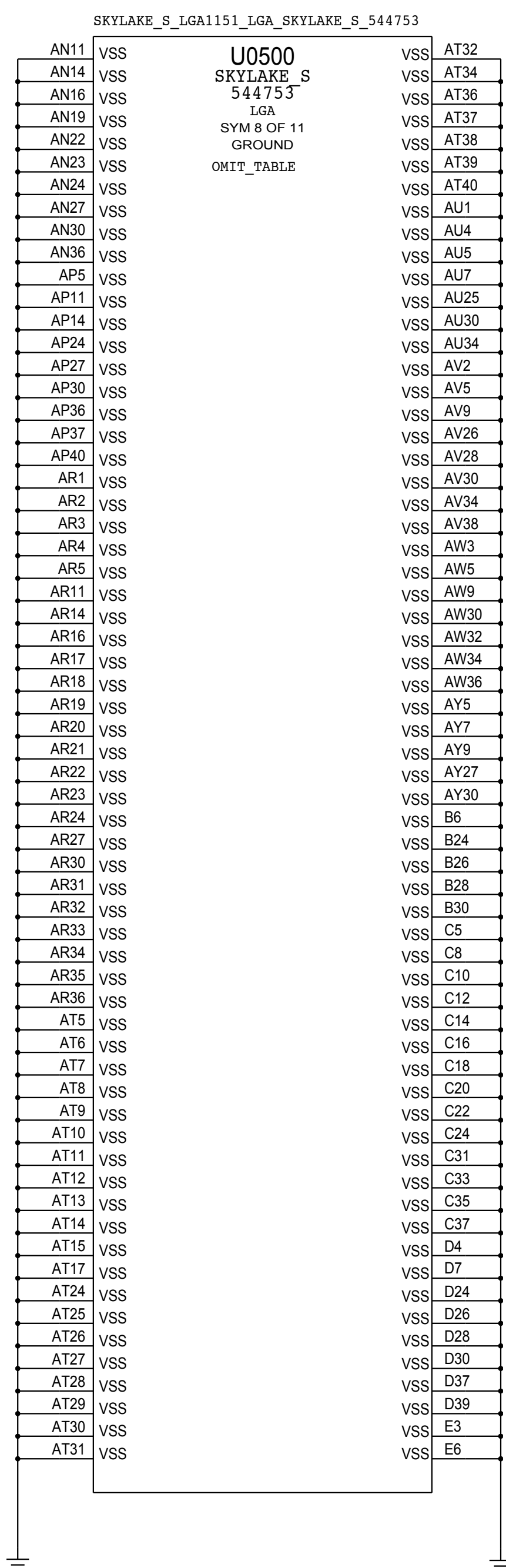
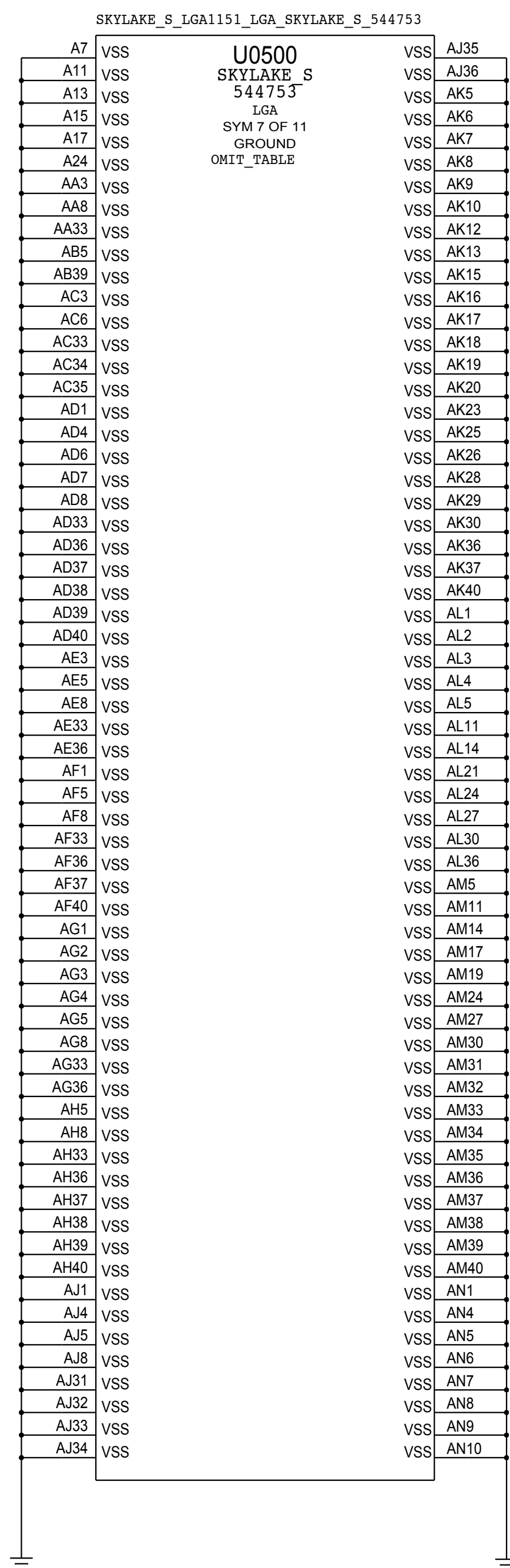
B

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Vinafix



SYNC_MASTER=J78_MLB		SYNC_DATE=06/30/2014	
PAGE TITLE			
CPU & CHIPSET: CPU Power			
	Apple Inc.	DRAWING NUMBER	051-00673
		REVISION	0.24.0
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		BRANCH	
		PAGE	8 OF 121
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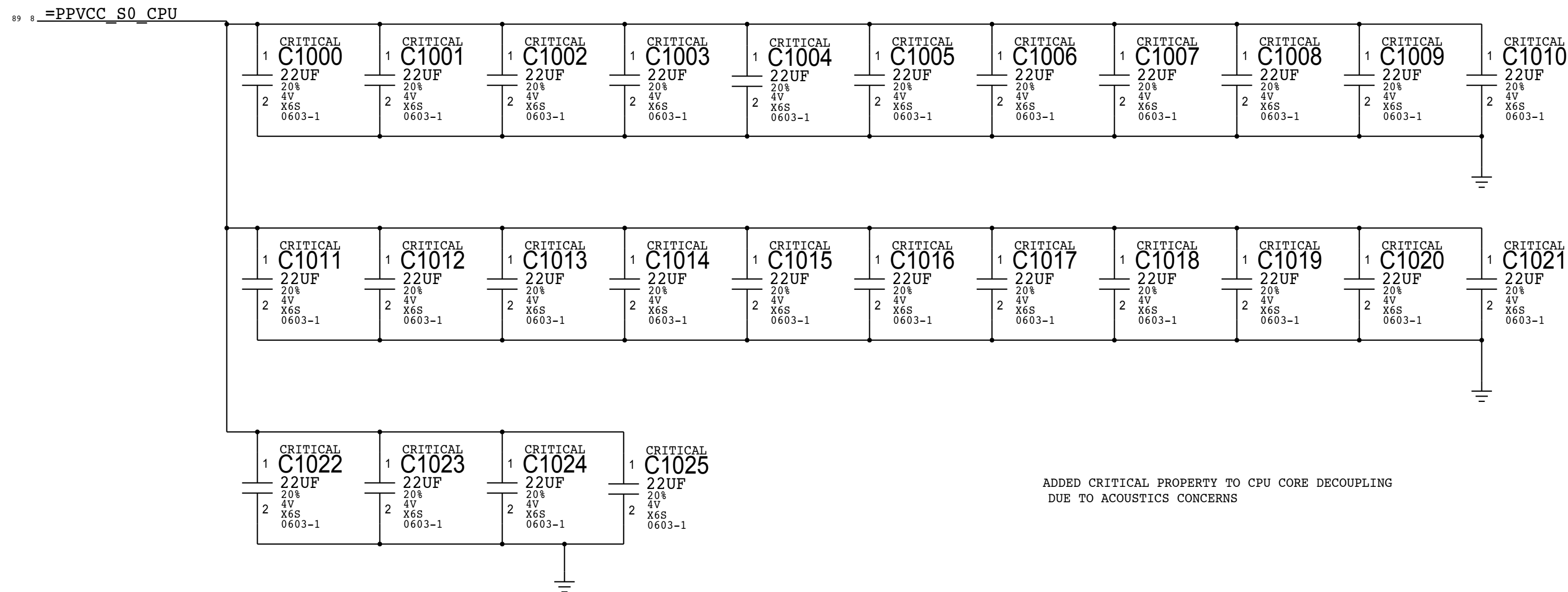


CPU VCORE DECOUPLING

Intel Recommendation: 12x 22UF 0805 (top side cavity)
6x 22UF 0603 (top side cavity)
5x 22UF 0805 (top side outside cavity)

Apple Implementation: 26x 22UF 0603

Layout Note: These caps should be placed symmetrically on Top and Bottom sides.
BULK CAPS ON CPU VREG PAGE 71



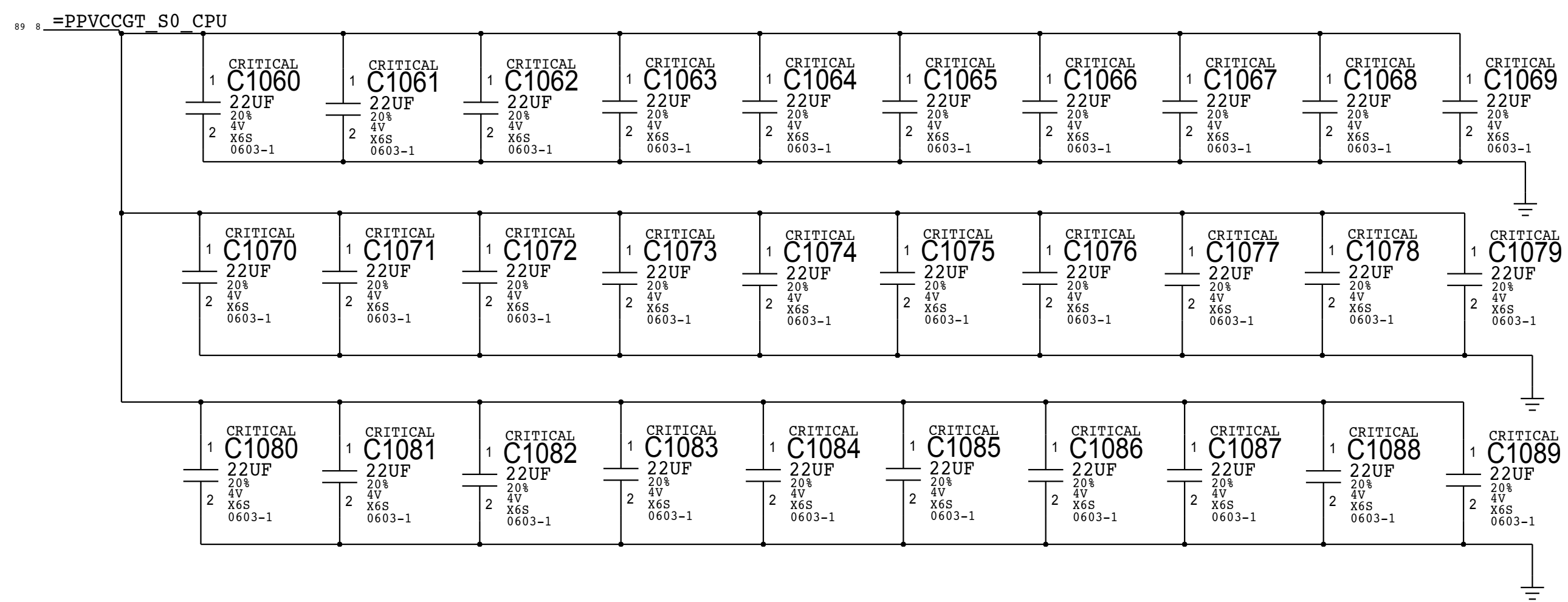
ADDED CRITICAL PROPERTY TO CPU CORE DECOUPLING
DUE TO ACOUSTICS CONCERNS

CPU GT DECOUPLING

Intel Recommendation: 9x 47UF 0805 (top side cavity)
4x 47UF 0805 (top side outside cavity)

Apple Implementation: 30x 22uF 0603

Layout Note: These caps should be placed symmetrically on Top and Bottom sides.

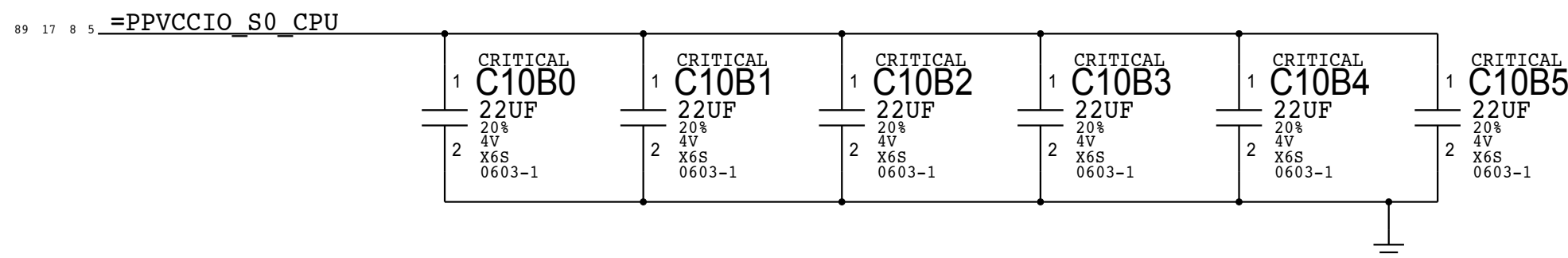


CPU VCCIO DECOUPLING

Intel Recommendation: 5x 22UF 0603 (top side cavity)
1x 22UF 0805 (top side cavity)

Apple Implementation:(following Intel recommendation w/ 0603)

Layout Note: These caps should be placed symmetrically on Top and Bottom sides.

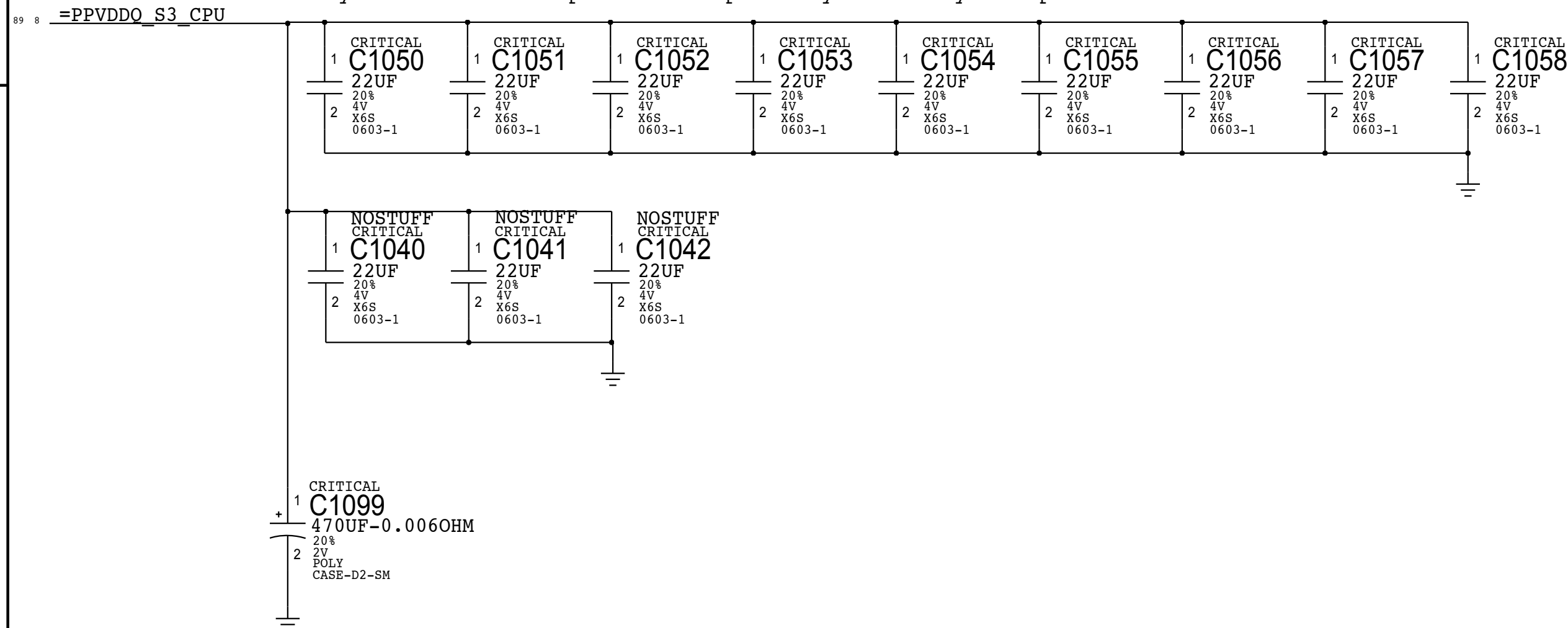


Memory (CPU VCCDDR) DECOUPLING

Intel Recommendation: 4x 22UF 0603 (top side outside cavity)

Apple Implementation: 9x 22UF 0603 (J78 carry over)

Layout Note: These caps should be placed symmetrically on Top and Bottom sides.

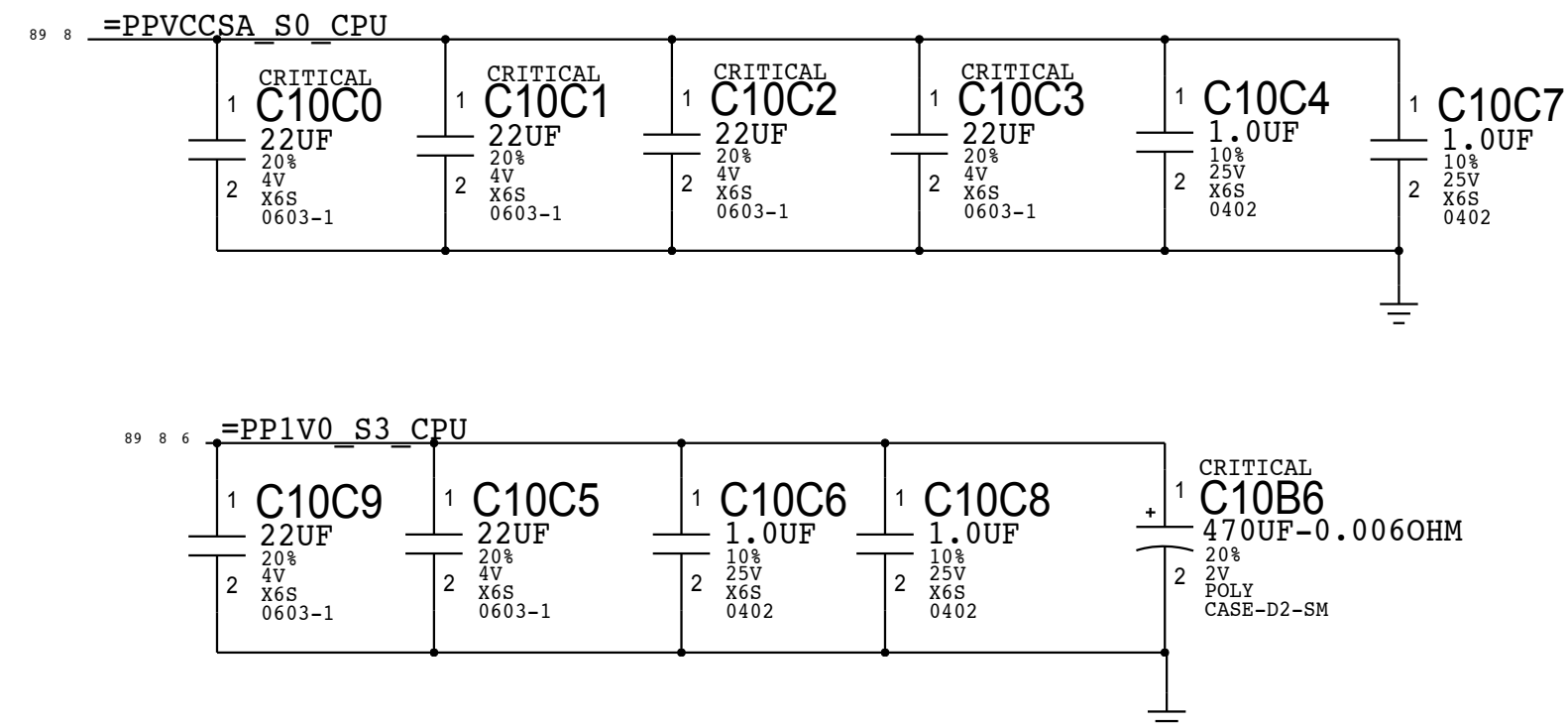



CPU VCCSA / VCCST+VCCPLL DECOUPLING

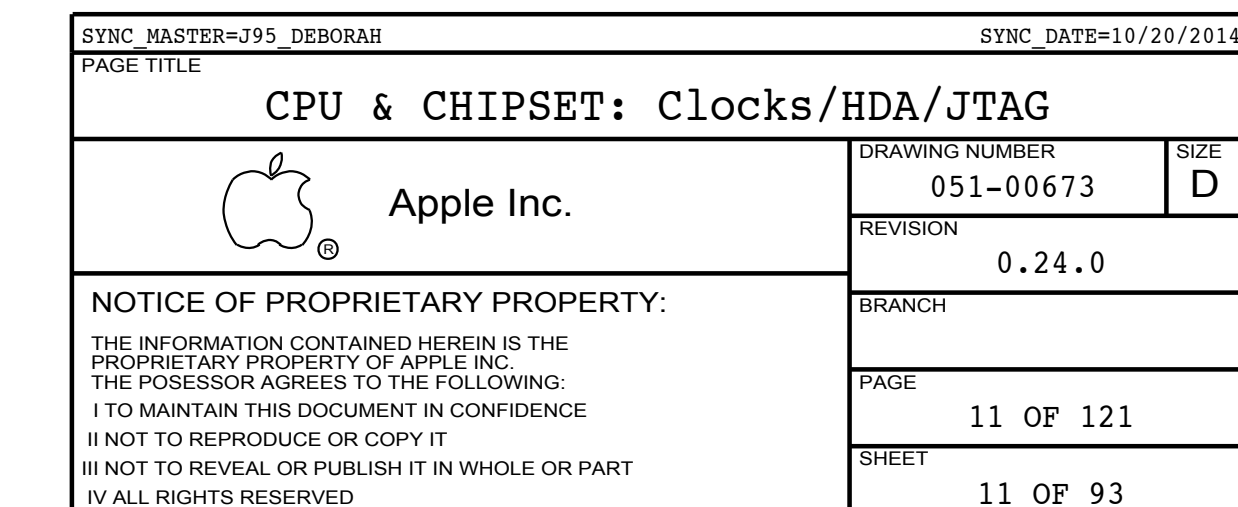
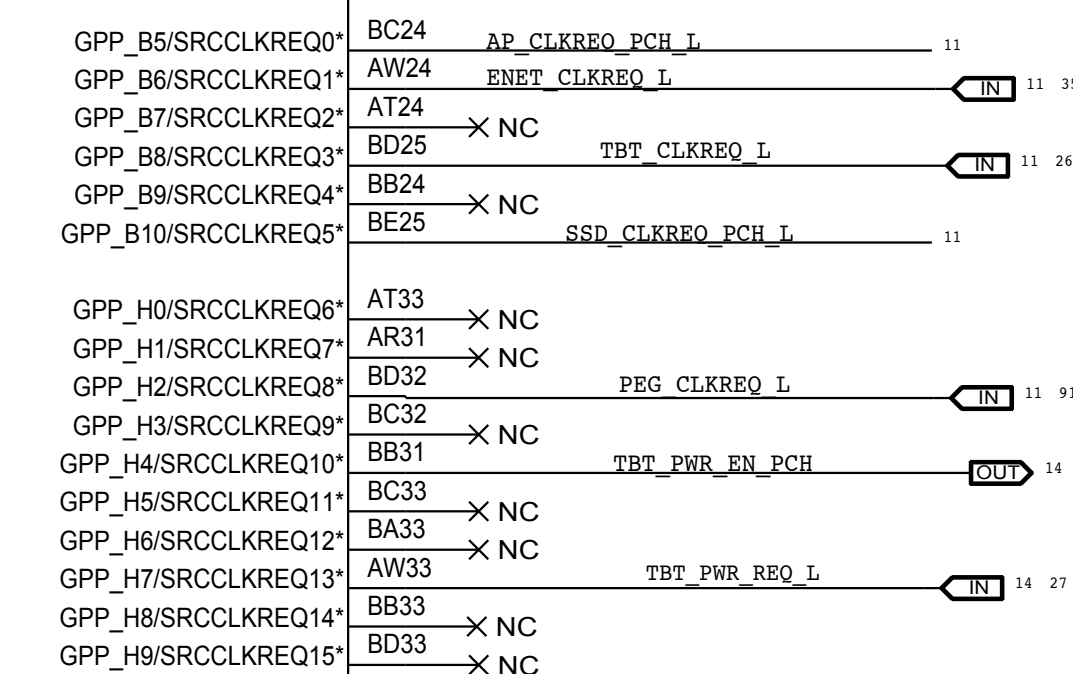
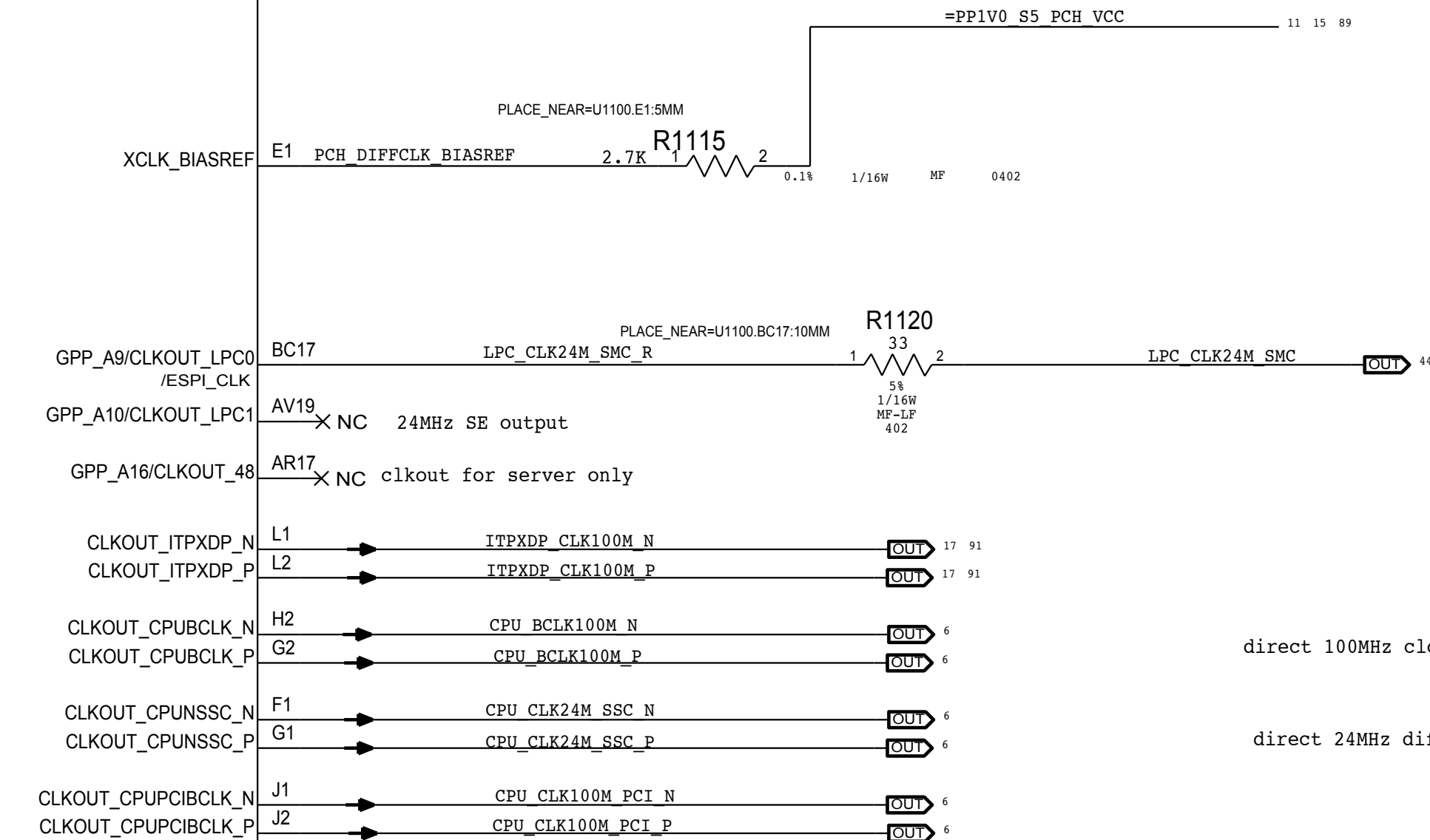
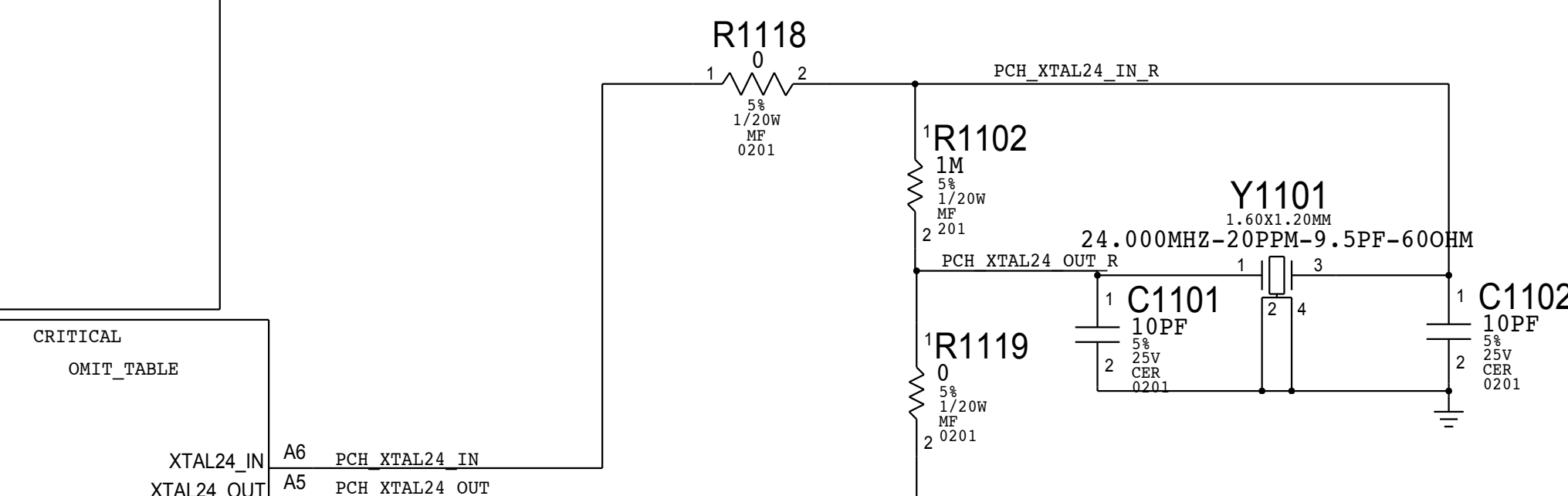
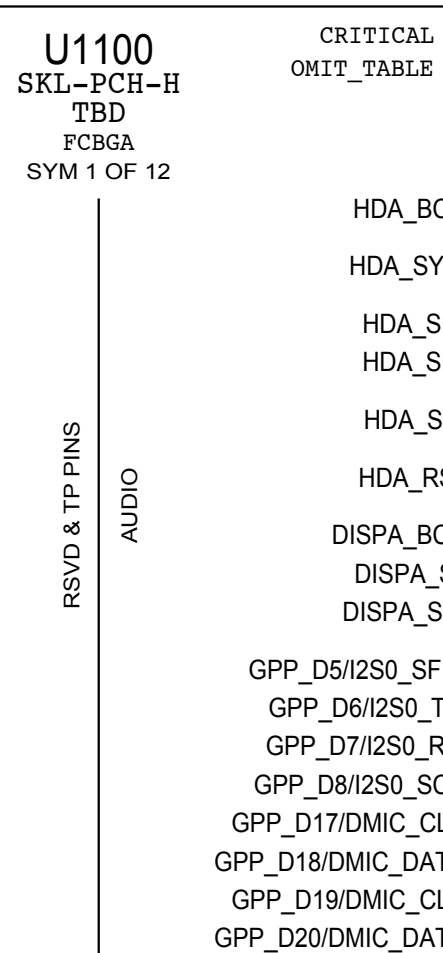
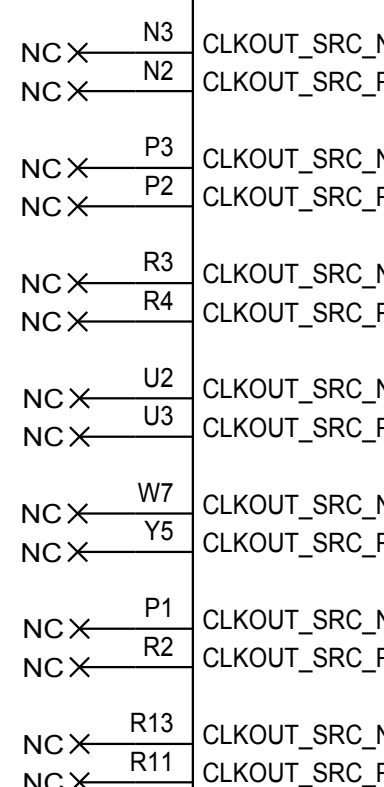
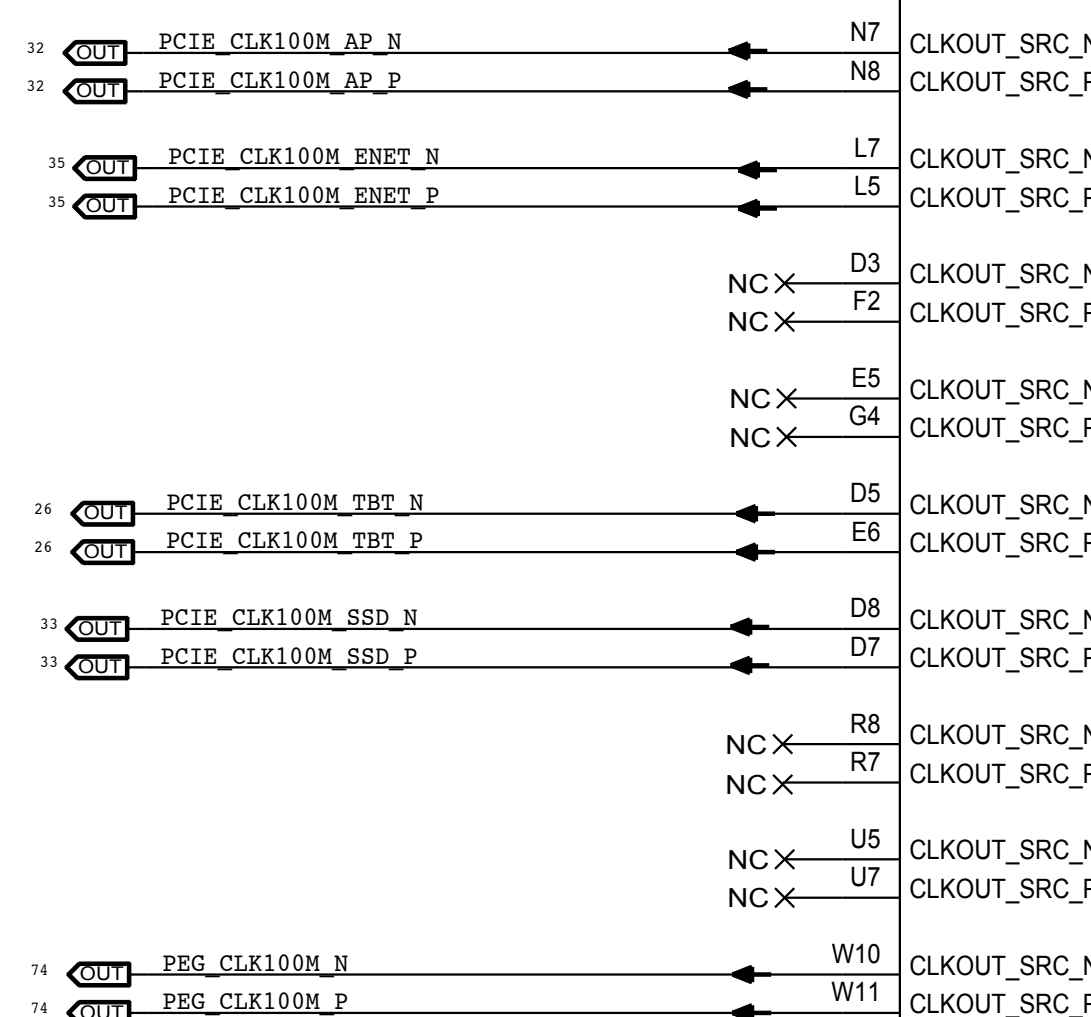
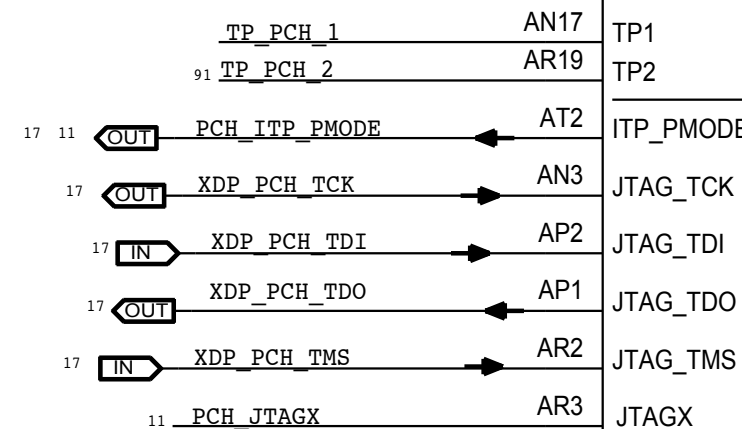
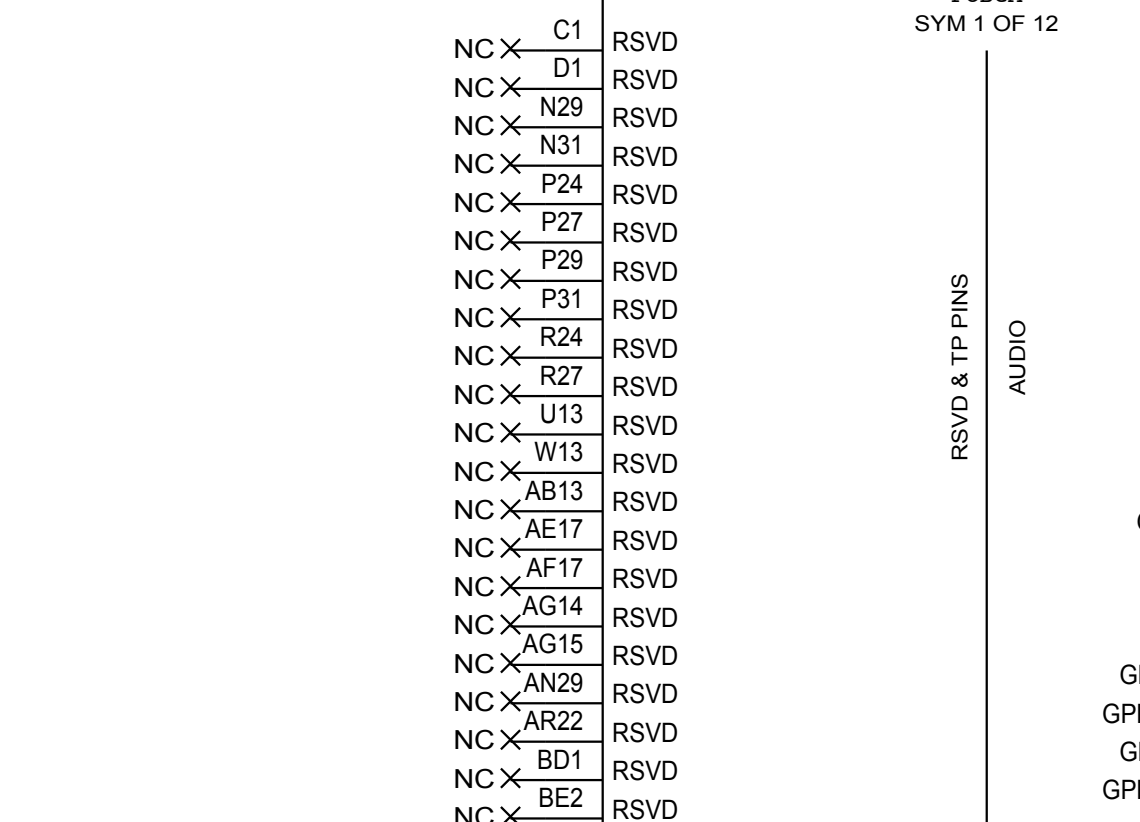
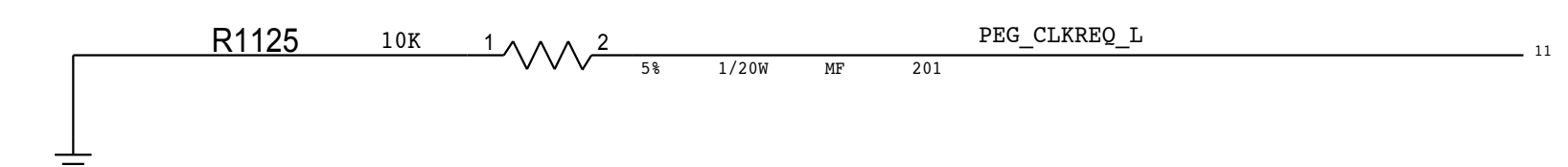
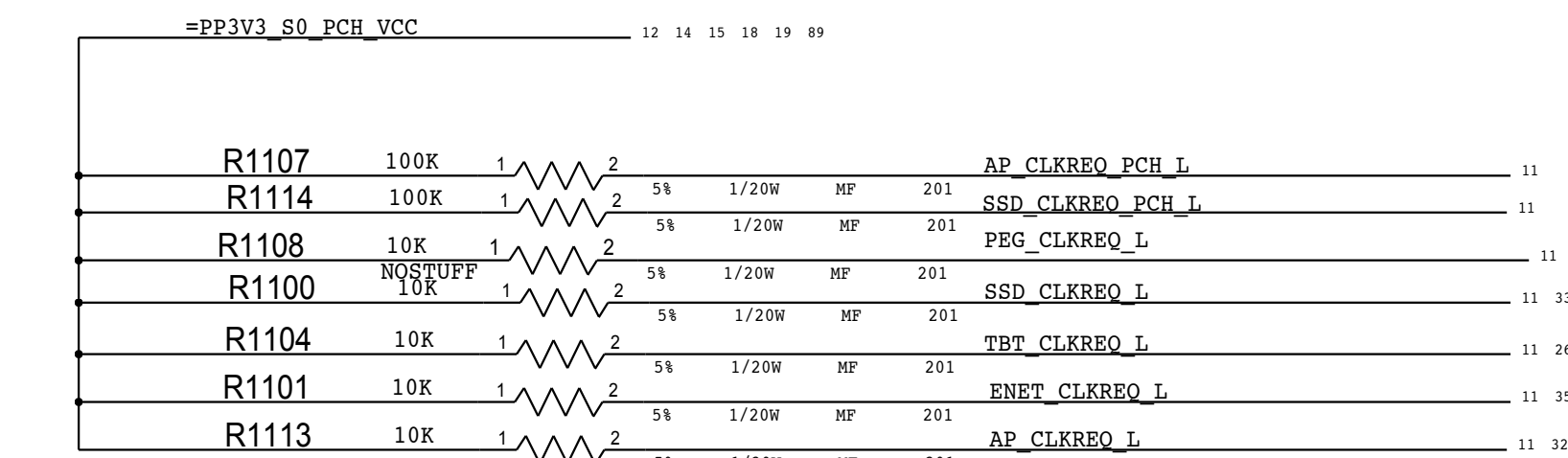
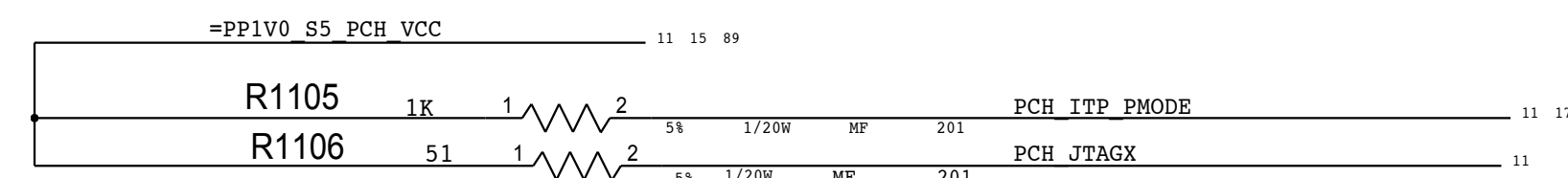
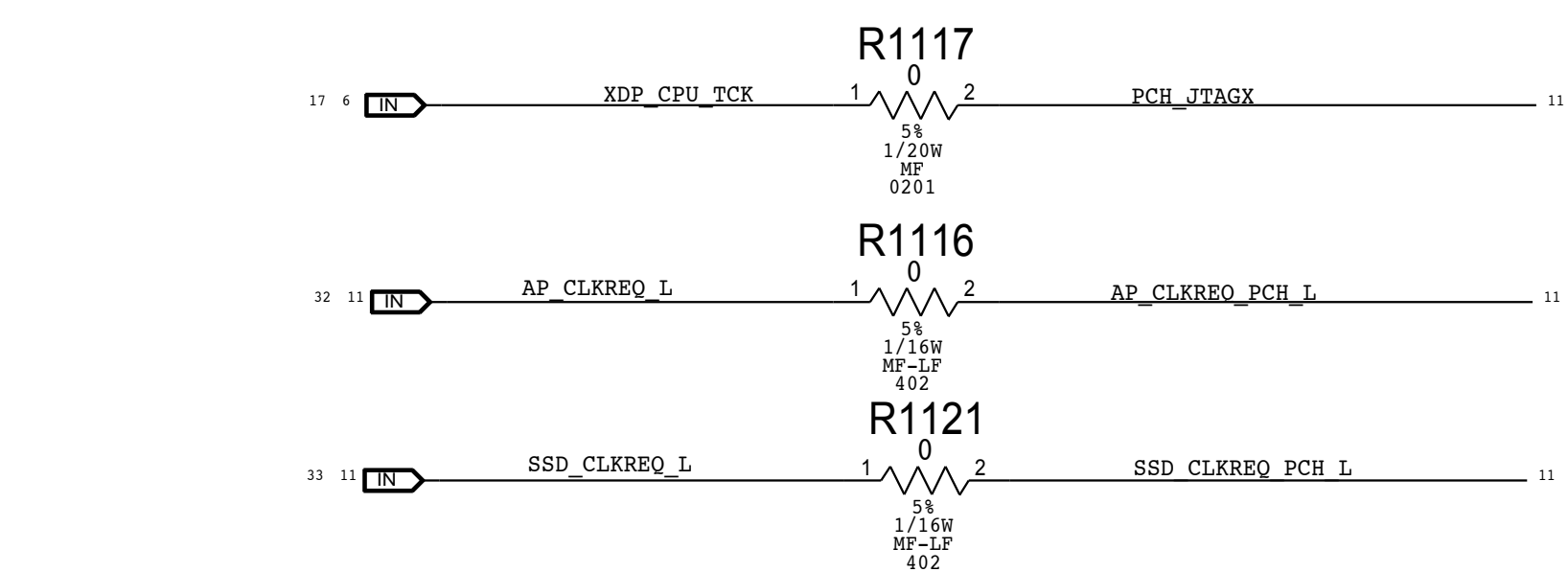
Intel Recommendation: 2x 22UF 0603 near top side cavity

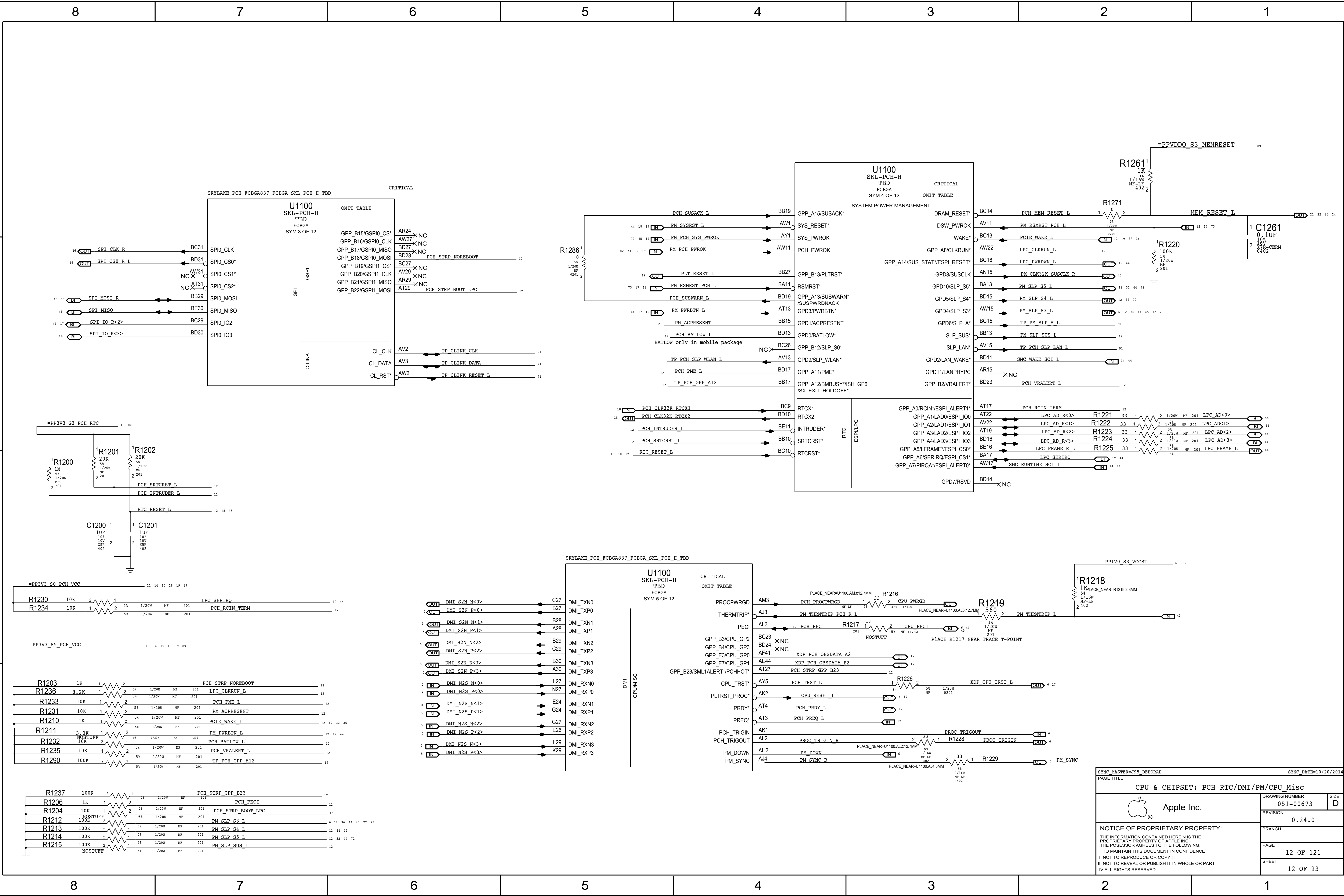
Apple Implementation: VCCST/VCCPLL: 1X 22UF 0603/2X 1UF 0402

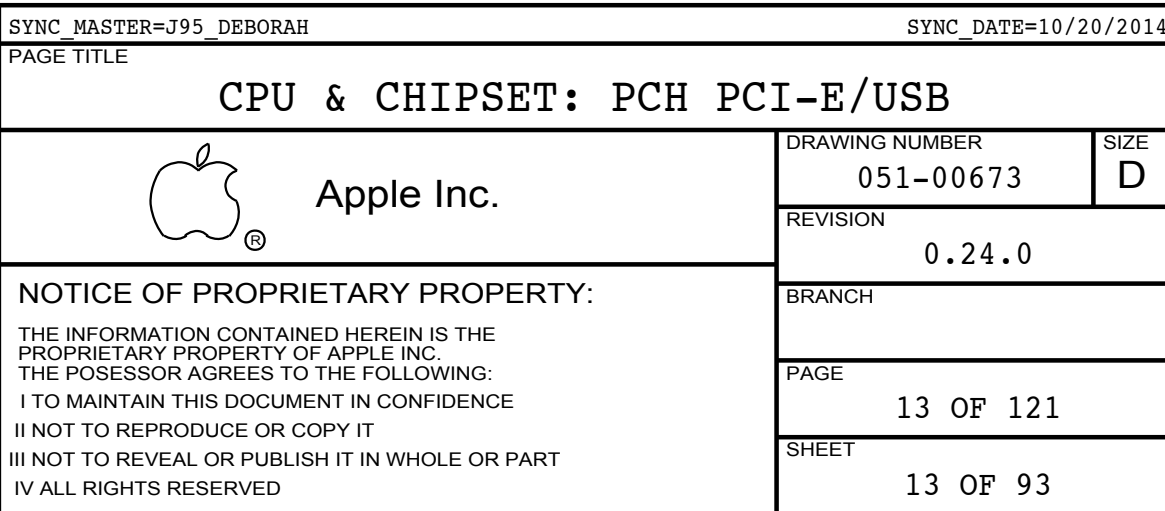
Layout Note: These caps should be placed on top side cavity.

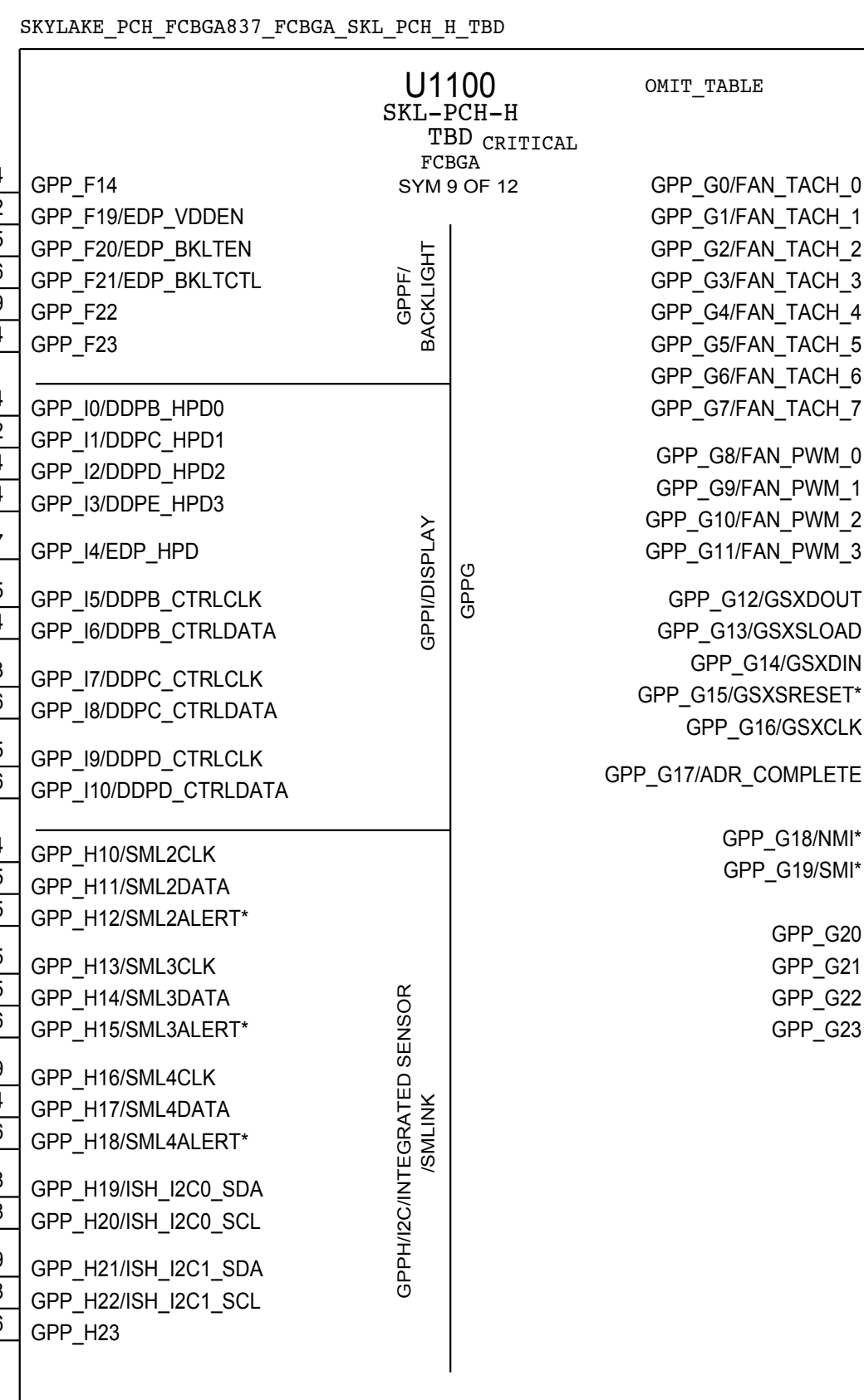
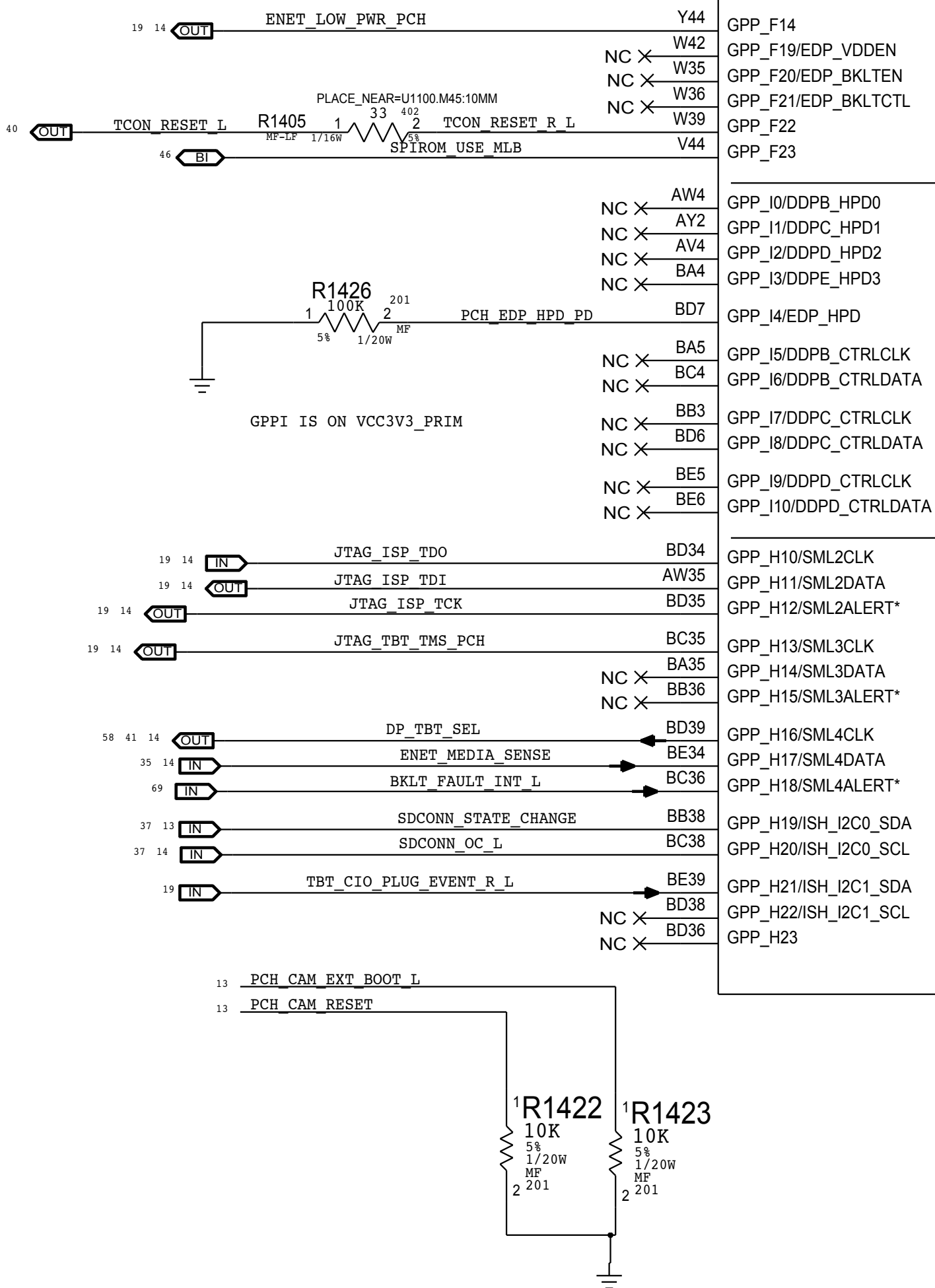
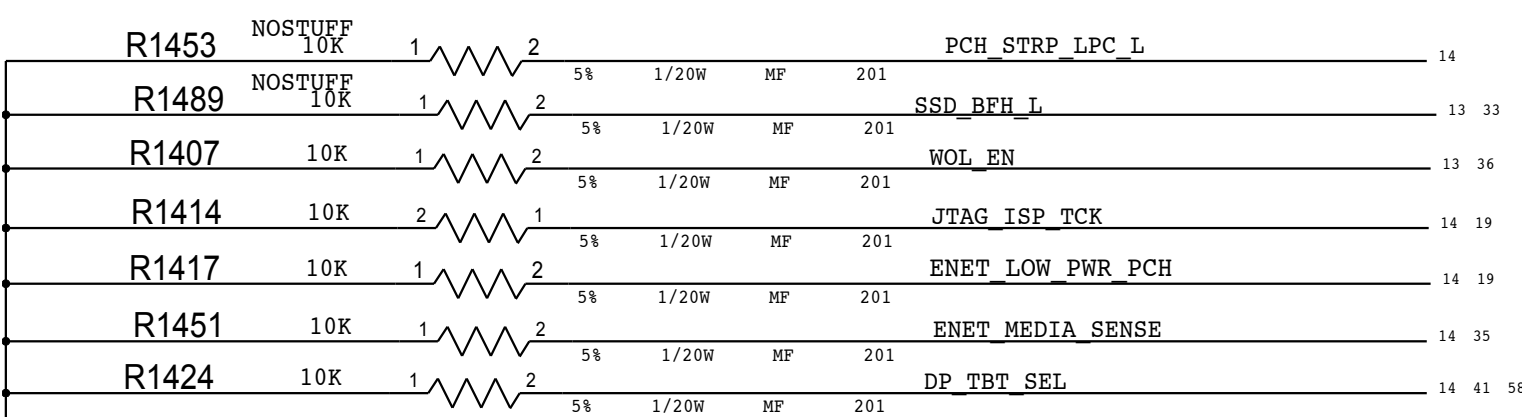
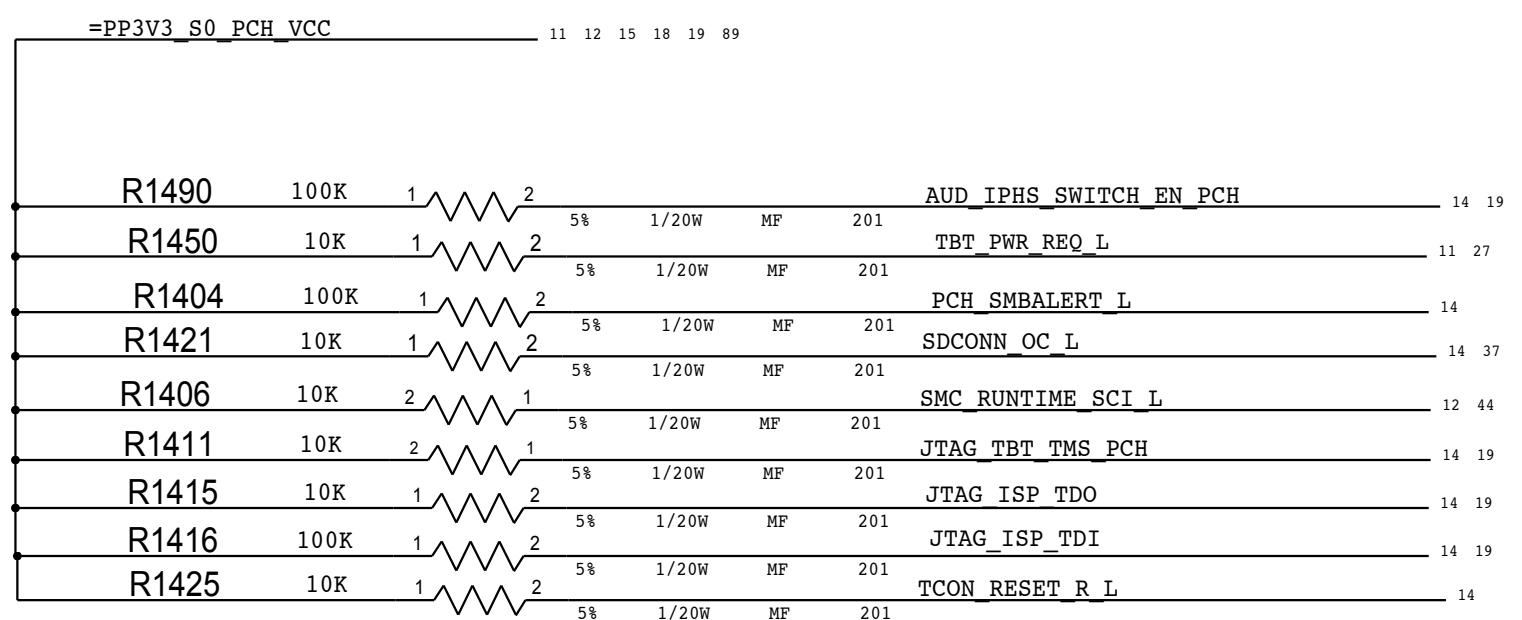
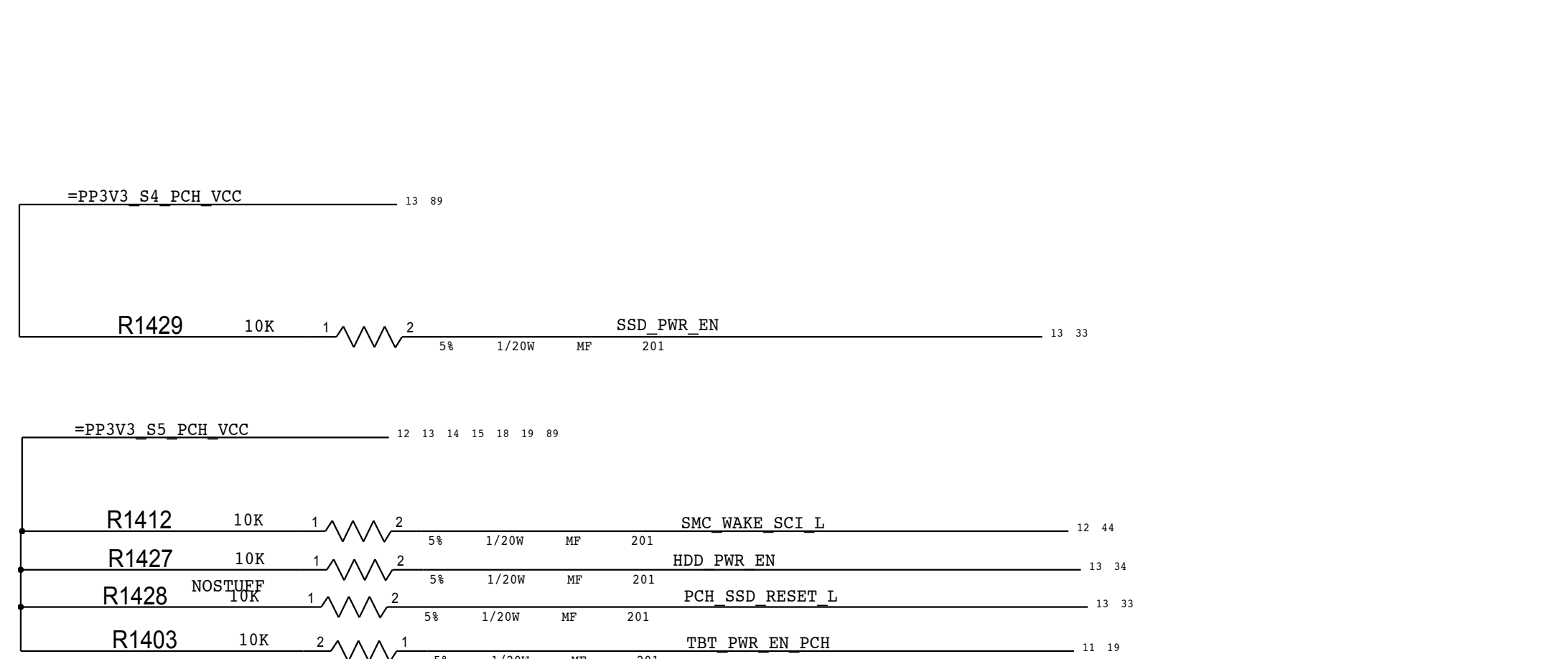
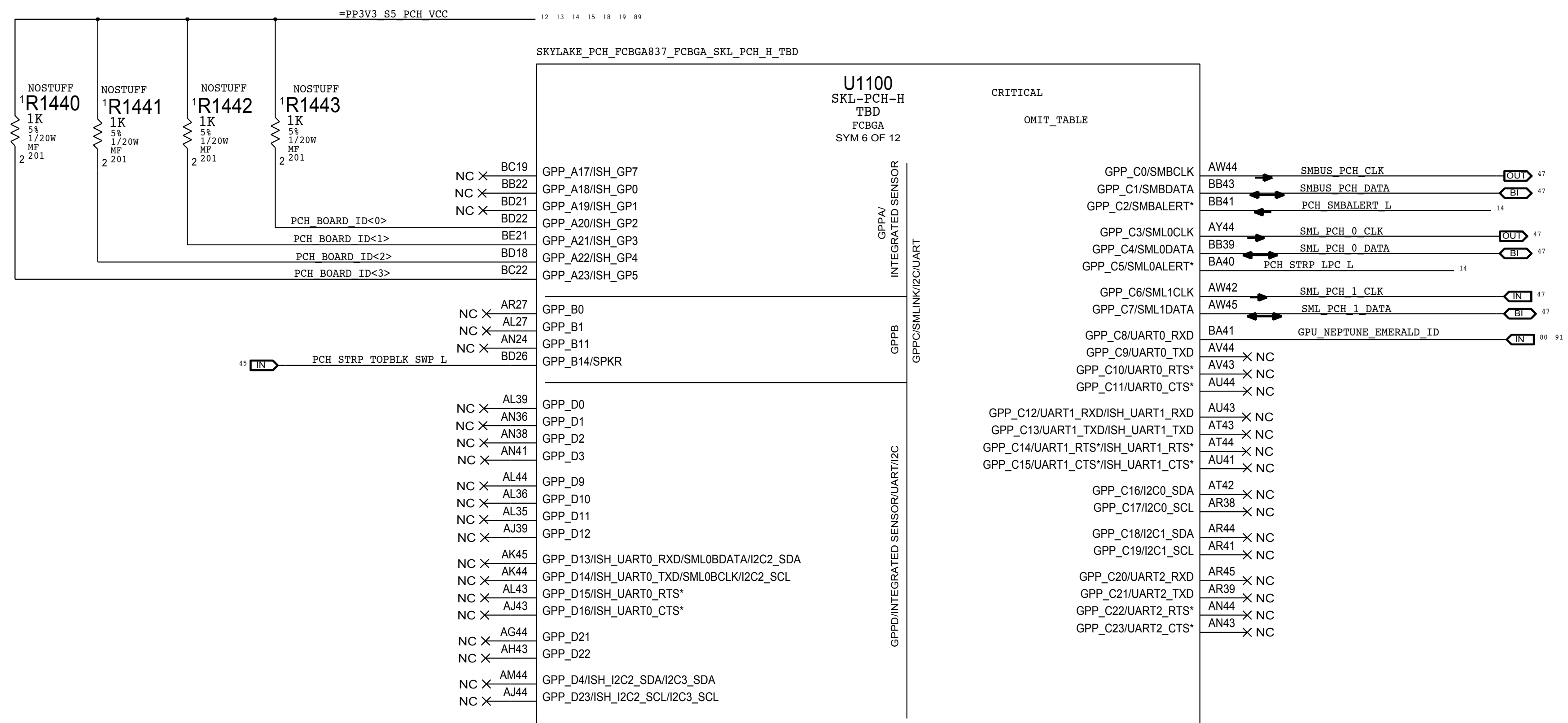



SYNC MASTER=J78 MLB		SYNC DATE=06/30/2014	
PAGE TITLE			
CPU & CHIPSET: CPU Decoupling			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-00673		D
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		0.24.0	
		BRANCH	
		PAGE	
		10 OF 121	
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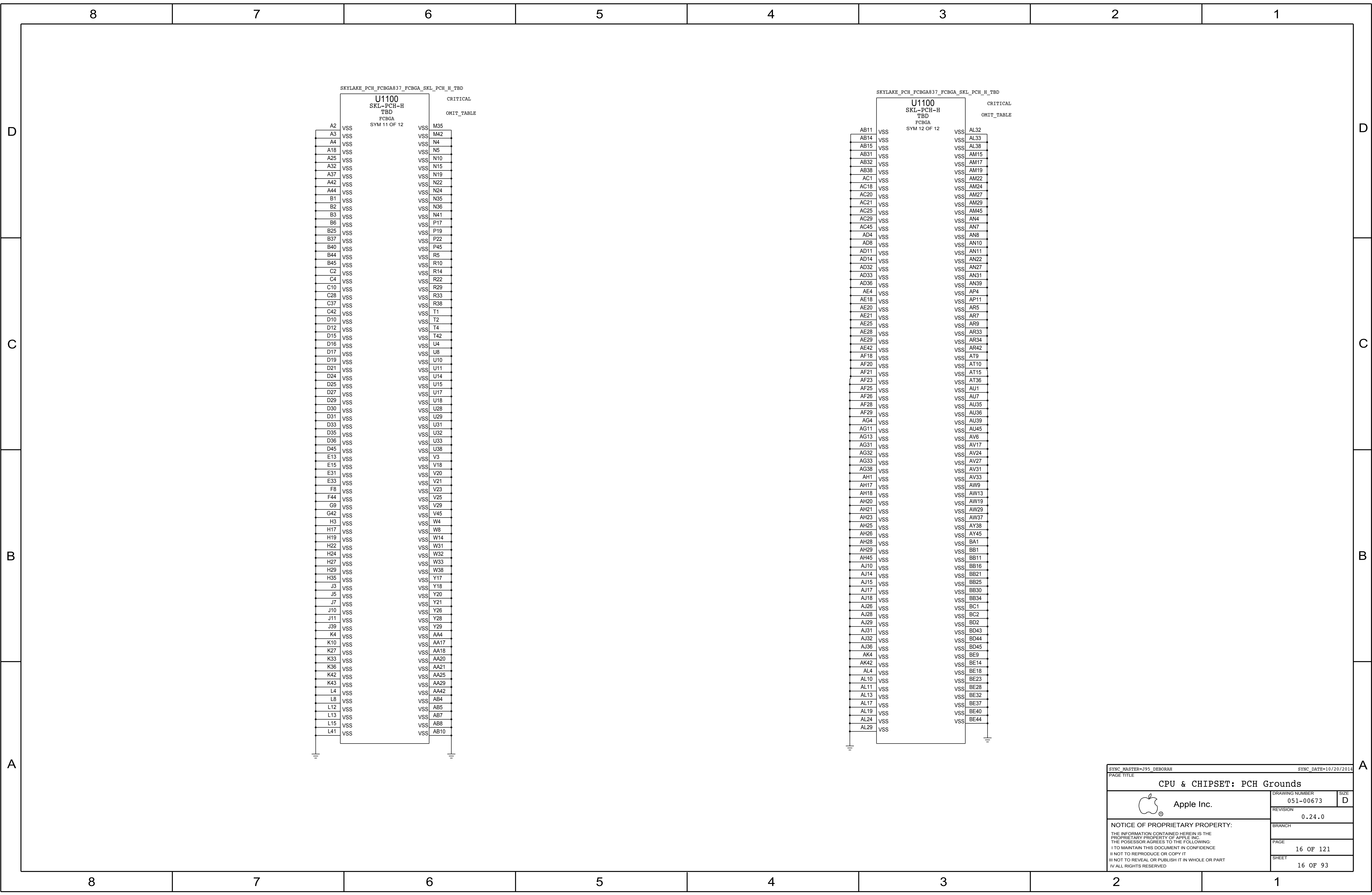




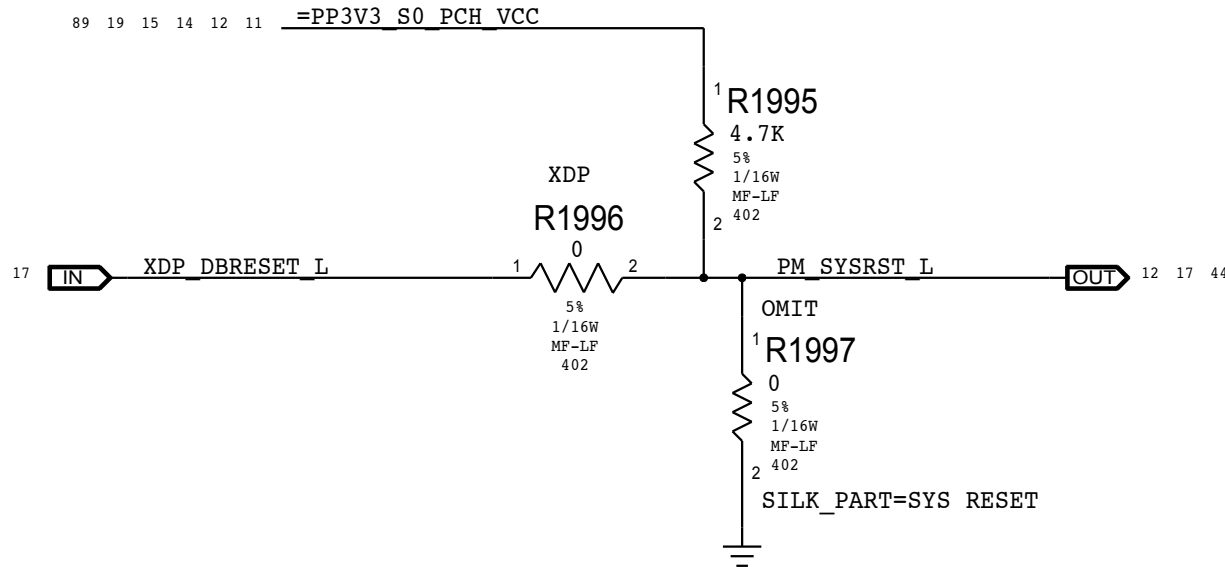




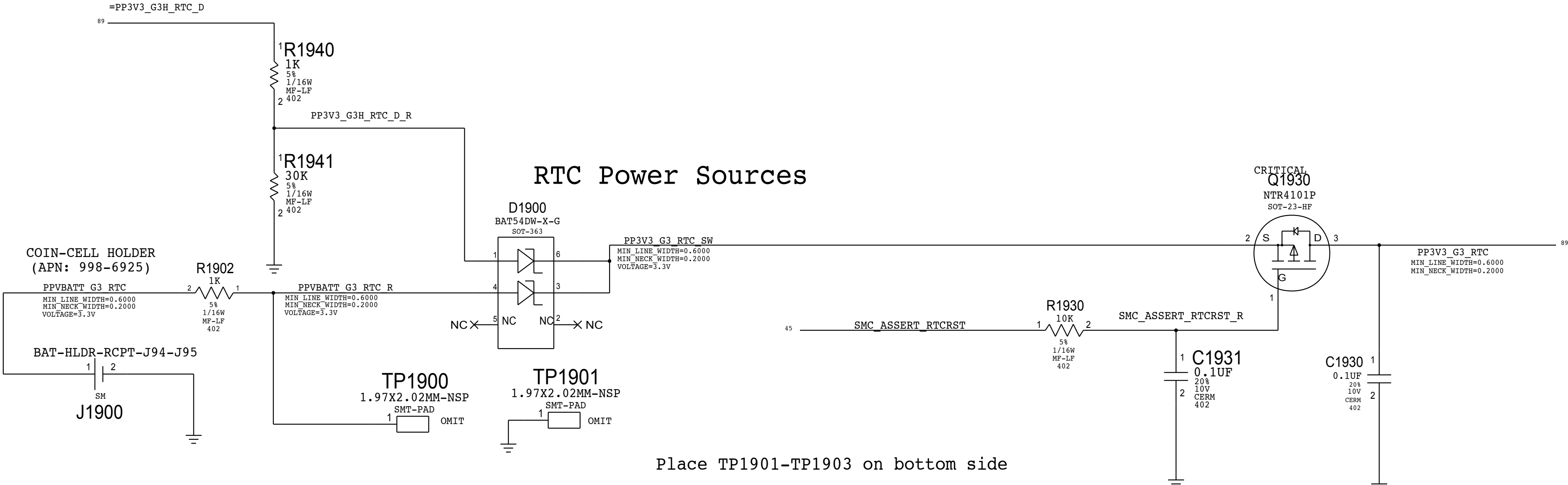
SYNCHMASTER=J95_DEBORAH		SYNCHDATE=10/20/2014	
PAGE TITLE			
CPU & CHIPSET: PCH GPIO/Misc			
 Apple Inc.	DRAWING NUMBER 051-00673		SIZE D
	REVISION 0.24.0		
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PCH Reset Button

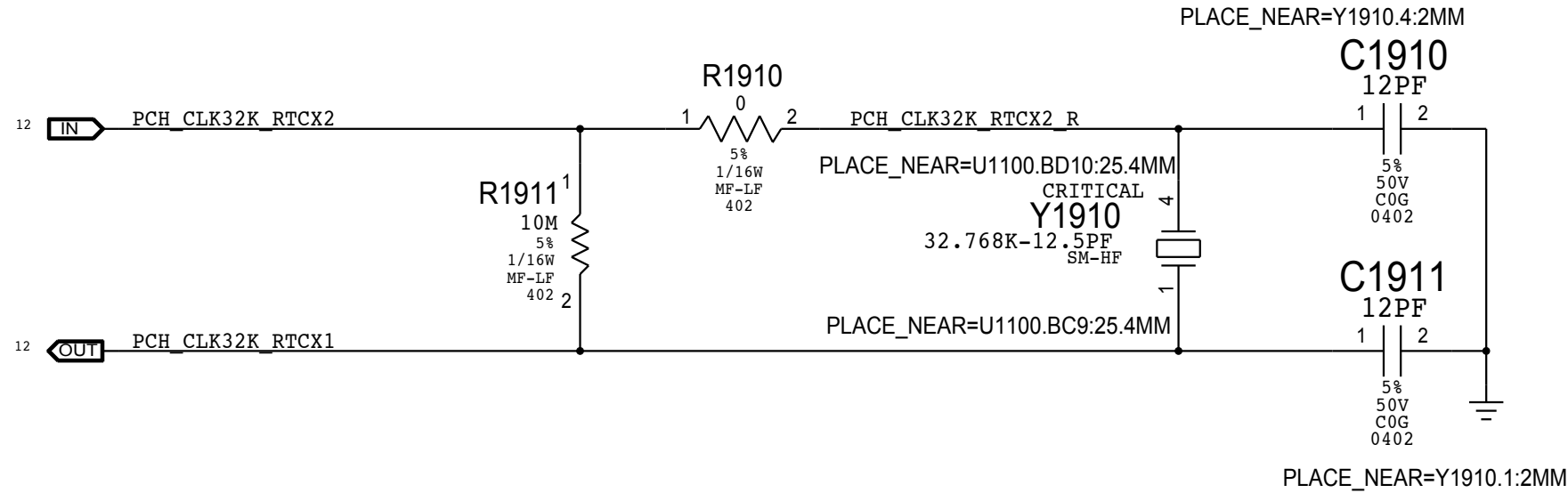


RTC Power Sources



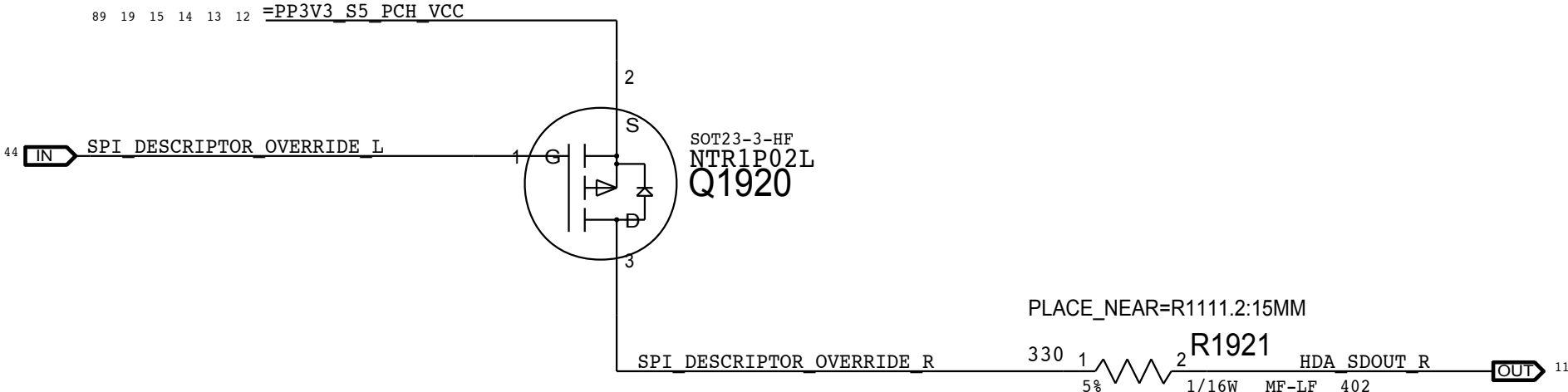
Place TP1901-TP1903 on bottom side

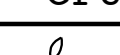
PCH RTC Crystal



PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting.



SYNC_MASTER=BRANCH_SYEDKAR		SYNC_DATE=09/10/2014	
PAGE TITLE			
CPU & CHIPSET: Chipset Support			
	DRAWING NUMBER		SIZE
	051-00673		D
Apple Inc.		REVISION	
		0.24.0	
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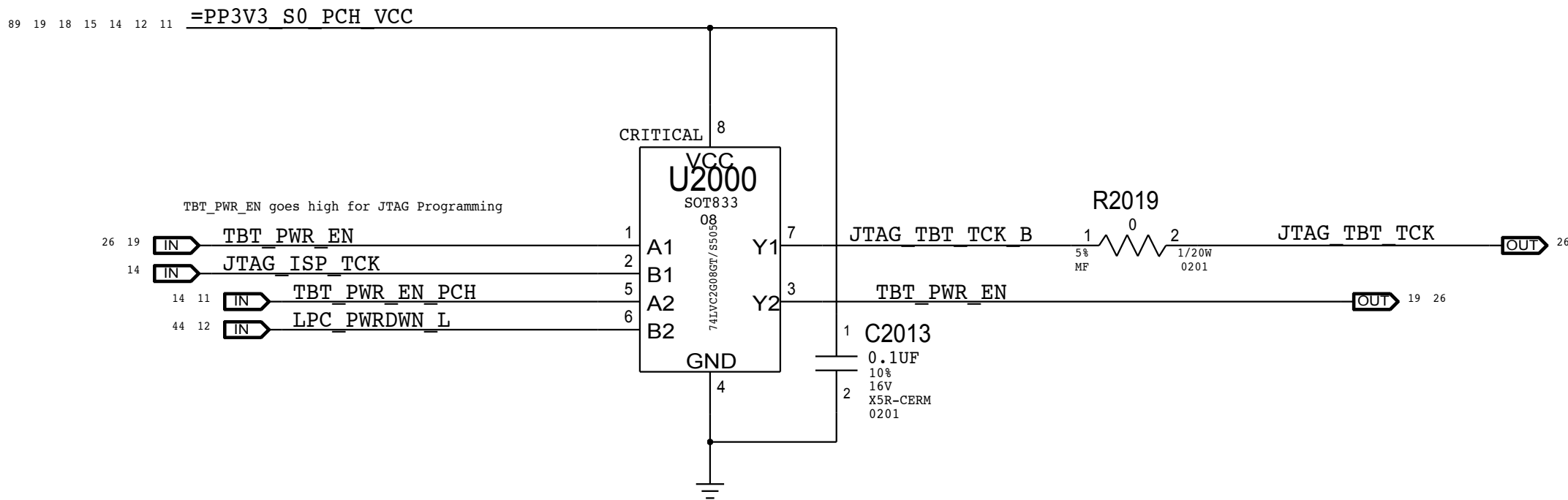
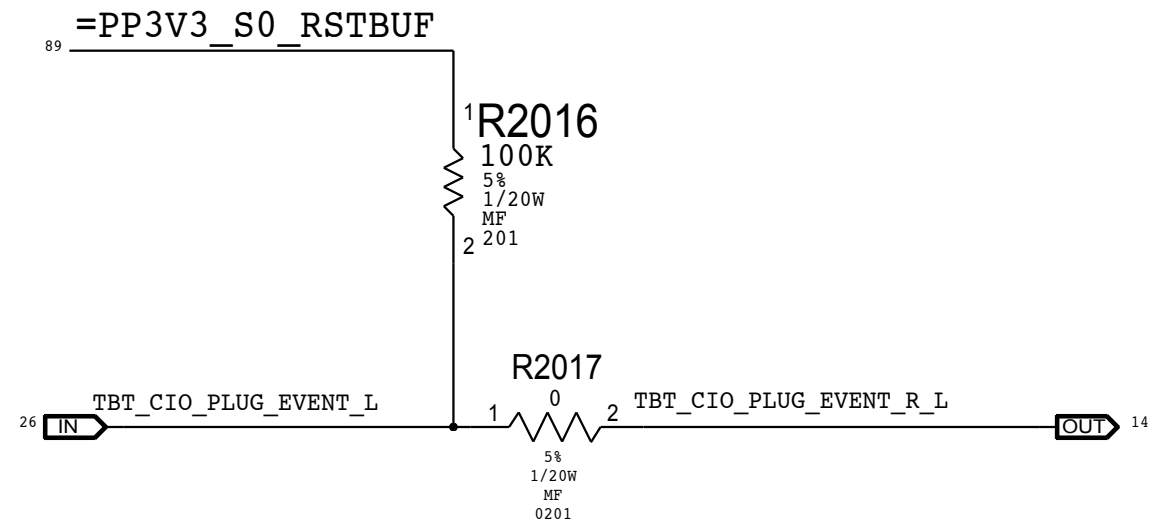
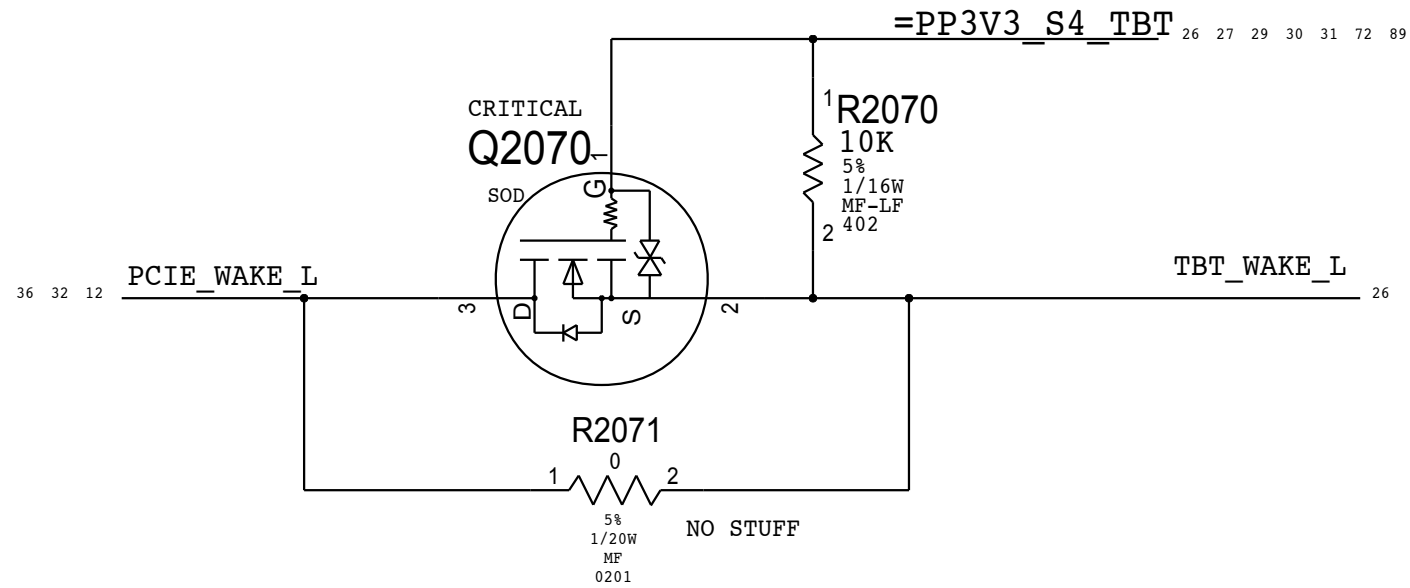
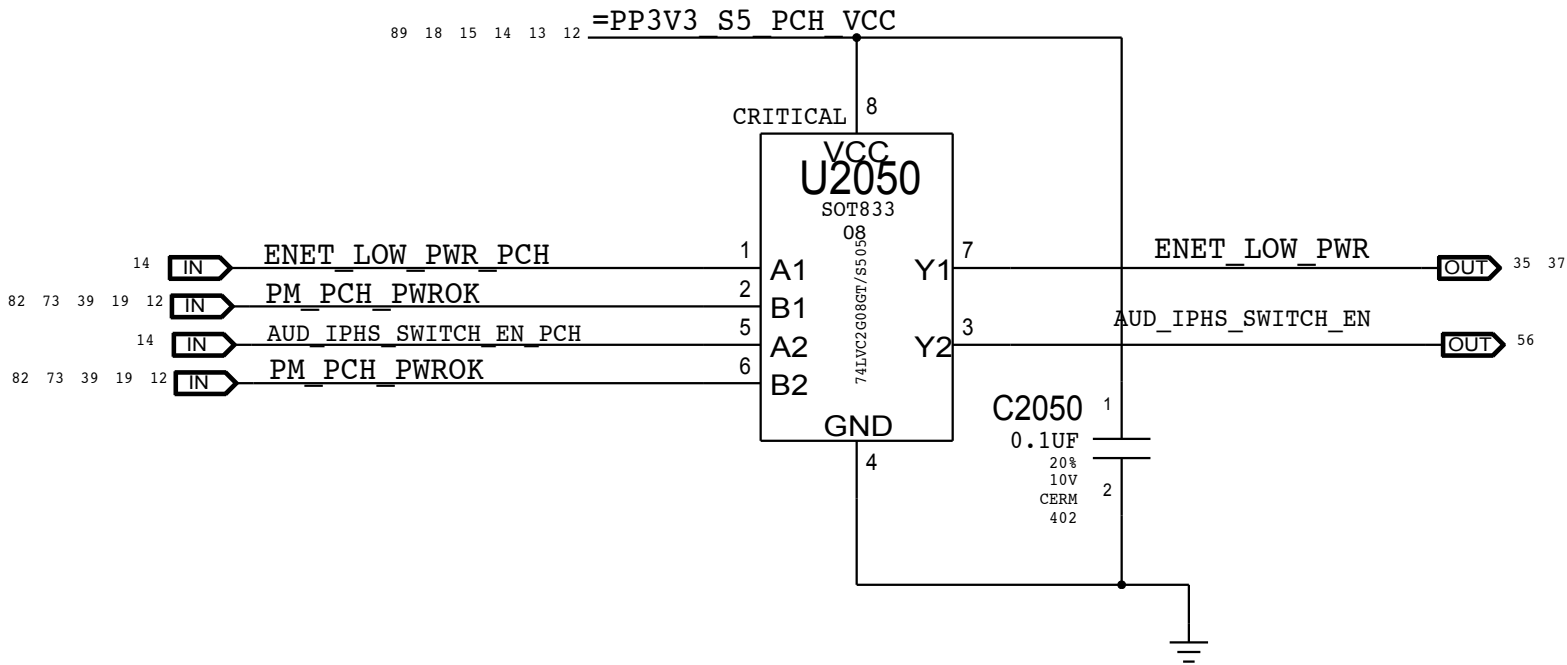
D

C

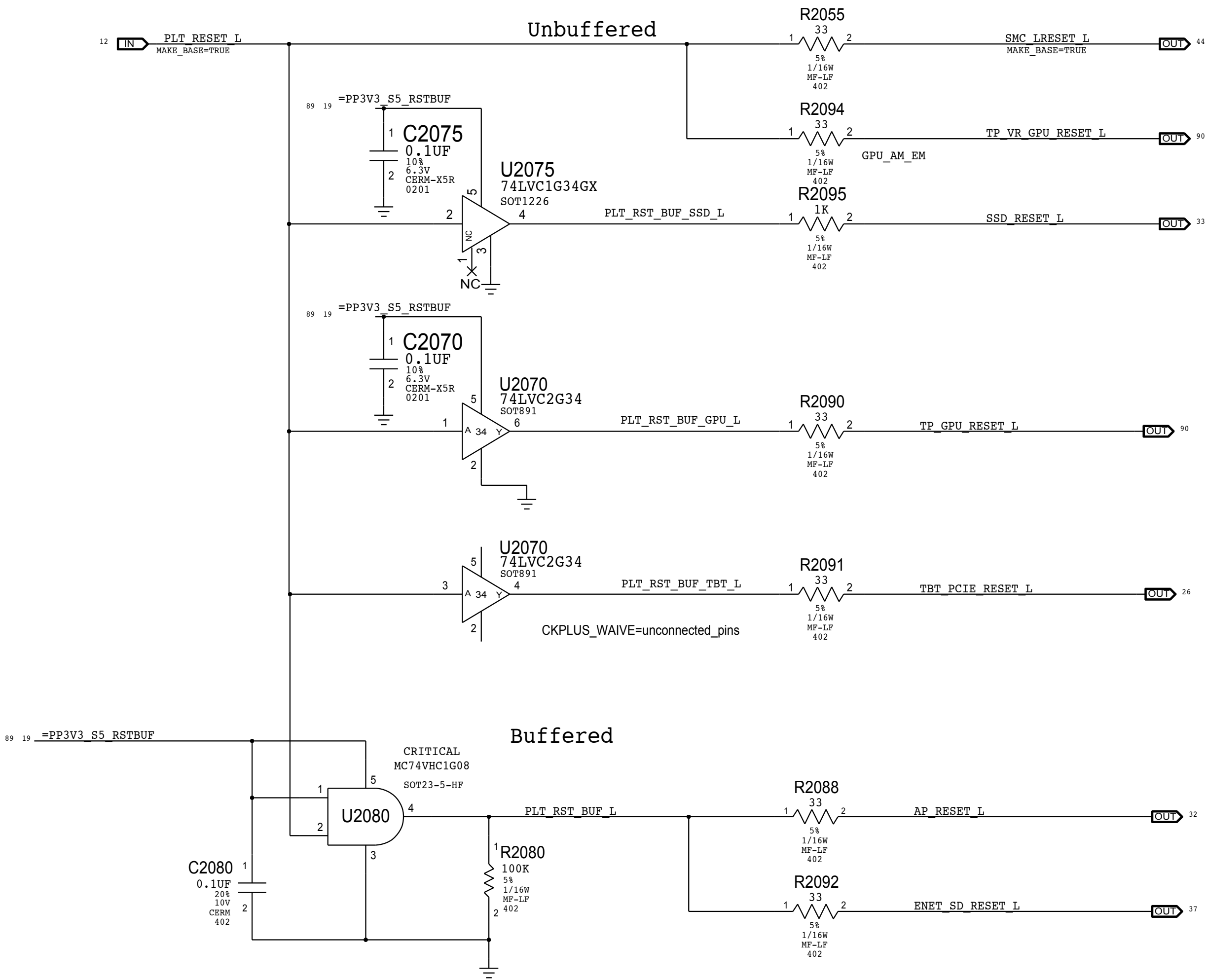
B

A

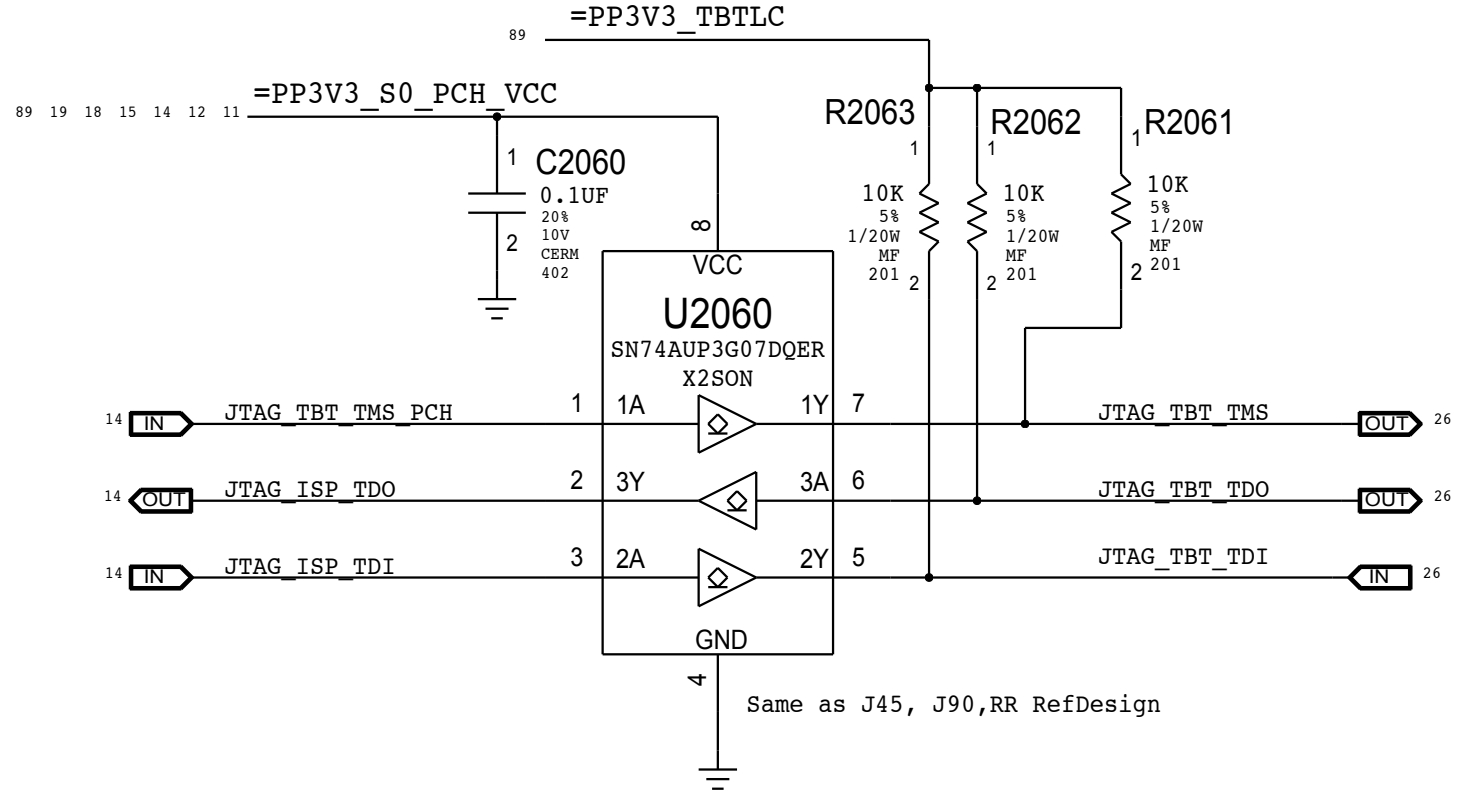
GPIO Glitch Prevention




Platform Reset Connections



TBT_LC can be on when S0 is off and vice-versa.
Isolation ensure no leakage to FR or PCH
U2060 Supports I/Os powered when VCC = 0V



SYNC_MASTER=J16_IG		SYNC_DATE=04/29/2013	
PAGE TITLE			
CPU & CHIPSET: Project Chipset Support			
 Apple Inc.		DRAWING NUMBER	051-00673
		REVISION	0.24.0
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Page Notes

Power aliases required by this page:

- =PP1V5_S0_MEM_A

- =PPVDDQ_S3_MEM_A

- =PPDDRVTT_S0_MEM_A

- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:

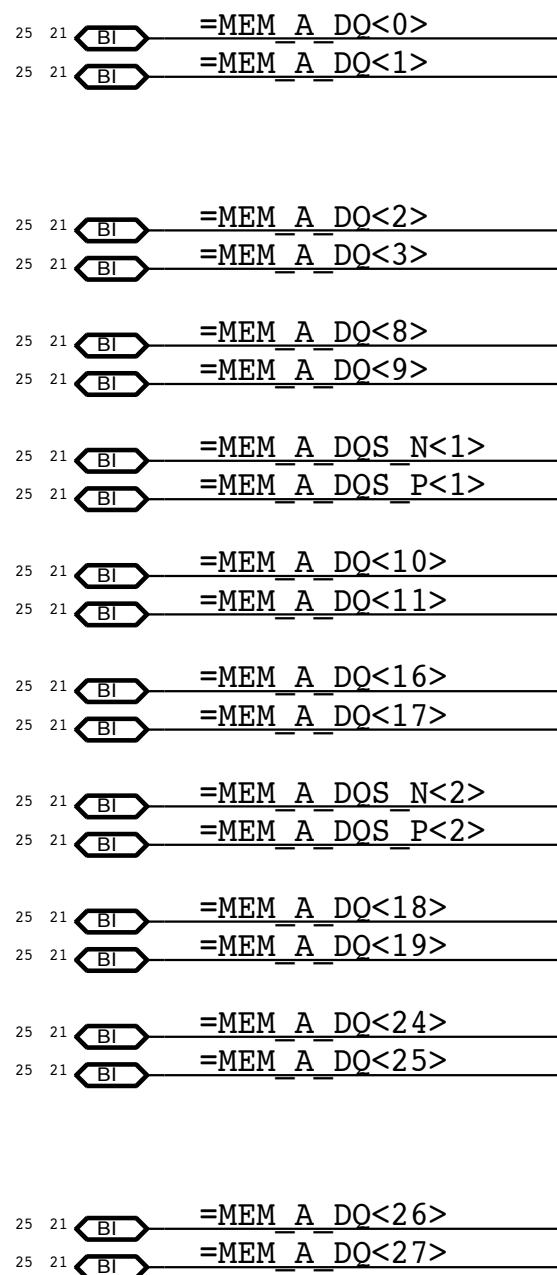
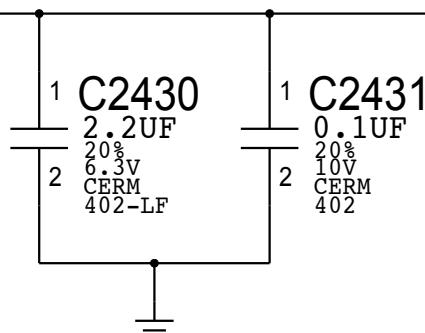
- =I2C_SODIMMA_SCL

- =I2C_SODIMMA_SDA

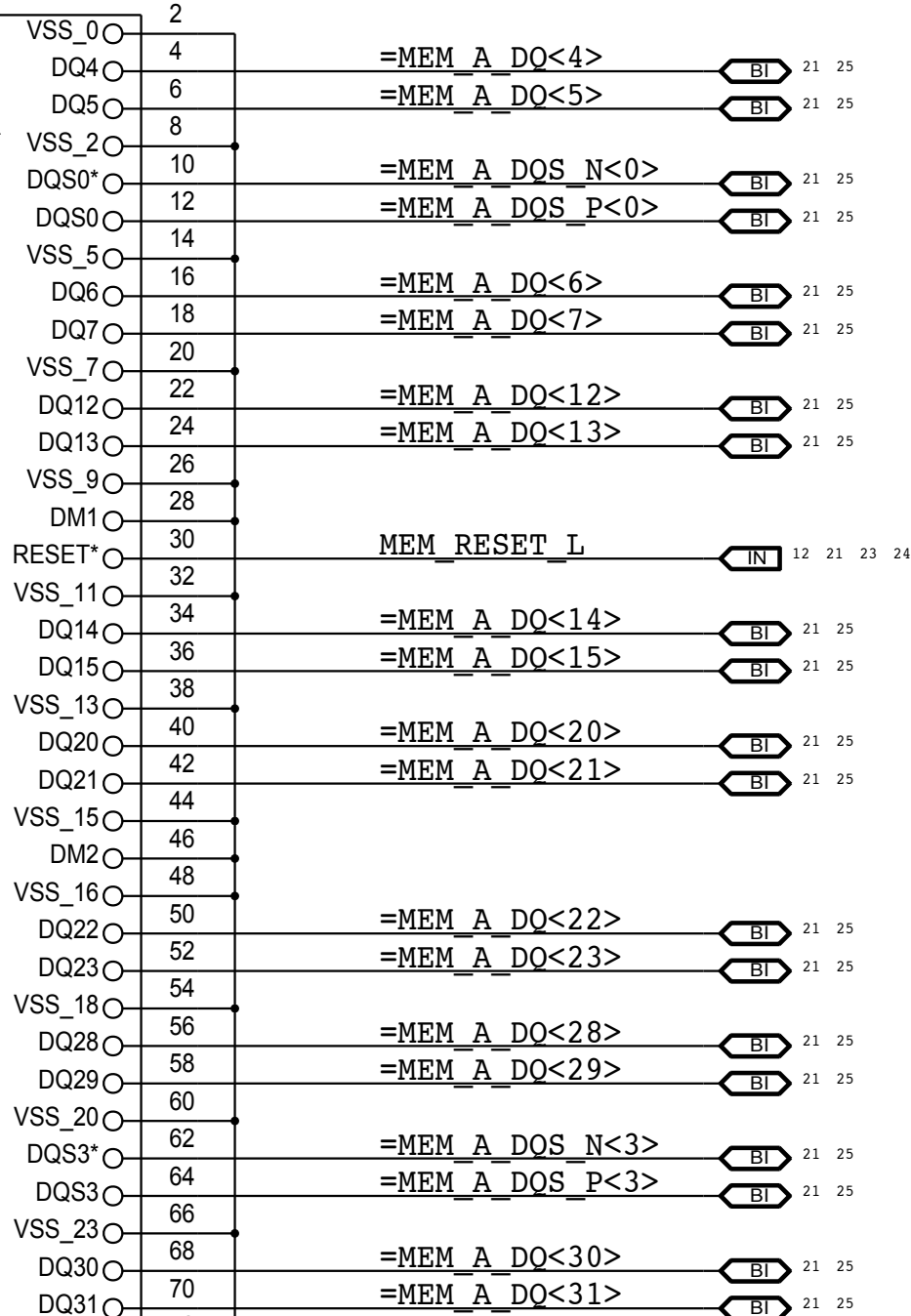
BOM options provided by this page:

(NONE)

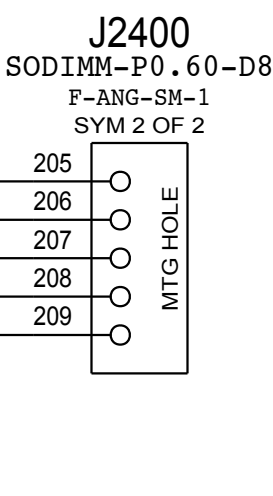
21 20 PPVREF_S3_MEM_VREFDQ_A



J2400
F-ANG-SM-1
SYM 1 OF 2

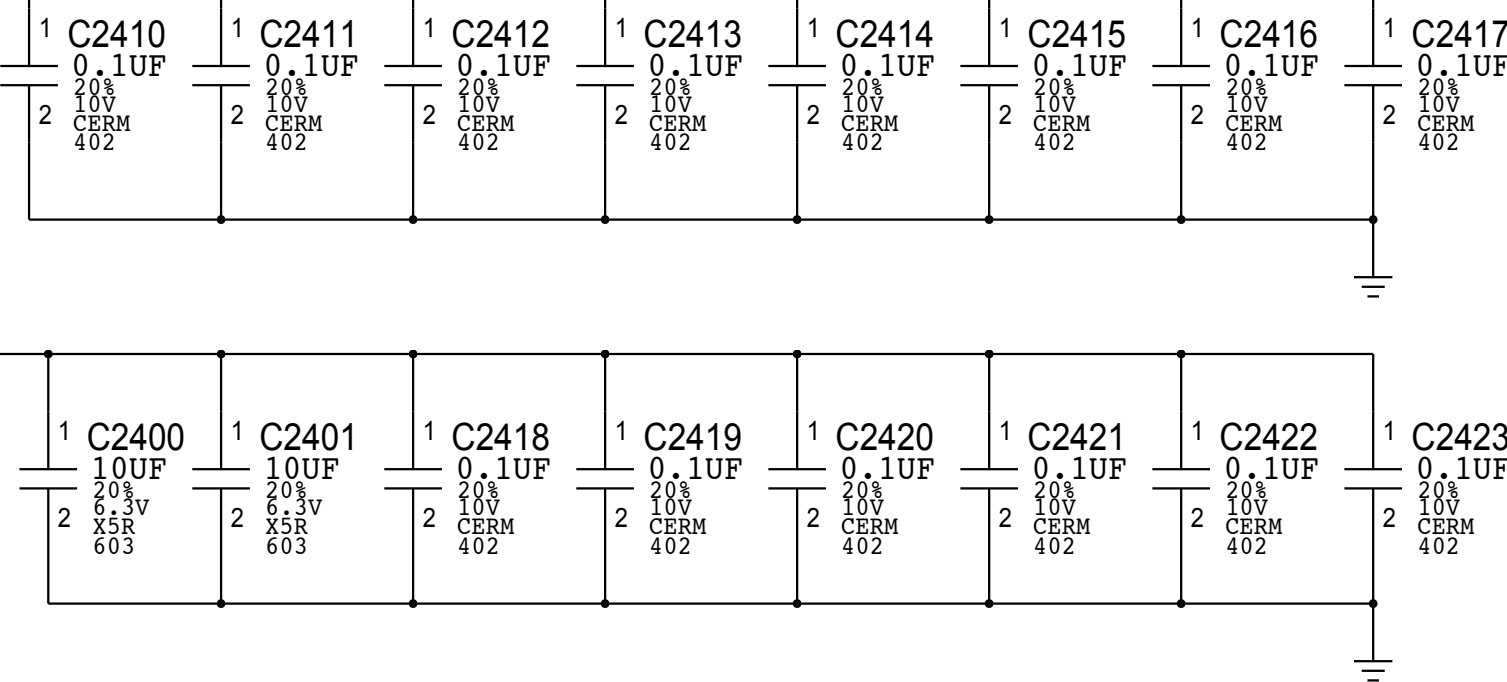


P/N: 516S1019

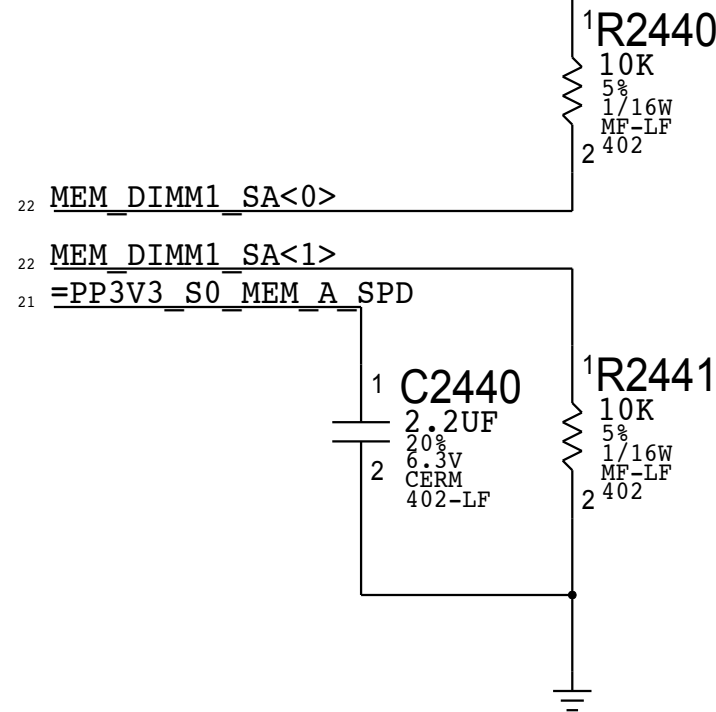


DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

89 22 21 =PPVDDQ_S3_MEM_A

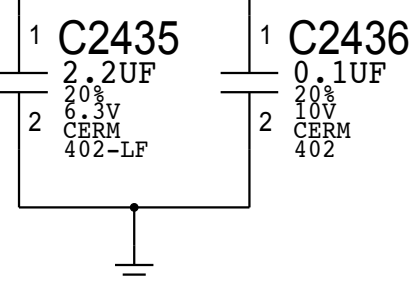


89 22 21 =PP3V3_S0_MEM_A_SPD

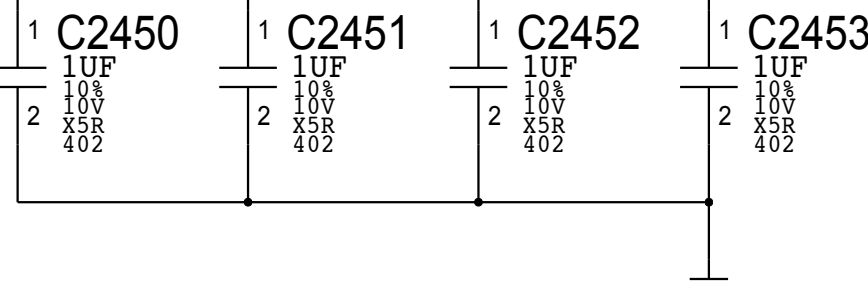


89 22 21 =PPDDRVTT_S0_MEM_A

20 21 23 24 PPVREF_S3_MEM_VREFCA




21 22 89 =PPDDRVTT_S0_MEM_A



SYNC_MASTER=J78_RAT

SYNC_DATE=10/30/2013

DRAM: SO-DIMM Connector A Slot1

 Apple Inc.

DRAWING NUMBER
051-00673

REVISION
0.24.0

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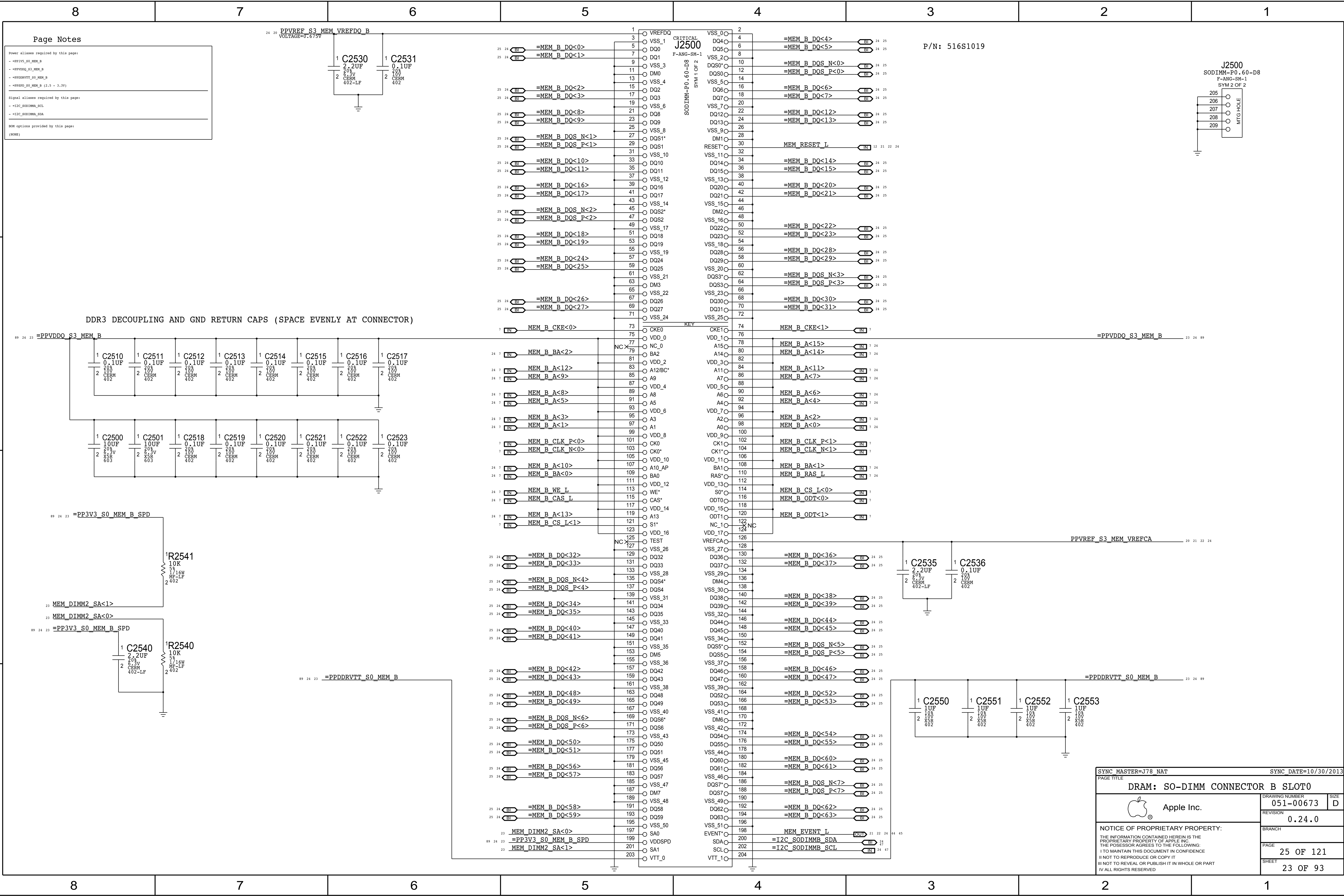
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Page Notes

Power aliases required by this page:

- *PP1V3_S0_MEM_B
- *PPVDDQ_S3_MEM_B
- *PPDDRVTT_S0_MEM_B
- *PPREF_S0_MEM_B (2.5 - 3.3V)

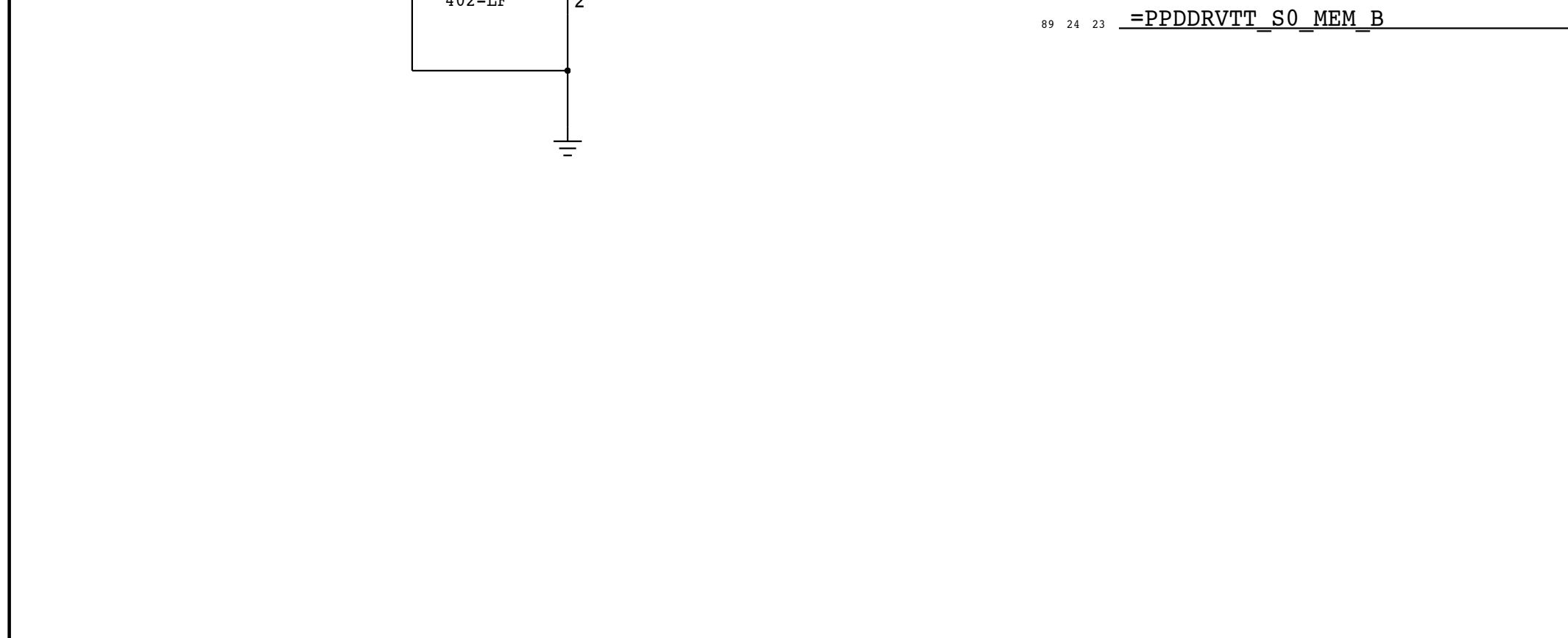
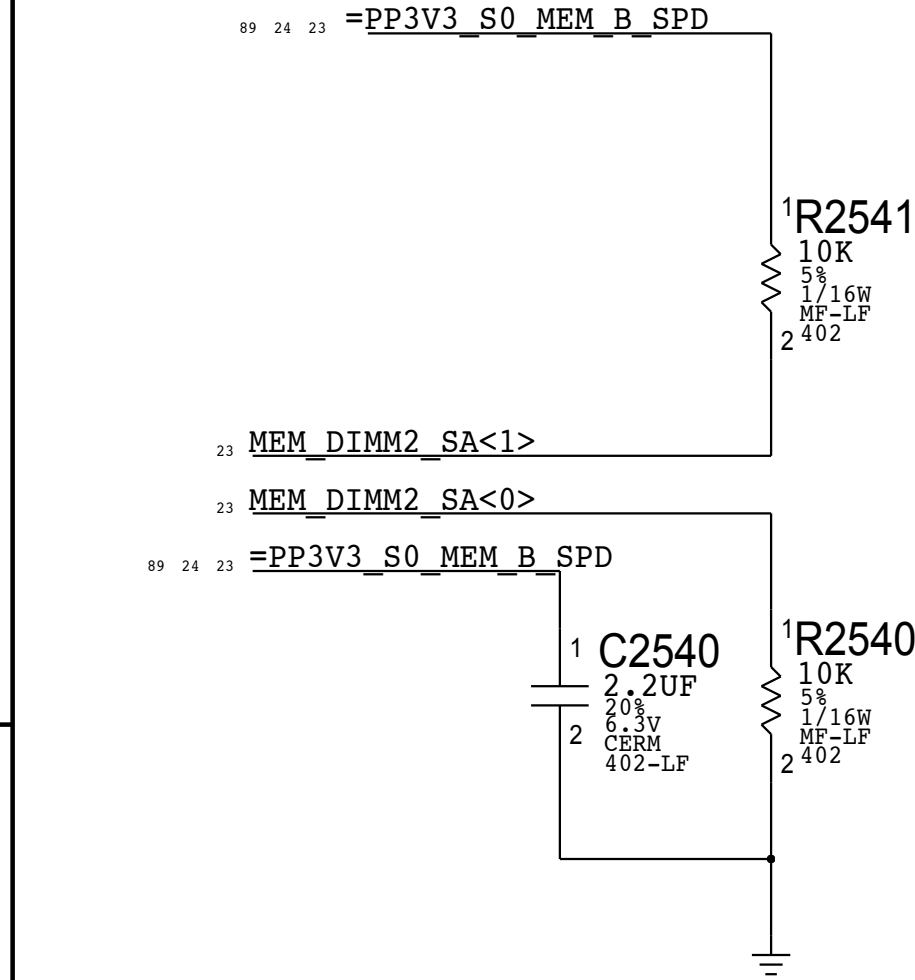
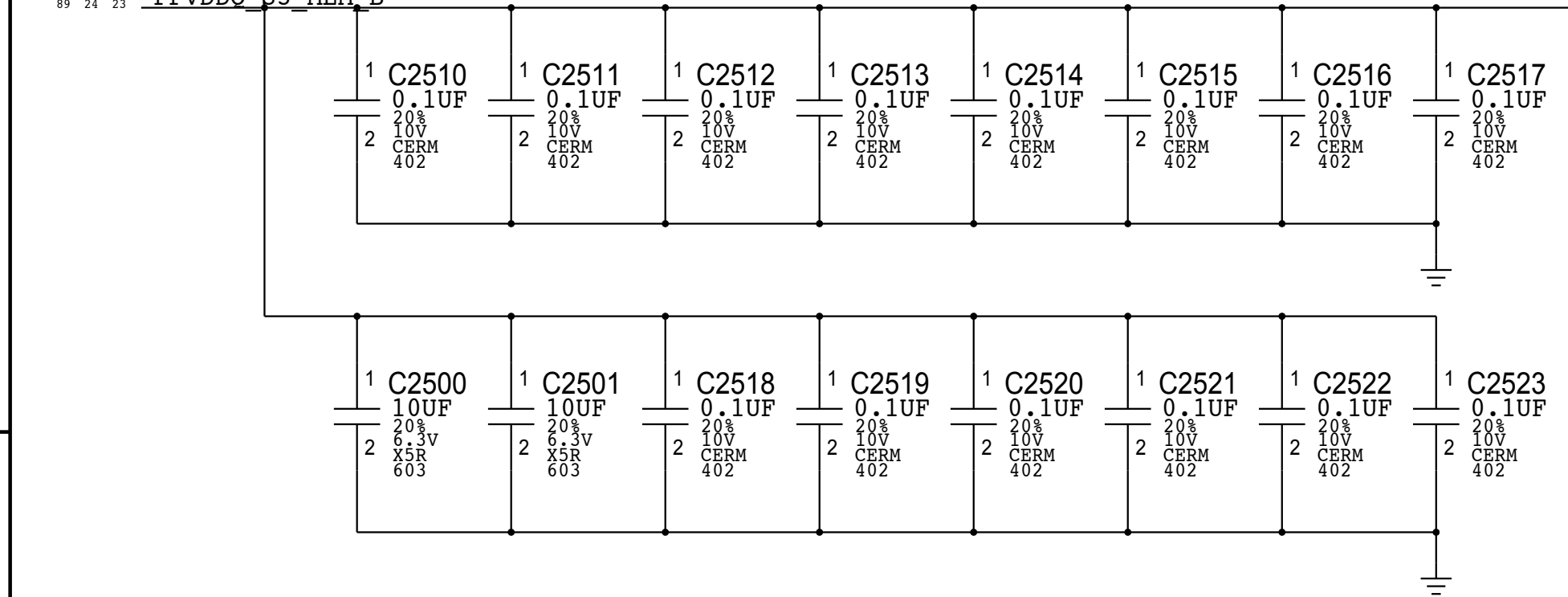
Signal aliases required by this page:

- *I2C_S0DIMM_A_SCL
- *I2C_S0DIMM_A_SDA

BOM options provided by this page:

(NONE)

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)



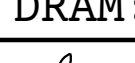
A

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SYNC_MASTER=J78 NAT		SYNC_DATE=10/30/2013	
PAGE TITLE			
DRAM: SO-DIMM CONNECTOR B SLOT0			
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		PAGE	25 OF 121
		SHEET	23 OF 93

Page Notes

Power aliases required by this page:

- =PP1V5_S0_MEM_B

- =PPVDDQ_S3_MEM_B

- =PPDD&VT?_SO_NEW_

FFSPD_30_AEA_B (

Signal aliases required by this page:

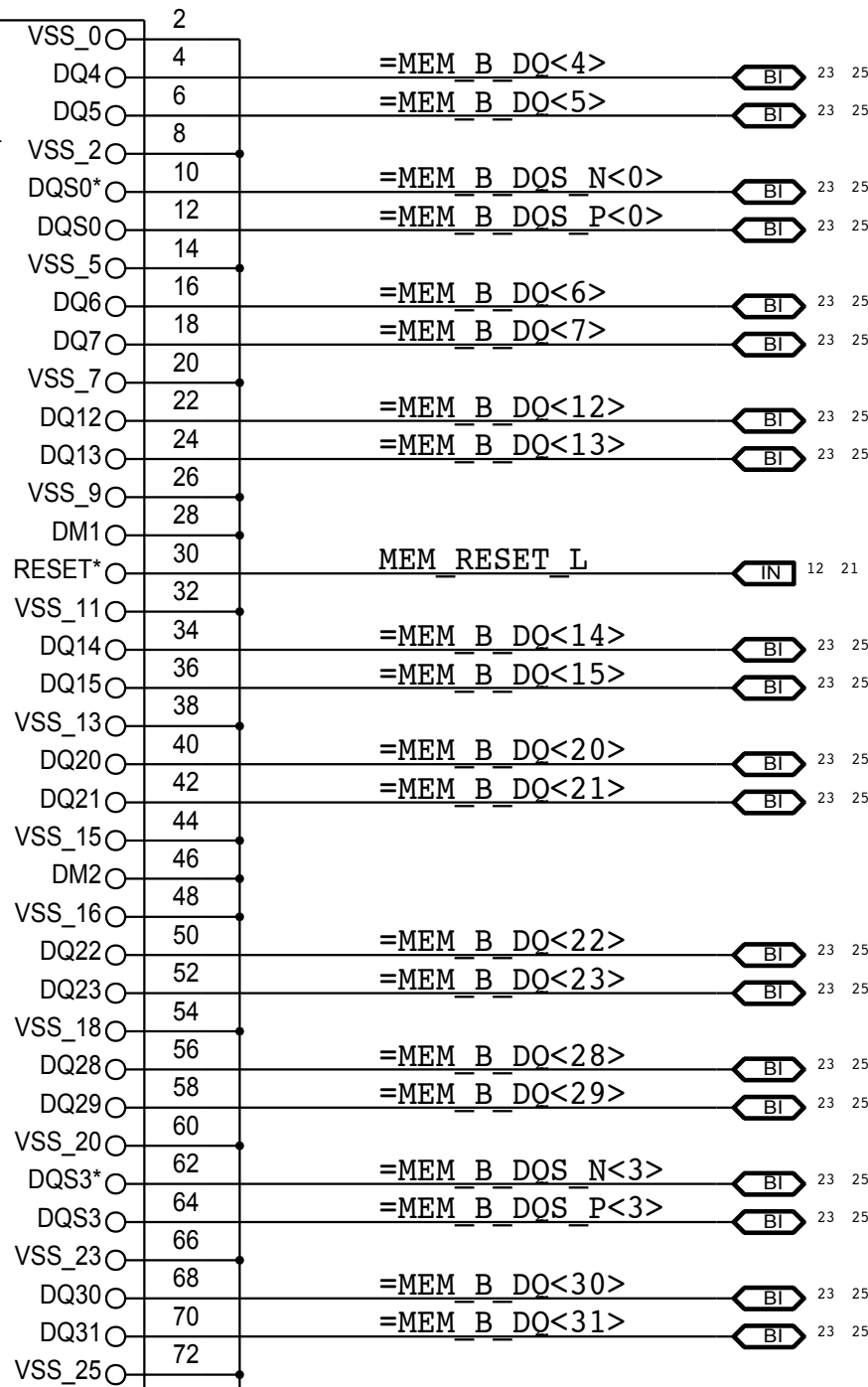
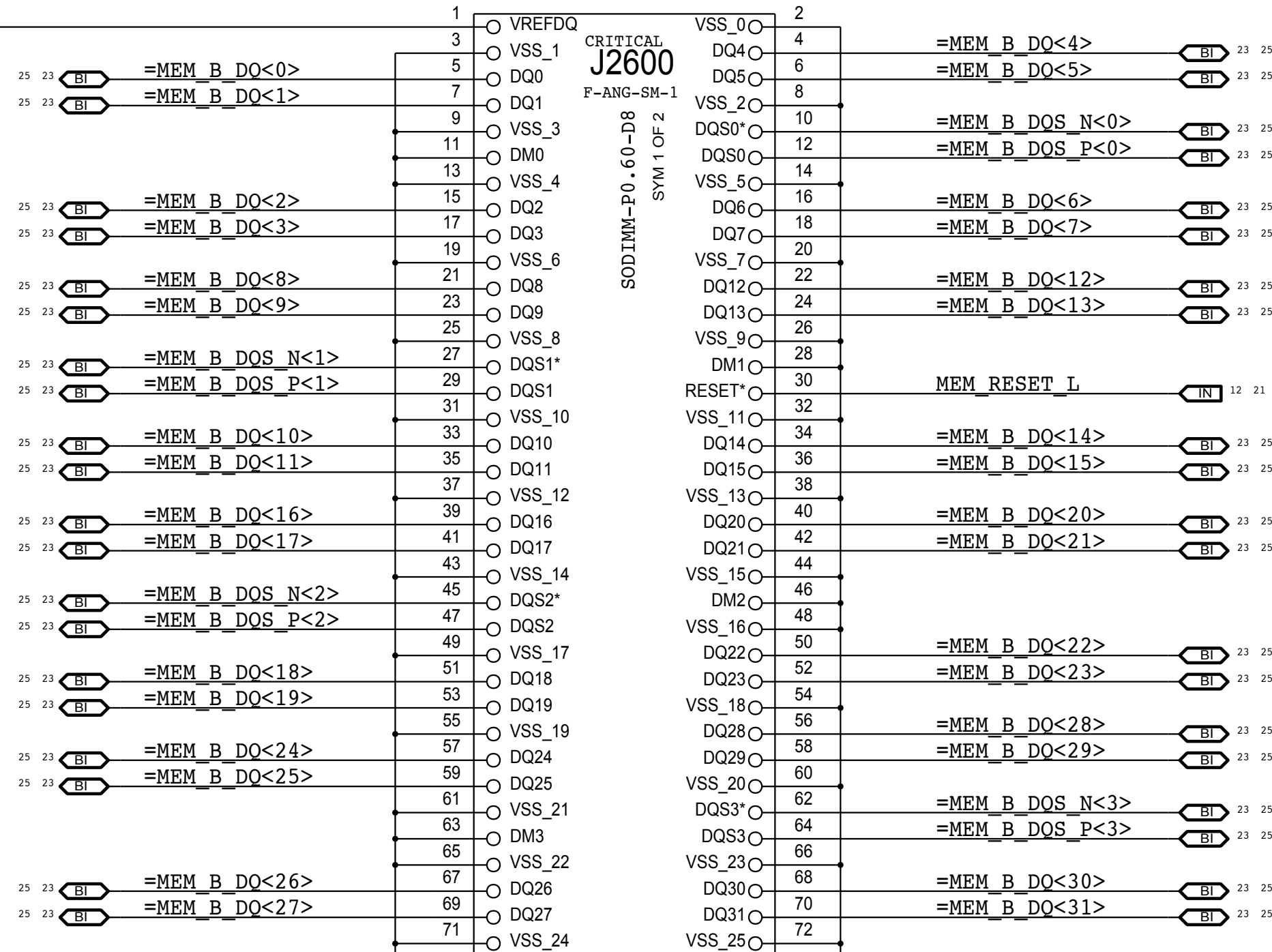
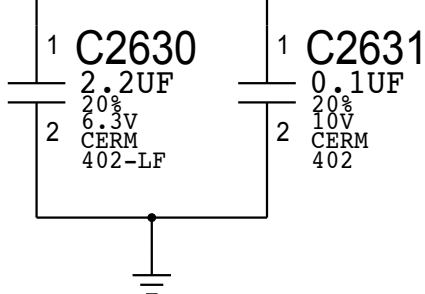
```
- #I2C_SODINMA_SCL
```

- =I2C_SODIMMA_SDA

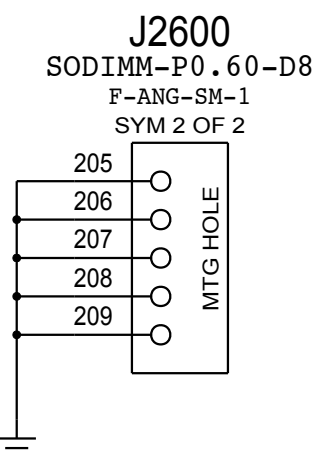
BOM options provided by this page:

(NONE)

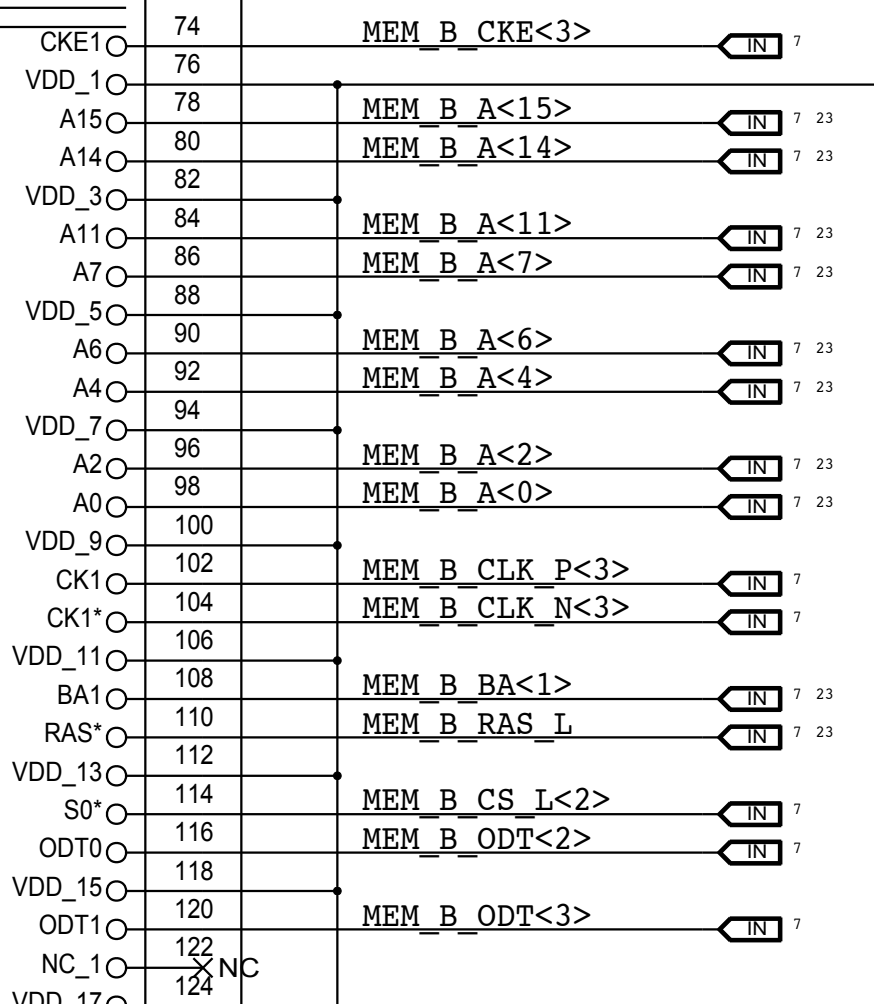
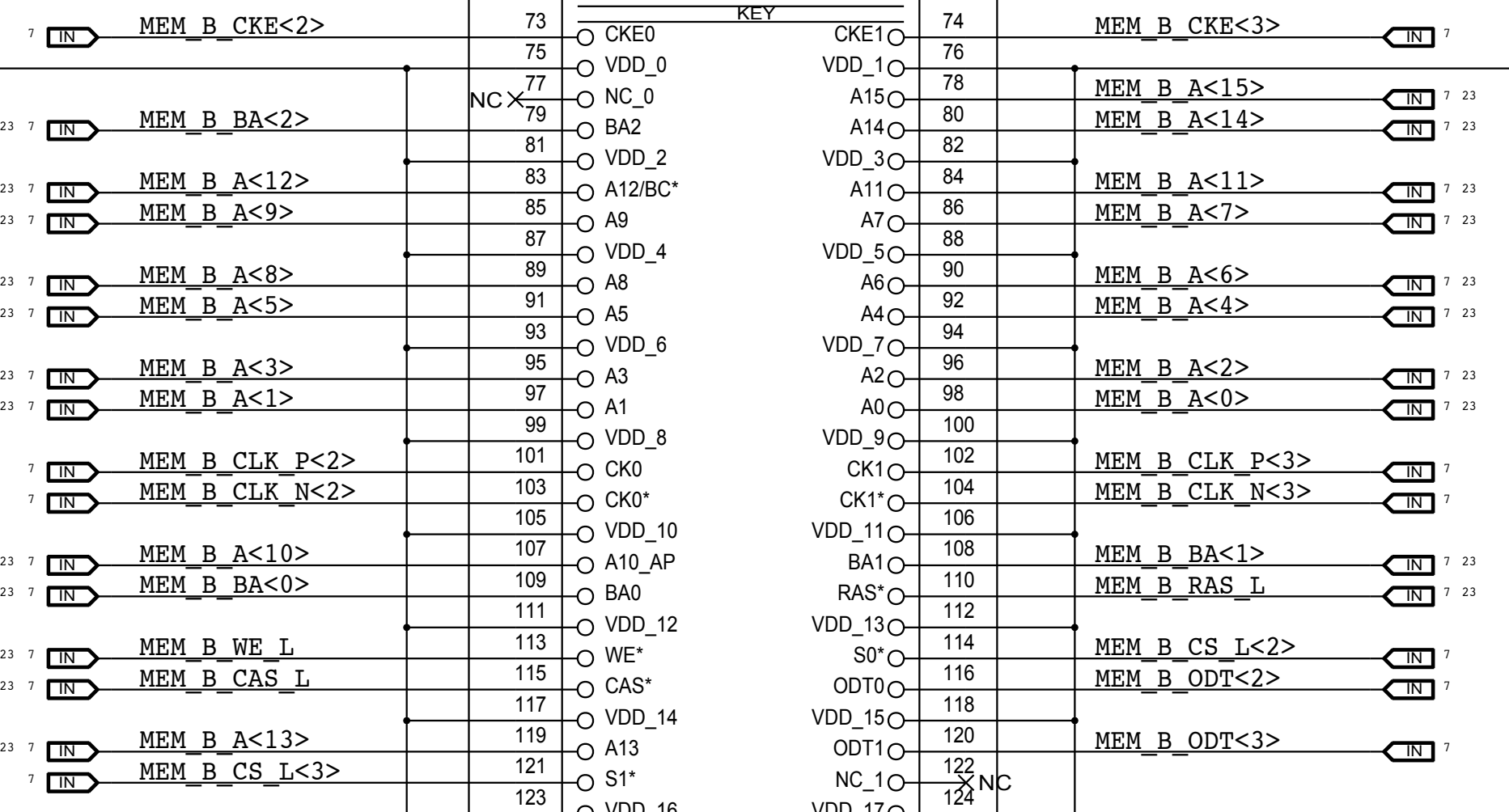
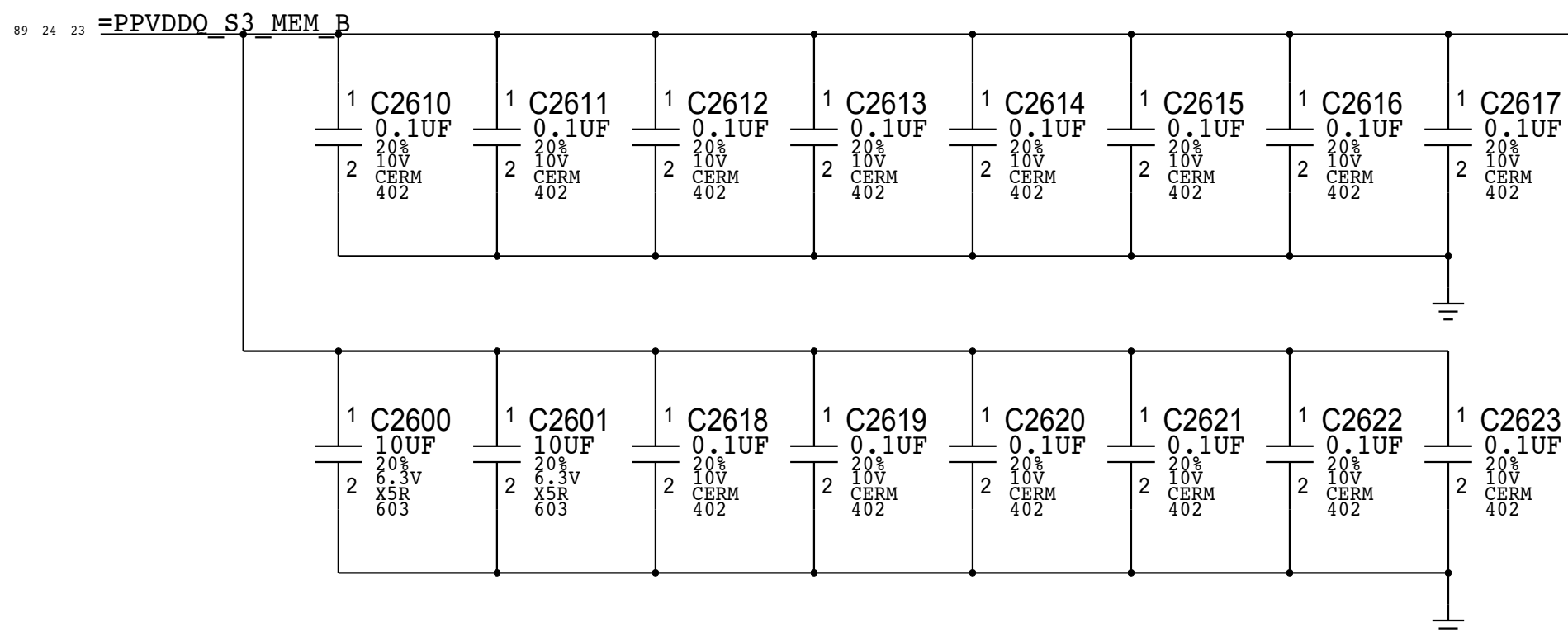
23 20 PPVREF S3 MEM VREFDQ B
VOLTAGE=0.675V



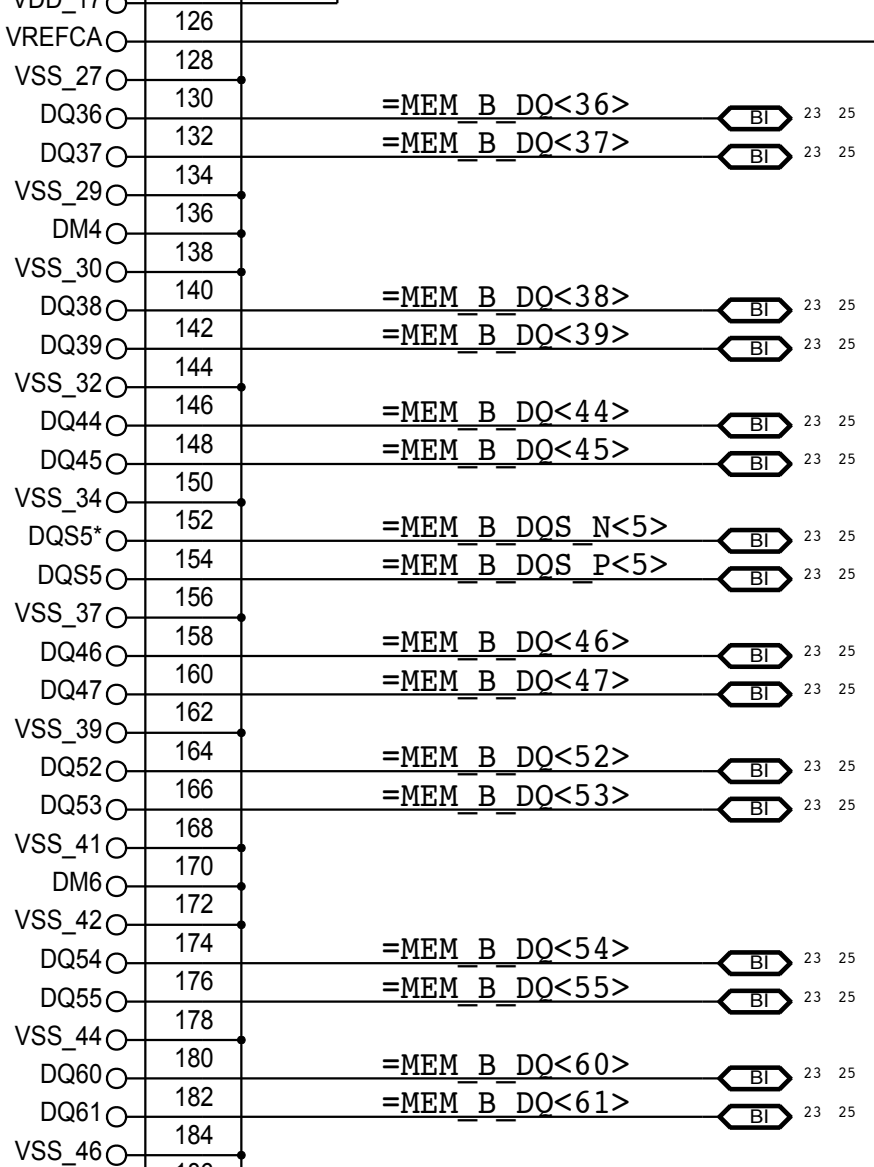
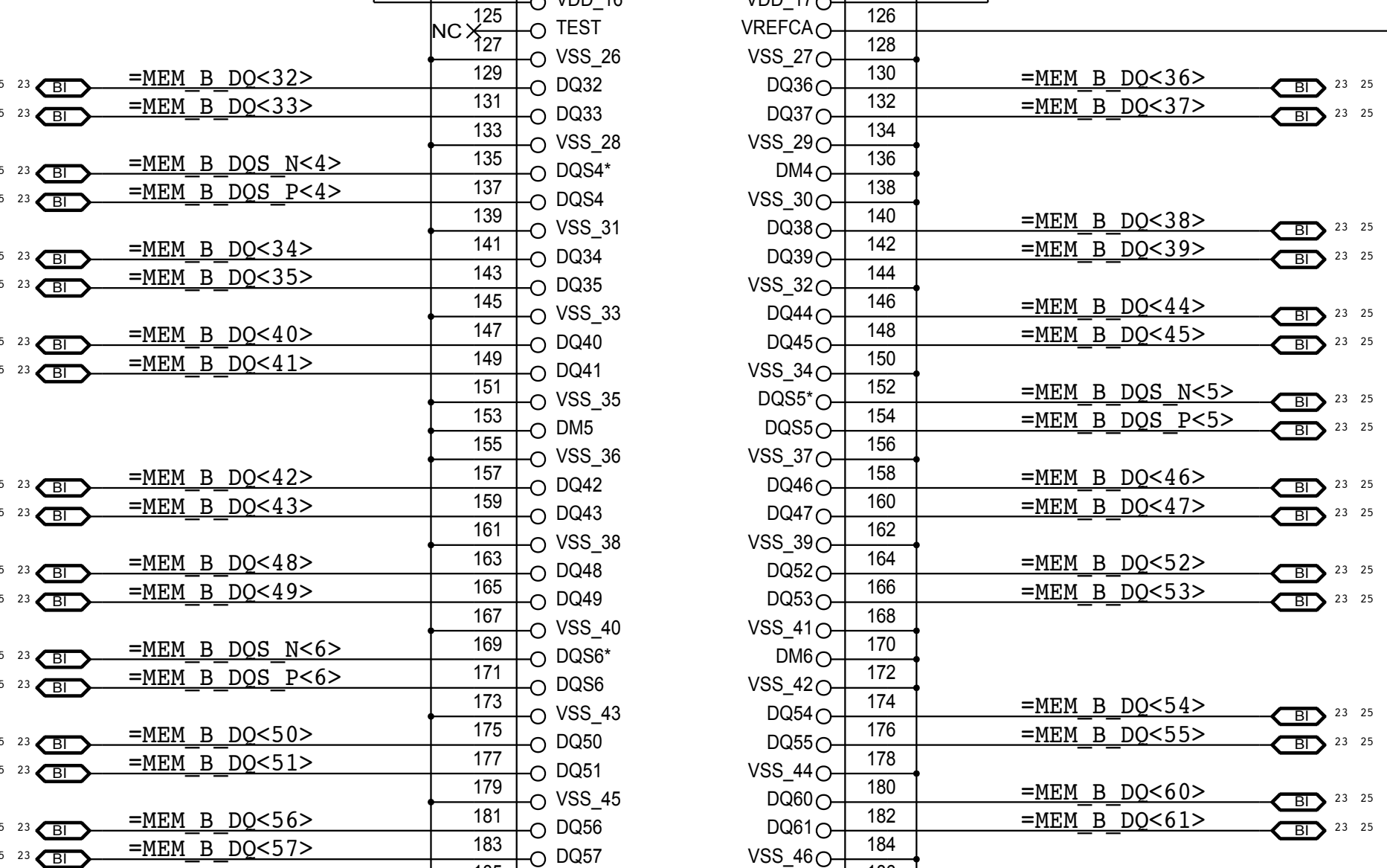
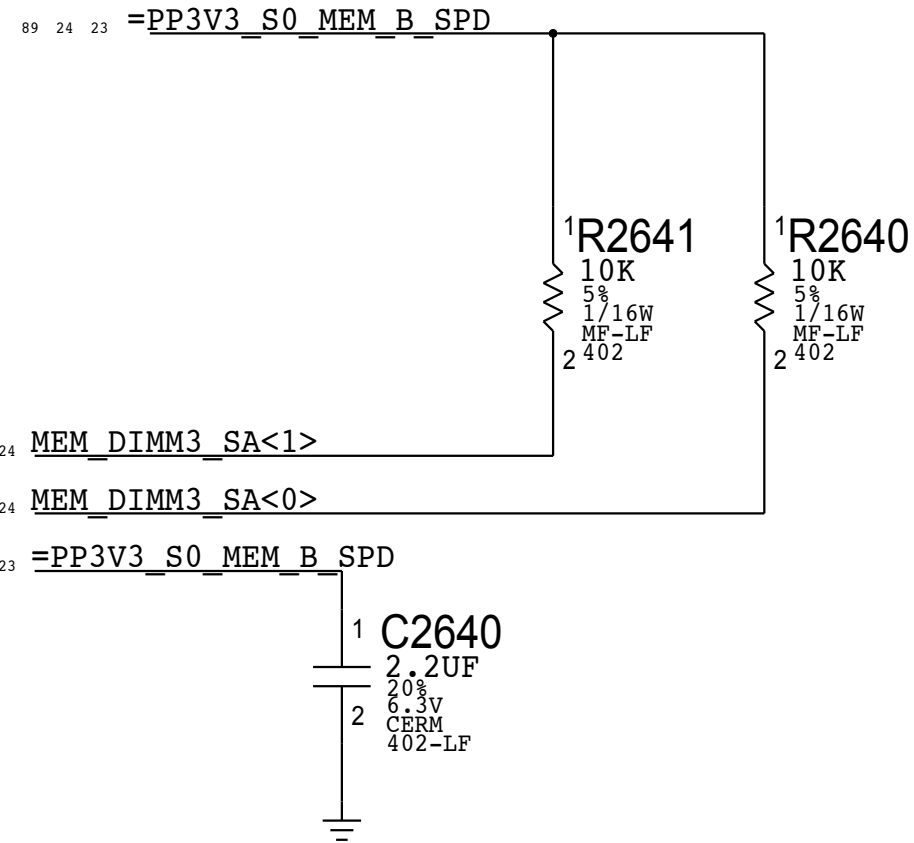
P/N: 516S1019



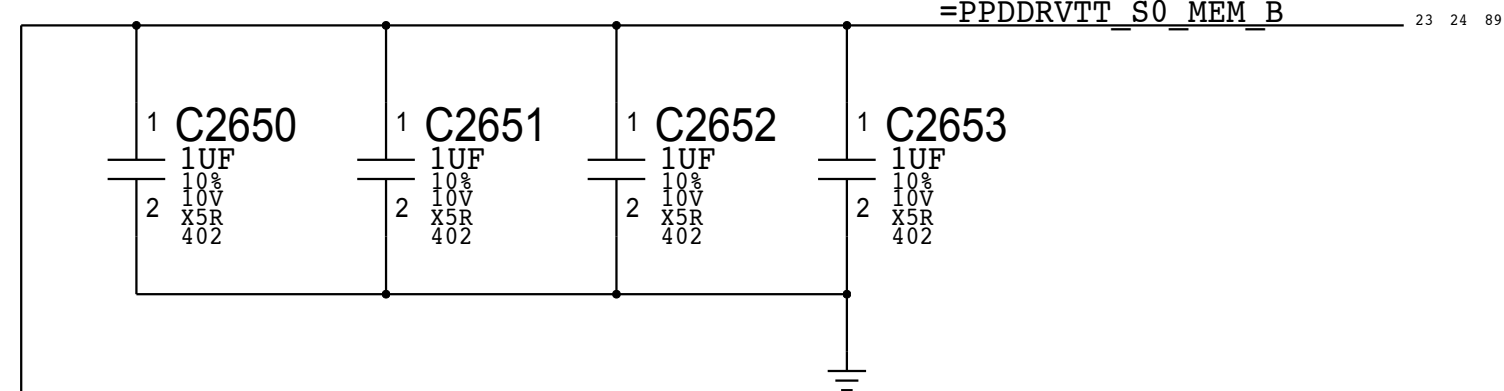
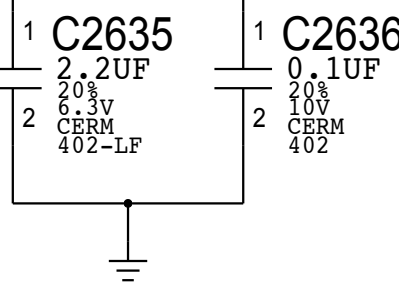
DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

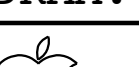


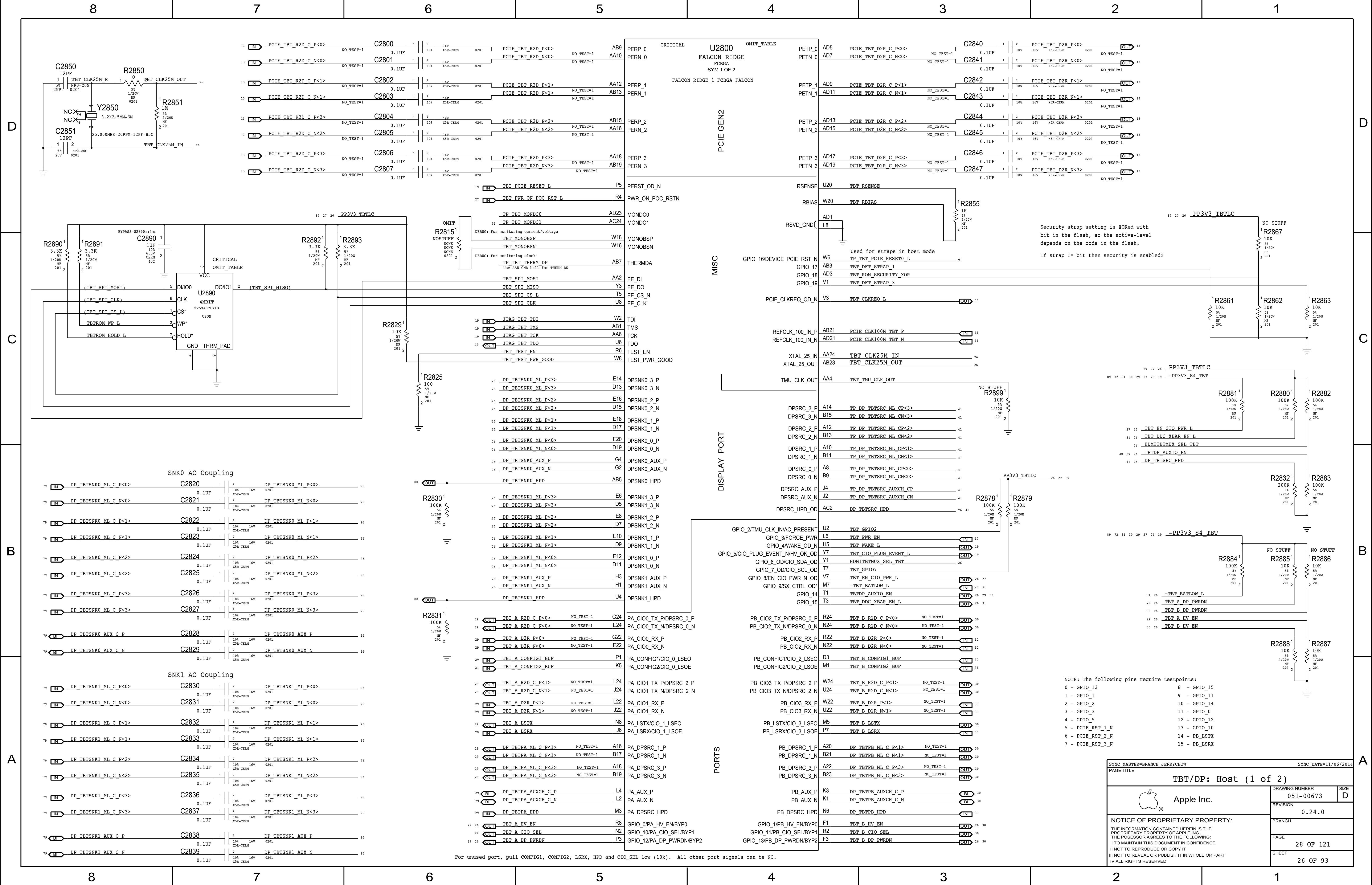
=PPVDDQ S3 MEM B 23 24 89

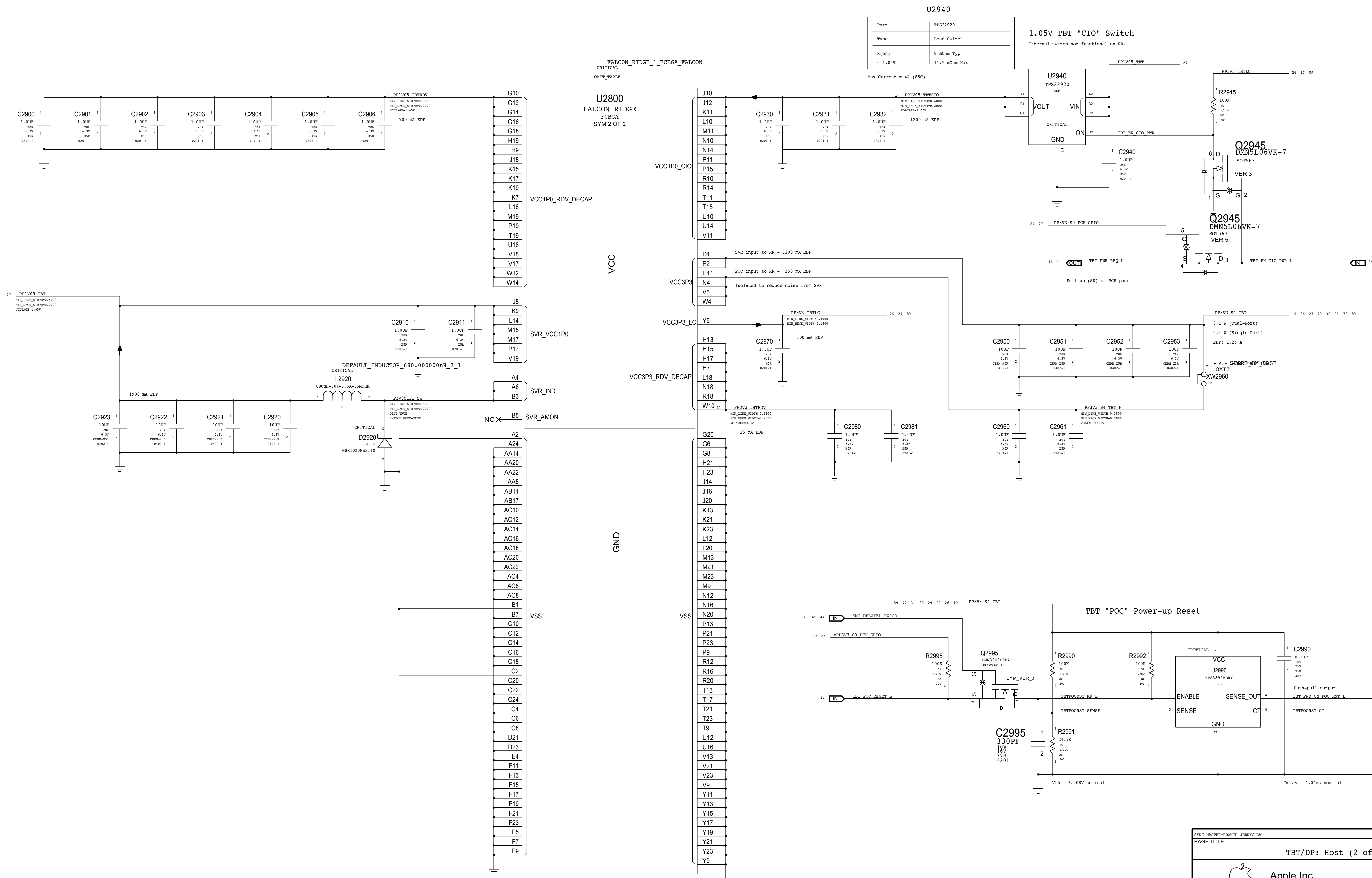


PPVREF	S3	MEM	VREFCA	20	21	22	23
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SYNC MASTER=J78 NAT		SYNC DATE=10/30/2013	
PAGE TITLE			
DRAM: SO-DIMM CONNECTOR B SLOT1			
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EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).

8		7		6		5		4		3		2		1	
D	<div>Page Notes</div> <div>Power aliases required by this page: - =PPVIN_SW_TBTBST (8-13V Boost Input) - =PP15V_TBT_REG (15V Boost Output) - =PP3V3_TBT_P3V3TBTFFET (3.3V FET Input) - =PP3V3_TBT_FET (3.3V FET Output) - =PP3V3_S0_TBTPWRCTL - =PP1V05_TBT_P1V05TBTFFET (1.05V FET Input) - =PP1V05_TBT_FET (1.05V FET Output)</div> <div>Signal aliases required by this page: - =TBT_CLKREQ_L - =TBT_RESET_L</div> <div>BOM options provided by this page: TBTBST:Y - Stuffs 15V boost circuitry.</div>														D
C		C		C		C		C		C		C		C	
B		B		B		B		B		B		B		B	
A		A		A		A		A		A		A		A	
8		7		6		5		4		3		2		1	

SYNC_MASTER=J78_JERRY			SYNC_DATE=10/09/2013		
PAGE TITLE			Thunderbolt: Power Support		
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		BRANCH			
		PAGE		30 OF 121	
		SHEET		28 OF 93	

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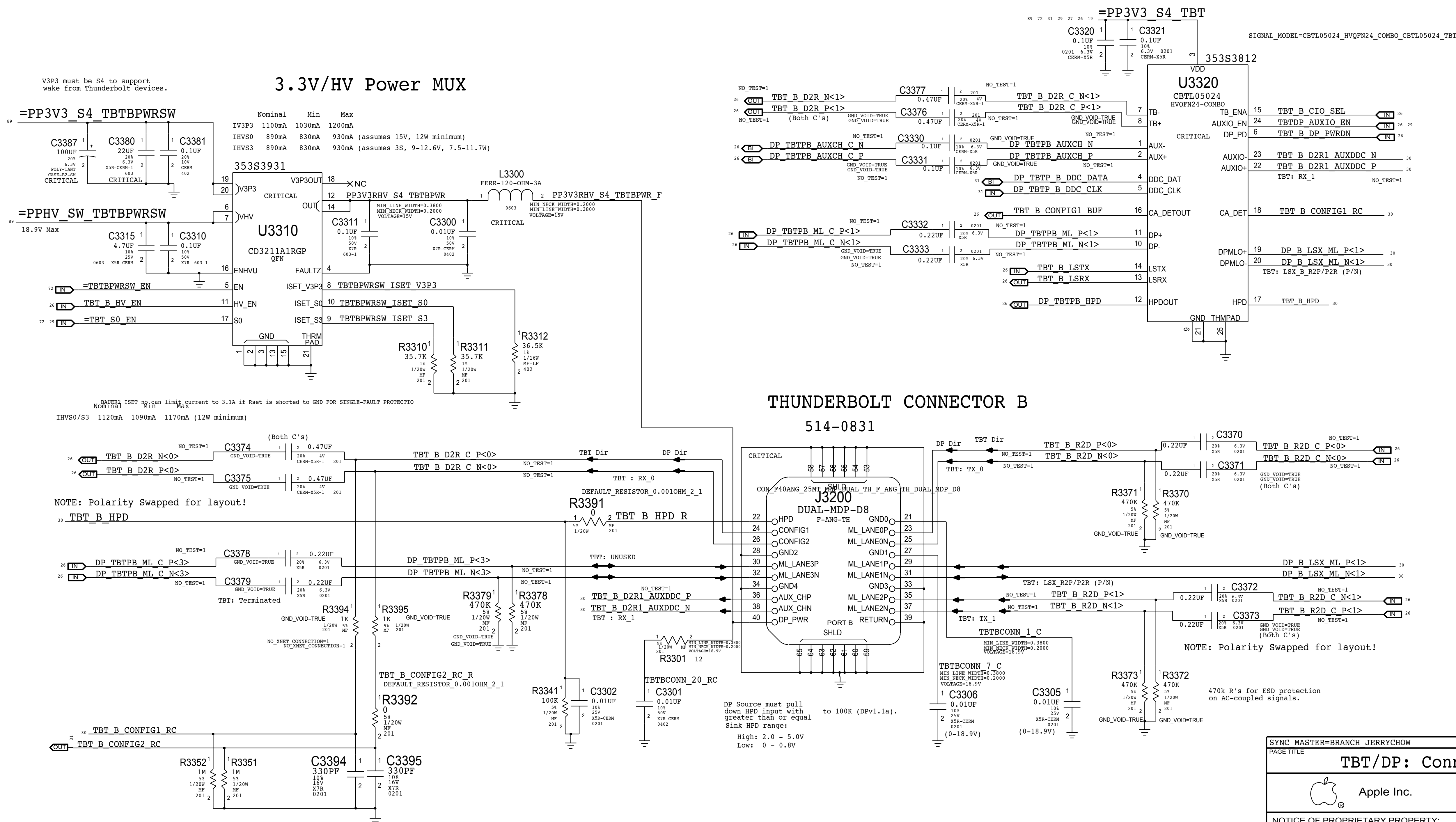
A


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SYNC MASTER=BRANCH JERRYCHOW		SYNC DATE=09/10/2014	
PAGE TITLE			
TBT/DP: Connector B			
	Apple Inc.	DRAWING NUMBER	
		051-00673	
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	0.24.0		D
		BRANCH	
		PAGE	33 OF 121
		SHEET	30 OF 93

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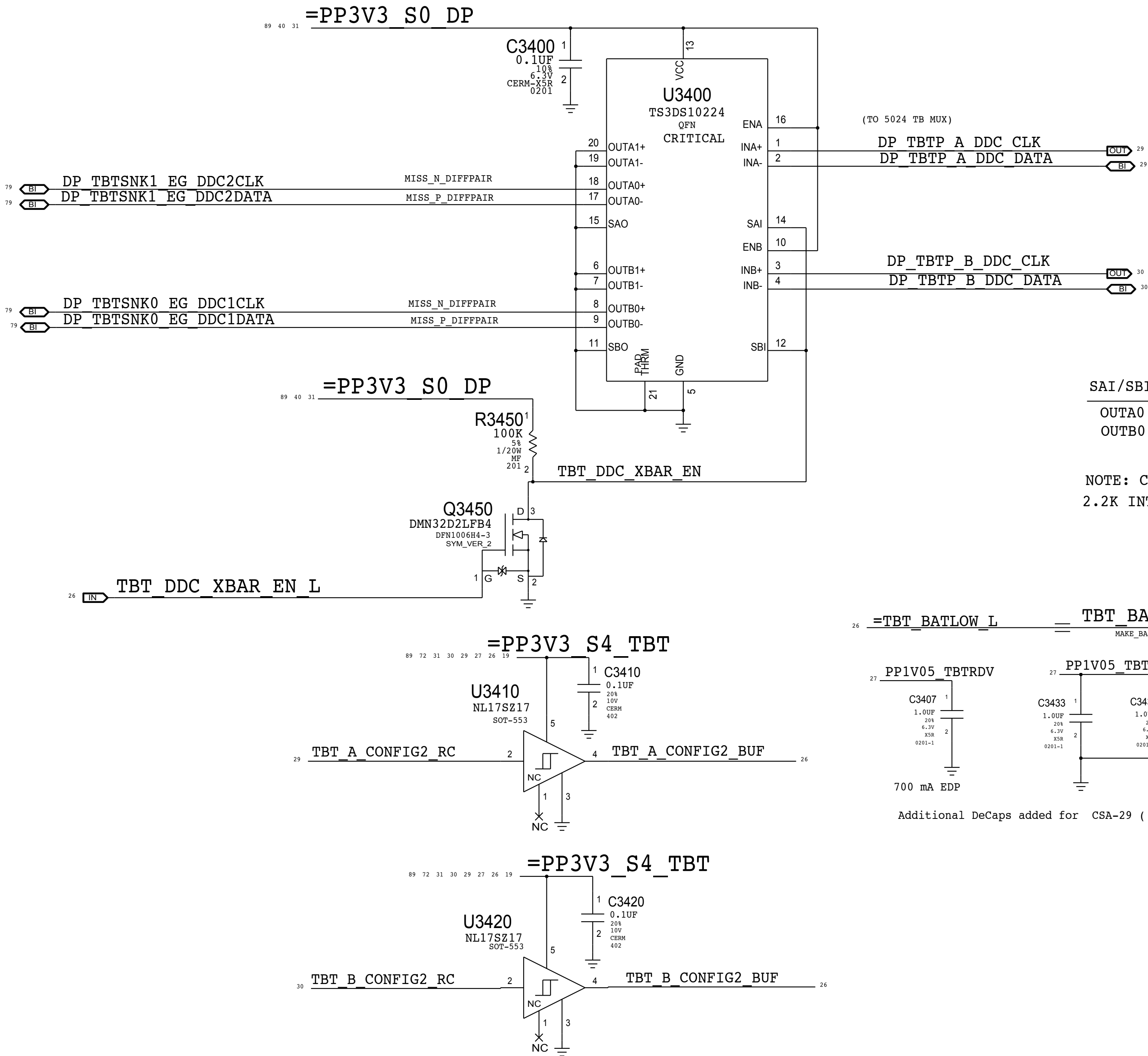
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Dual-Port Host DDC Crossbar



SAI/SBI =	0	1
OUTA0 =	INB	INA
OUTB0 =	INA	INB

NOTE: CABLE ADAPTERS ARE REQUIRED TO HAVE 2.2K INTERNAL PULL-UPS.

SYNC_MASTER=BRANCH JERRYCHOW		SYNC_DATE=11/05/2014	
PAGE TITLE			
TBT/DP: DDC Crossbar			
	Apple Inc.	DRAWING NUMBER	051-00673
		SIZE	D
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		PAGE	34 OF 121
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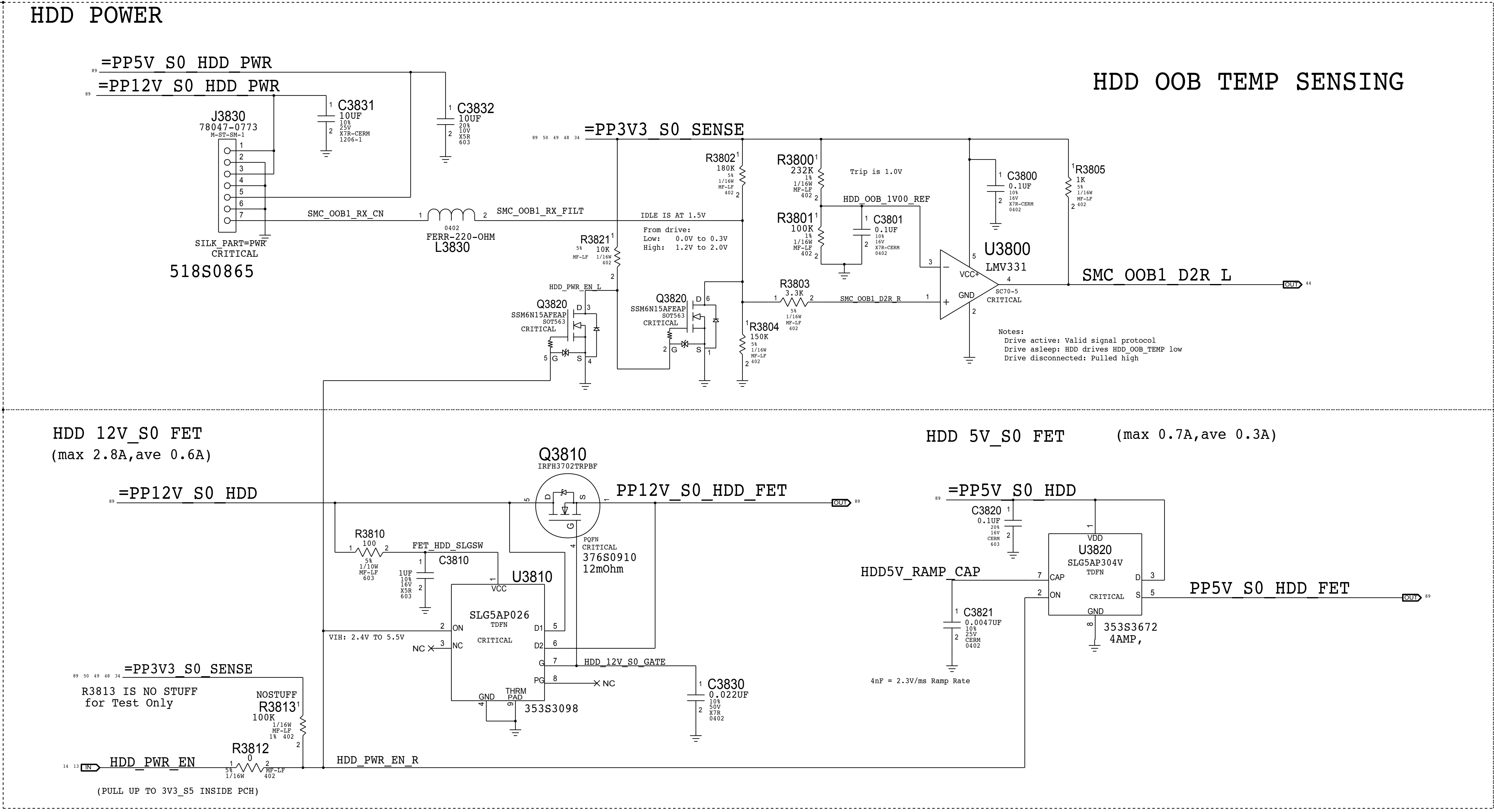
A


D

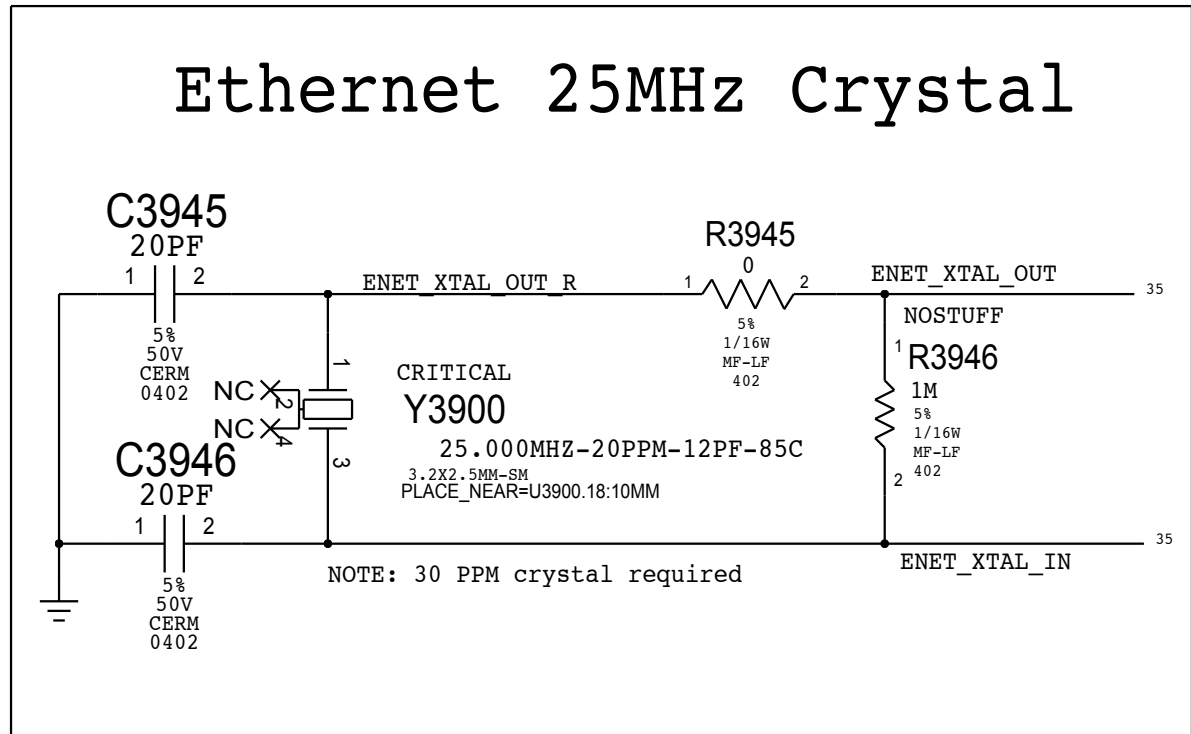
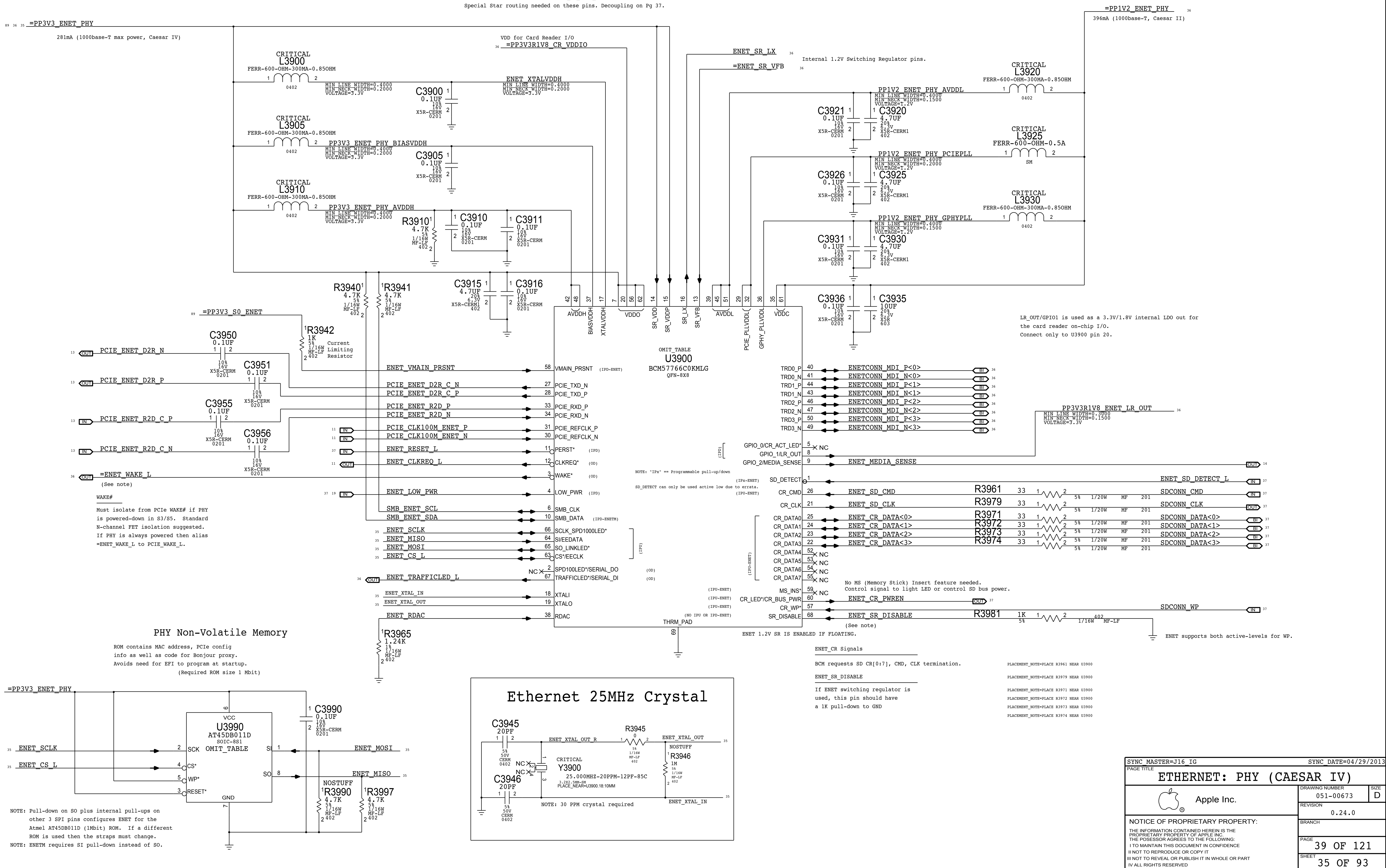
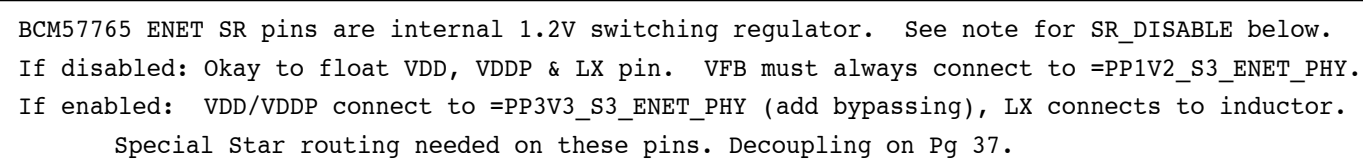
C

B

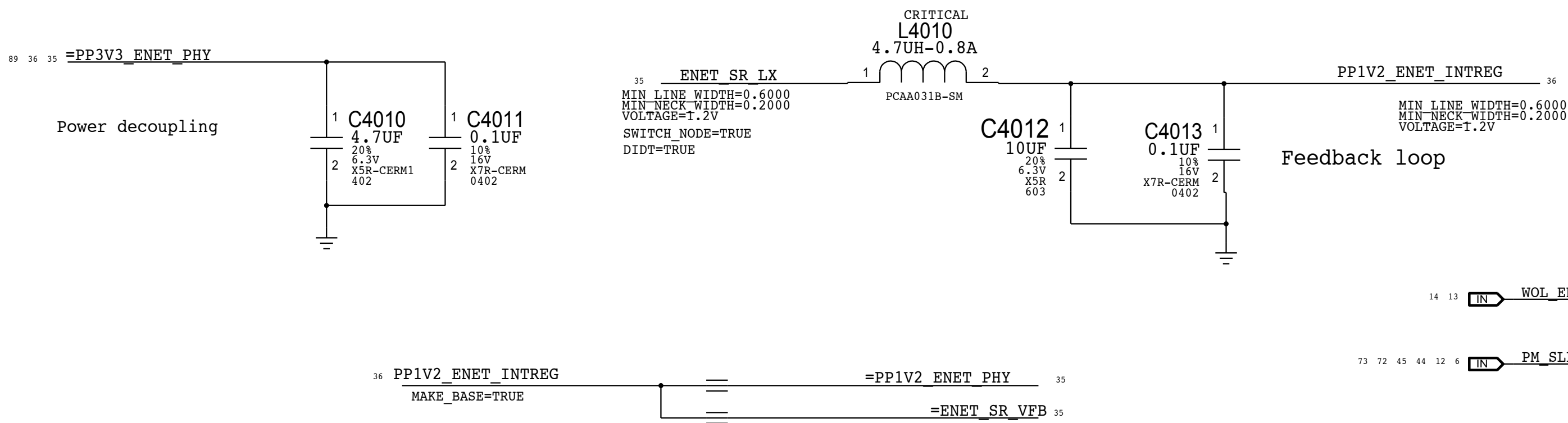
A



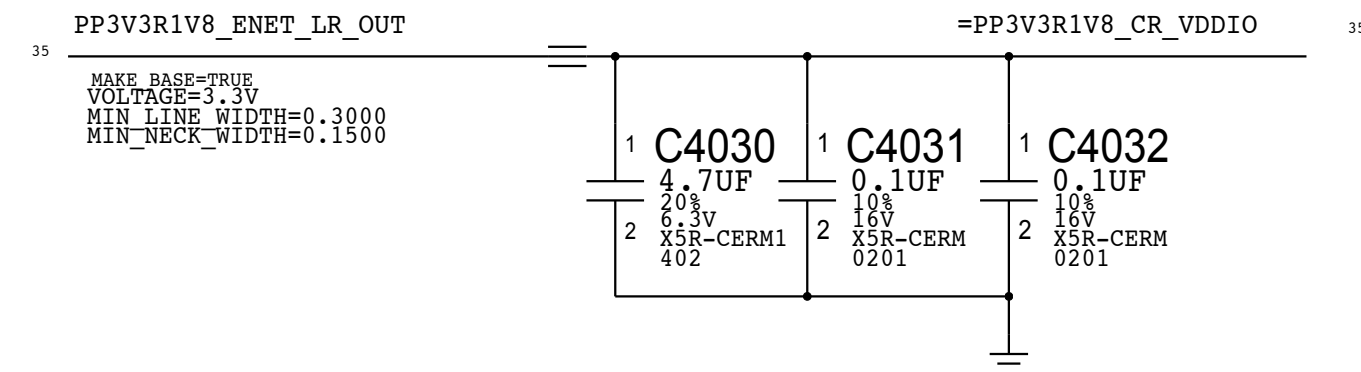
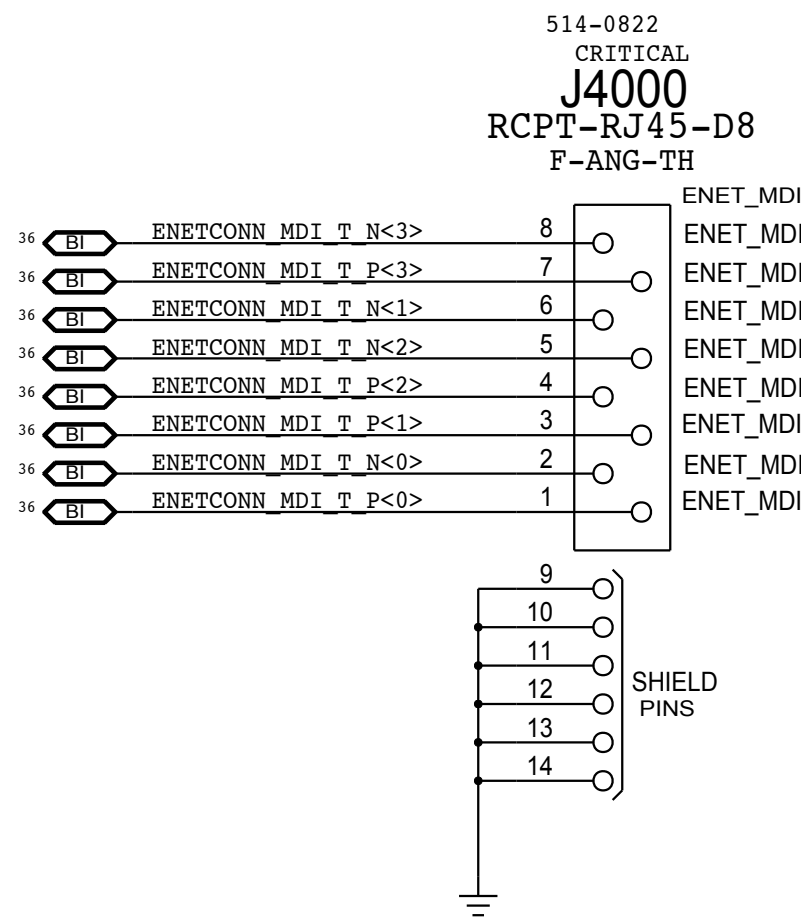
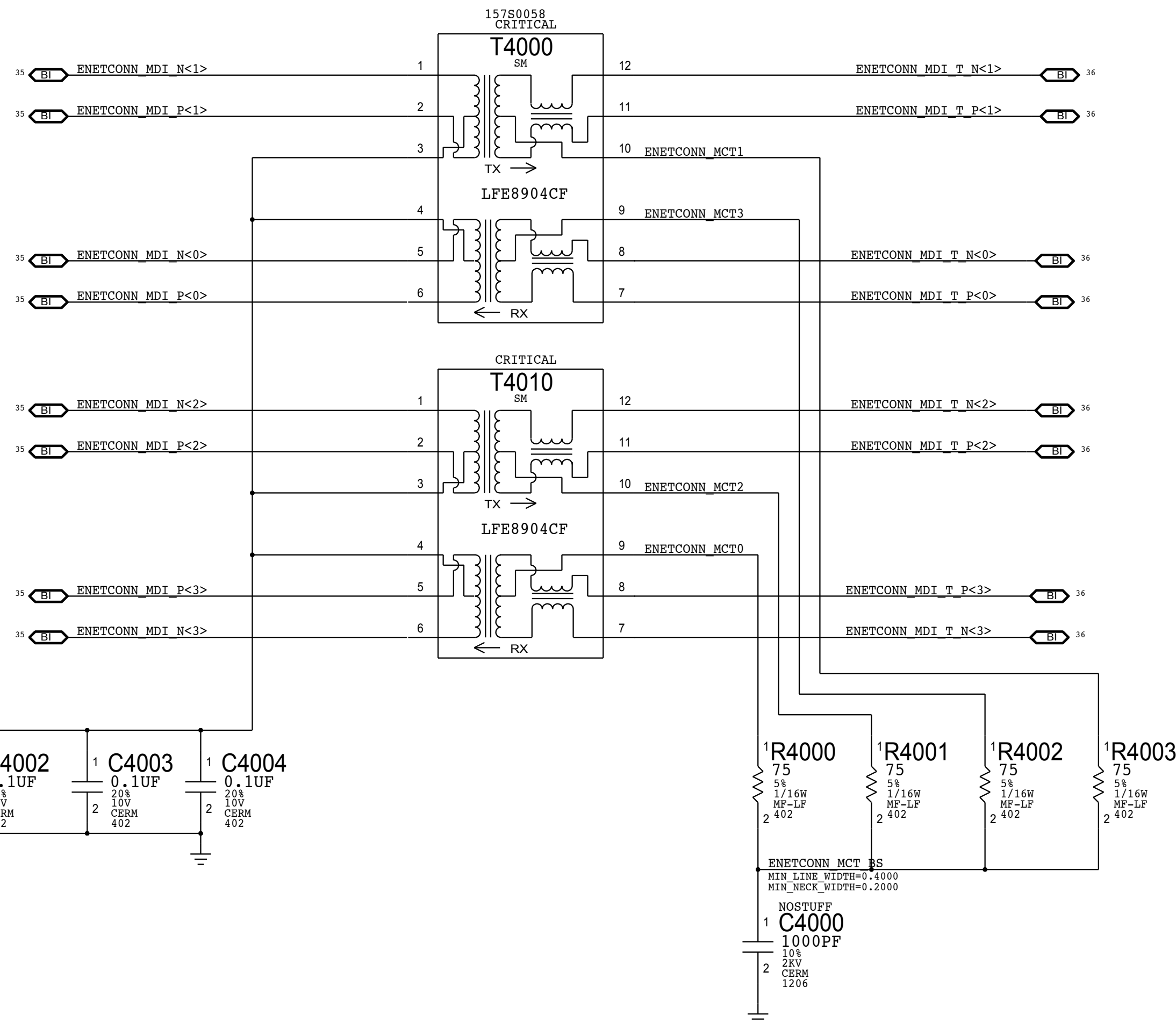
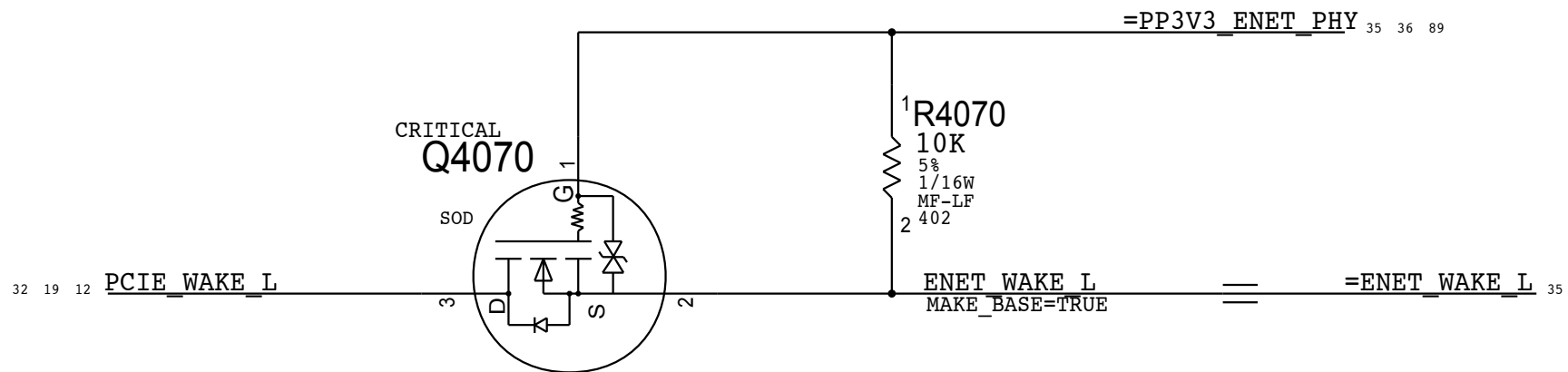
SYNC_MASTER=J78 KENNY		SYNC_DATE=03/10/2014	
PAGE TITLE			
HDD: SSD Temp Sense			
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CAESAR IV 1.2V INT.VR CMPTS



CAESAR IV WAKE# ISOLATION



SYNC MASTER=J16 IG		SYNC DATE=12/07/2012	
PAGE TITLE			
ETHERNET: Support & Connector			
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		SIZE	D
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		BRANCH	
		PAGE	40 OF 121
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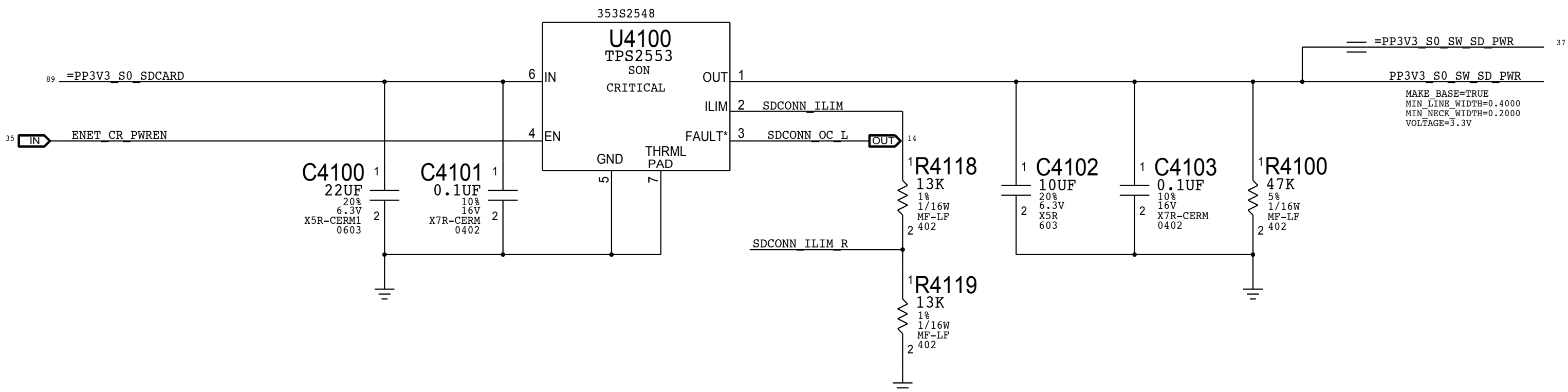
D

C

B

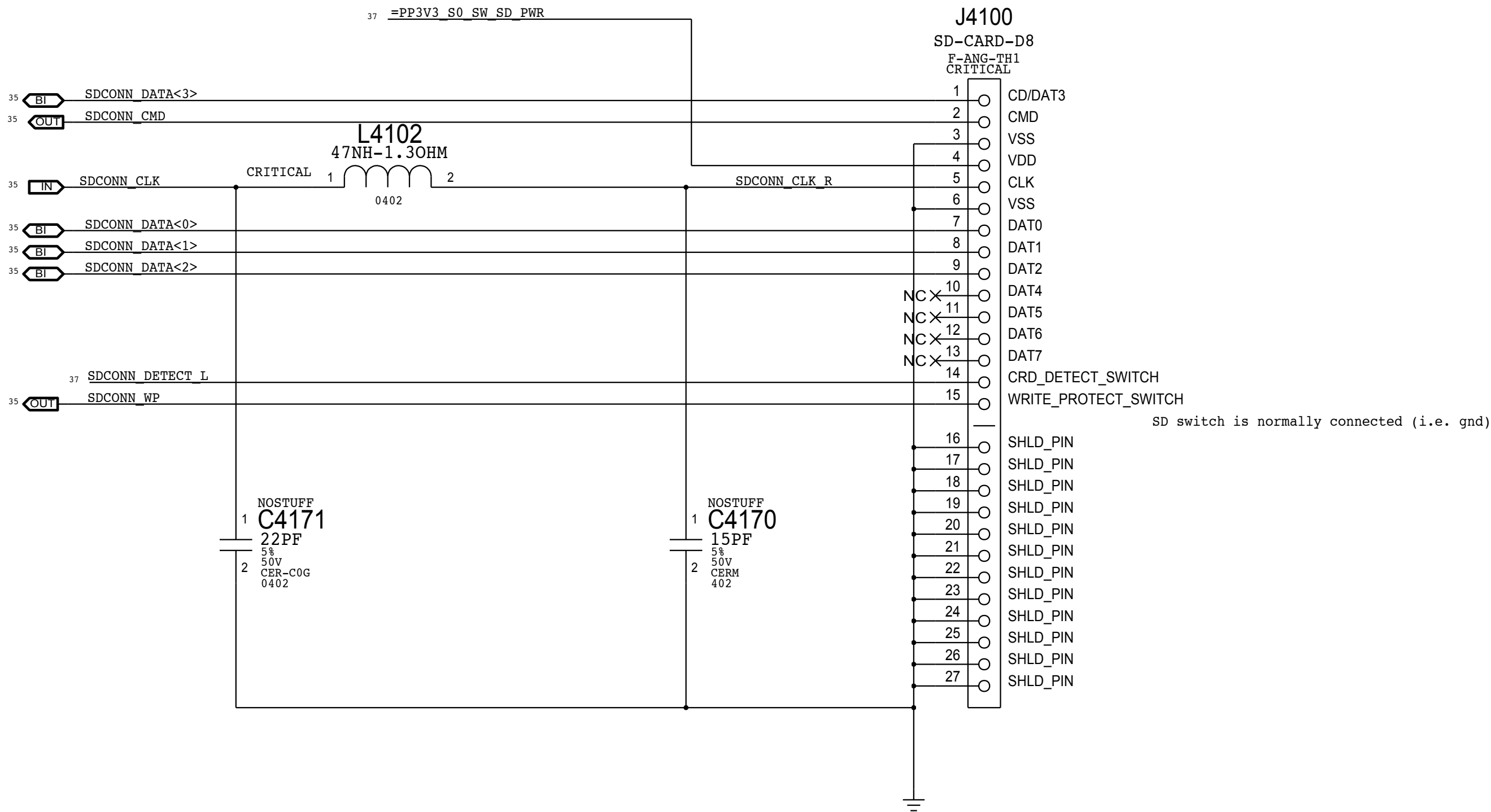
A

SD CARD 3.3V OVERCURRENT PROTECTION CHIP

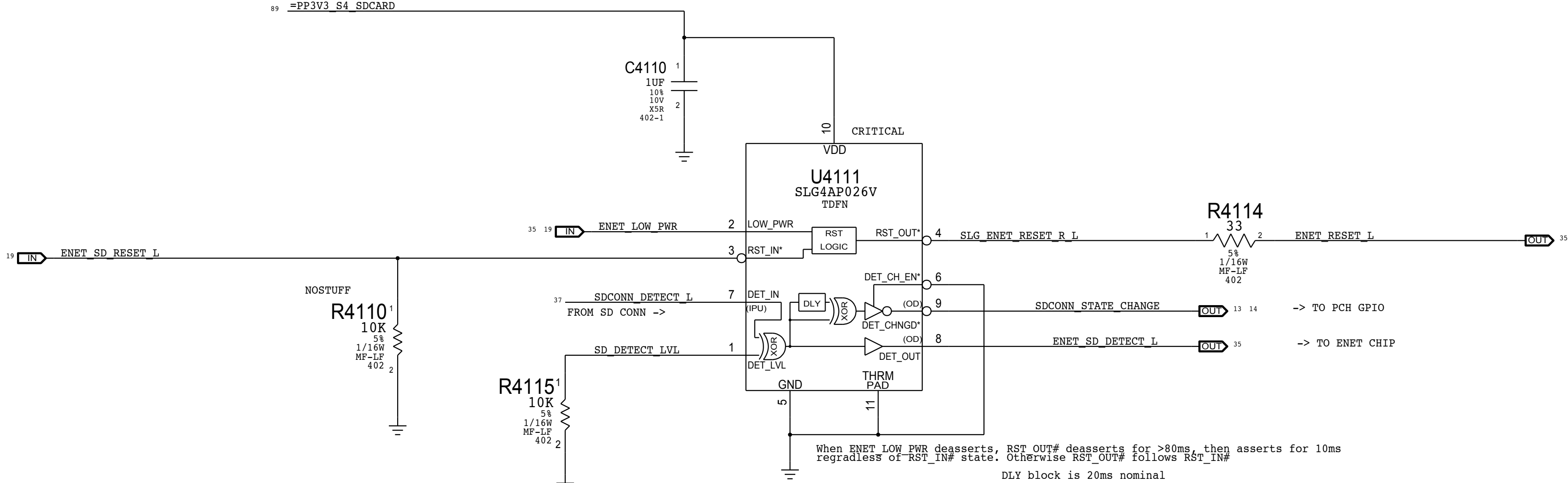



J16:516-0249 / J17:512-0038

SD CARD CONNECTOR



SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.



SYNC_MASTER=J16 IG		SYNC DATE=04/29/2013	
PAGE TITLE			
SD CARD: Connector			
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	0.24.0		
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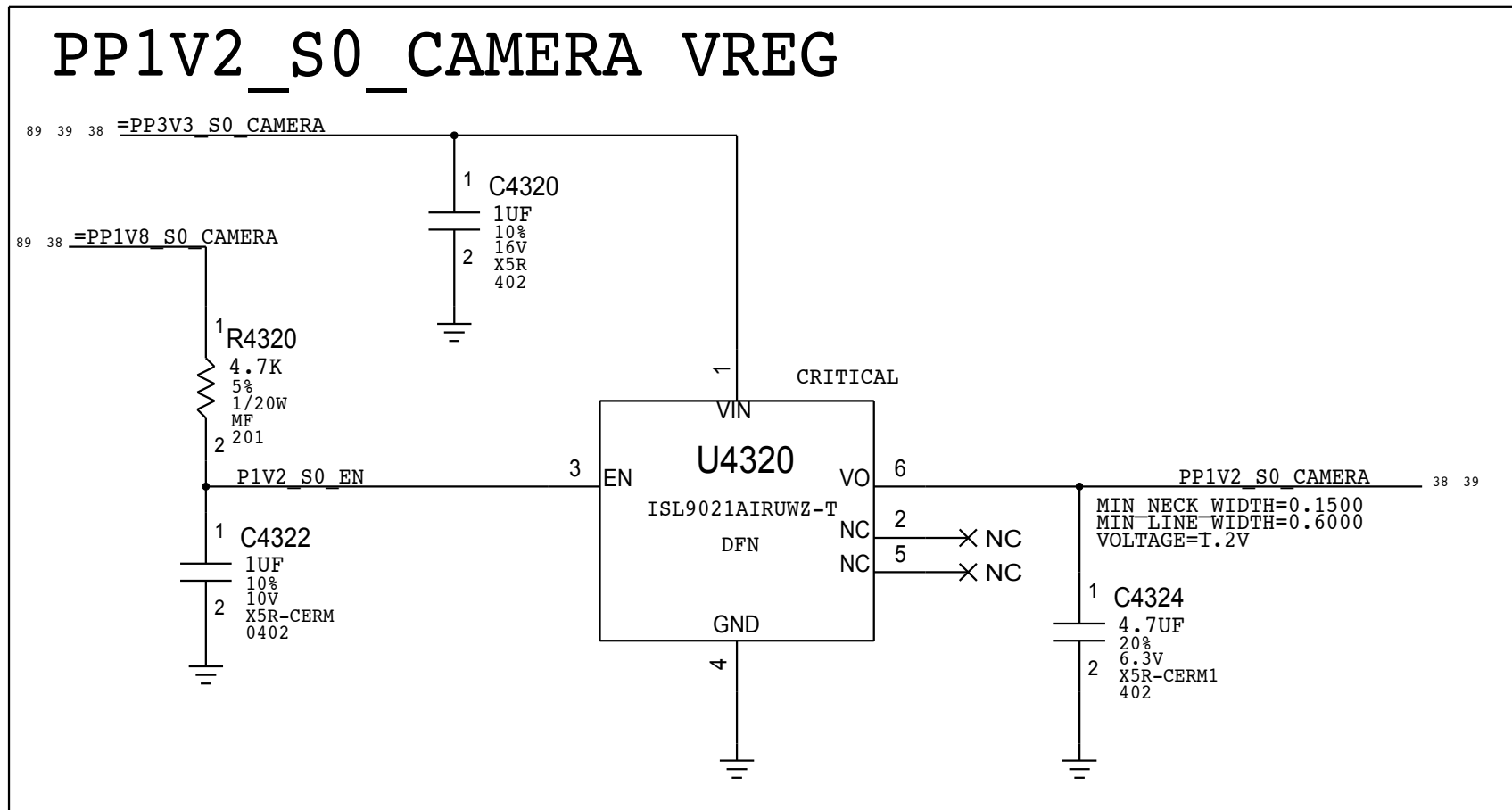
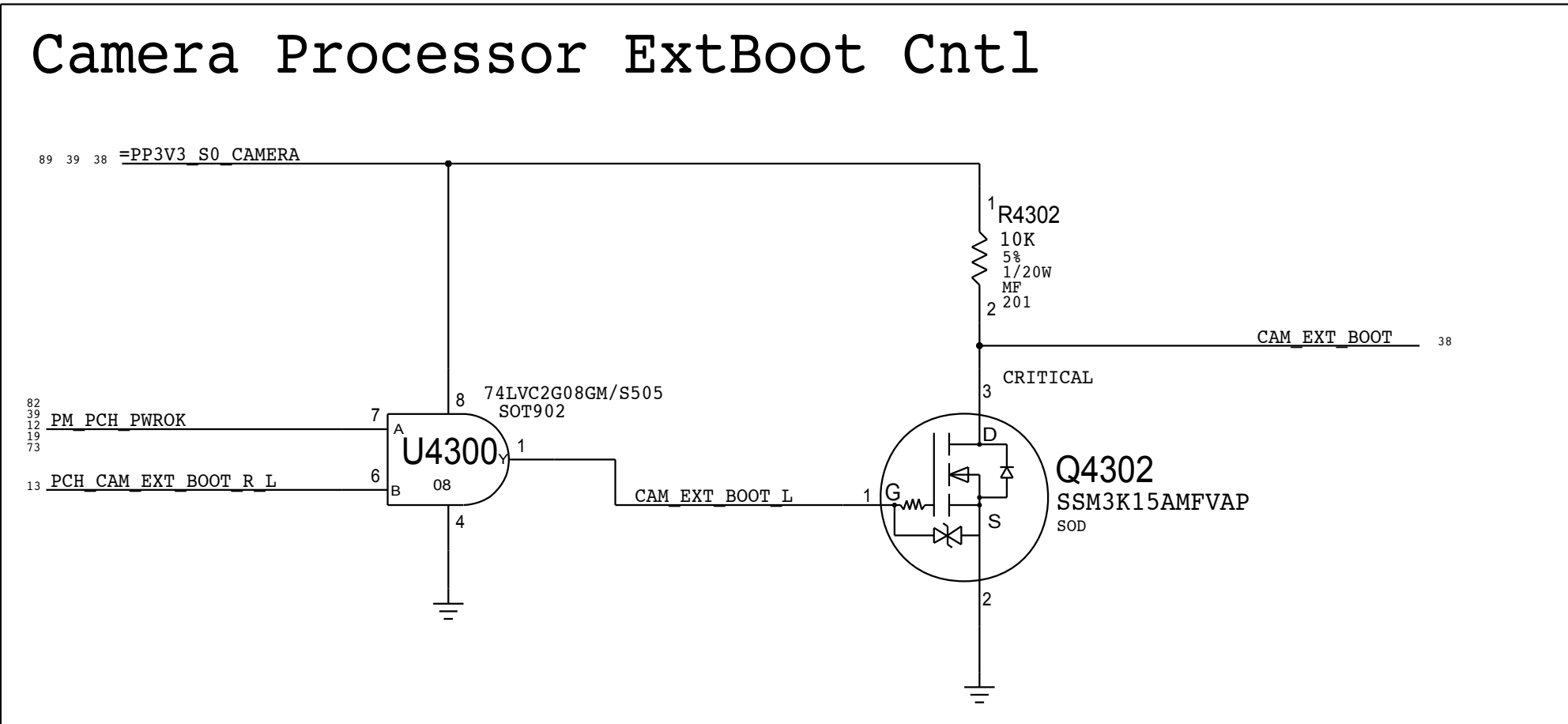
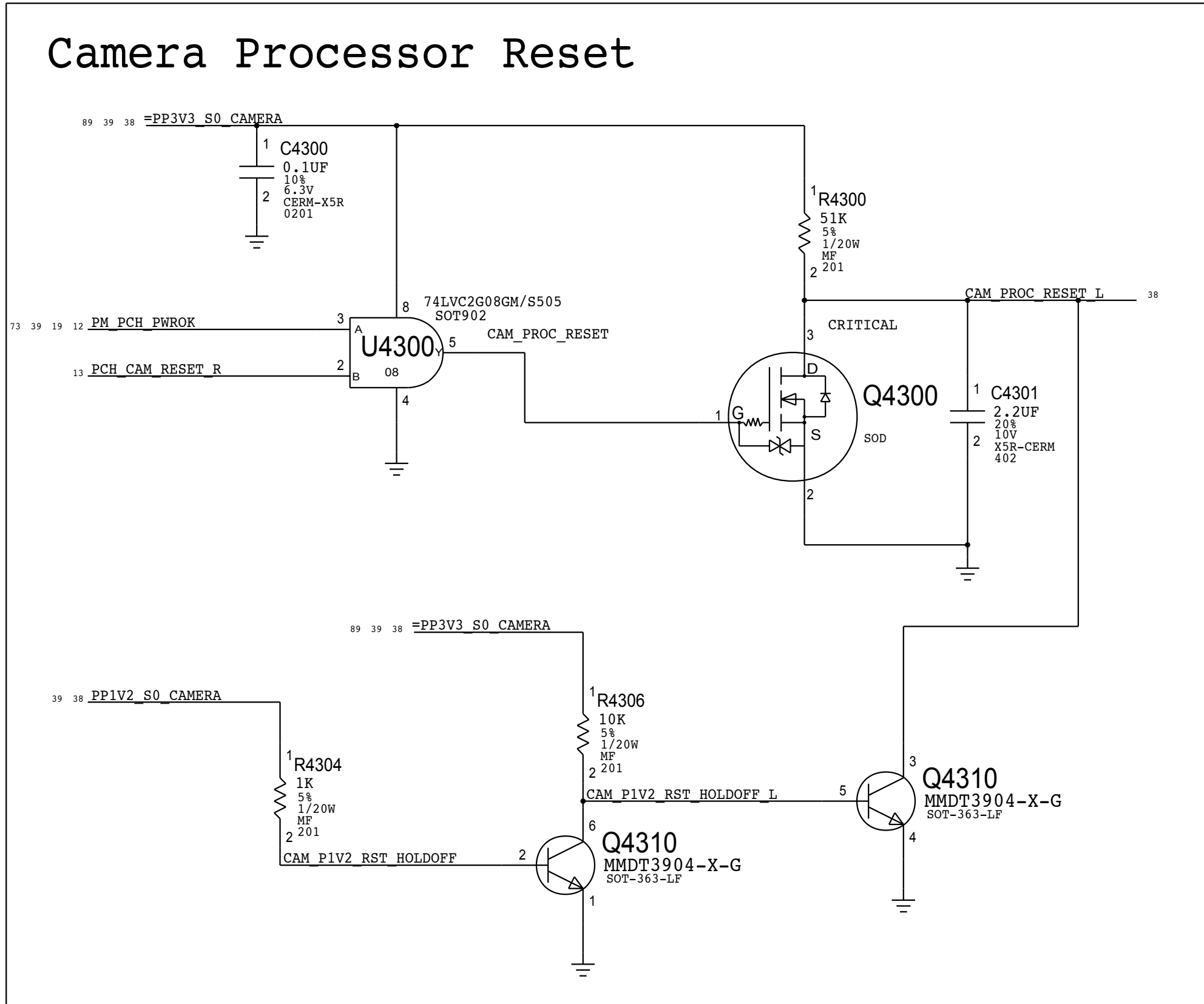
A


D

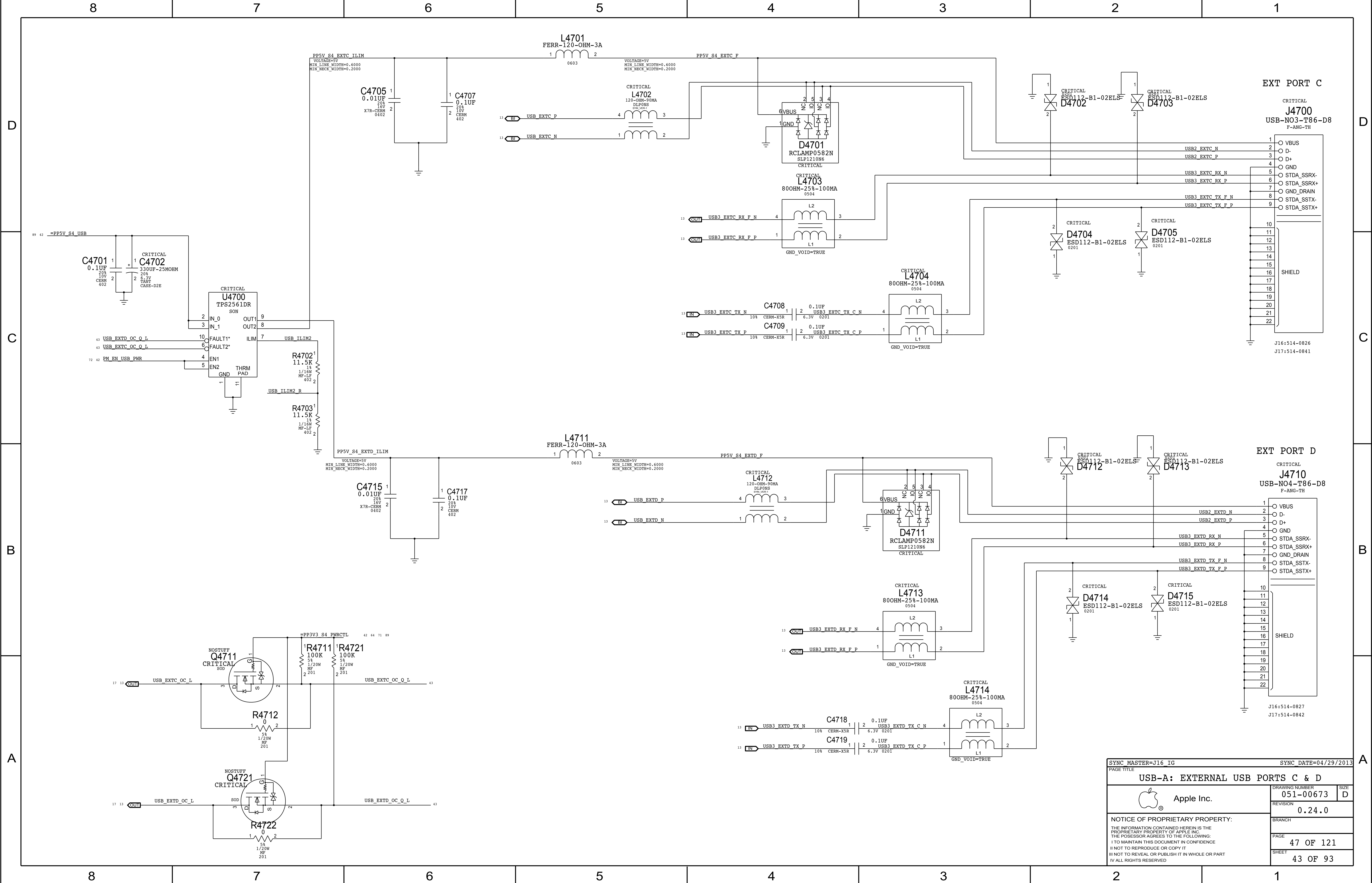
C


B

A

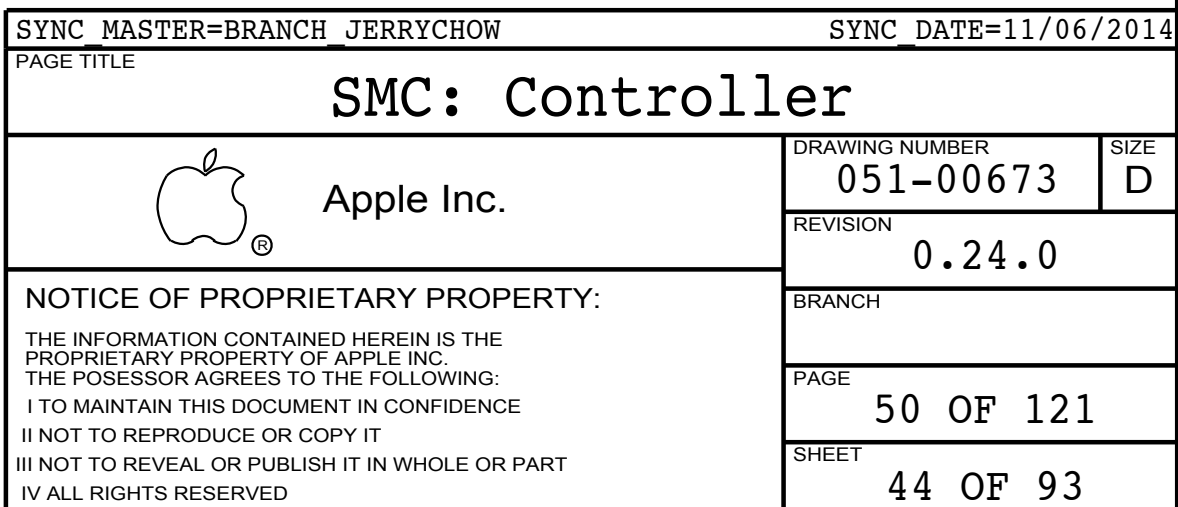


SYNC MASTER=J78 NAT		SYNC DATE=11/05/2013	
PAGE TITLE			
CAMERA: Controller Support			
	DRAWING NUMBER		SIZE
	051-00673		D
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SYNC_MASTER=J16_IG		SYNC_DATE=04/29/2013	
PAGE TITLE			
USB-A: EXTERNAL USB PORTS C & D			
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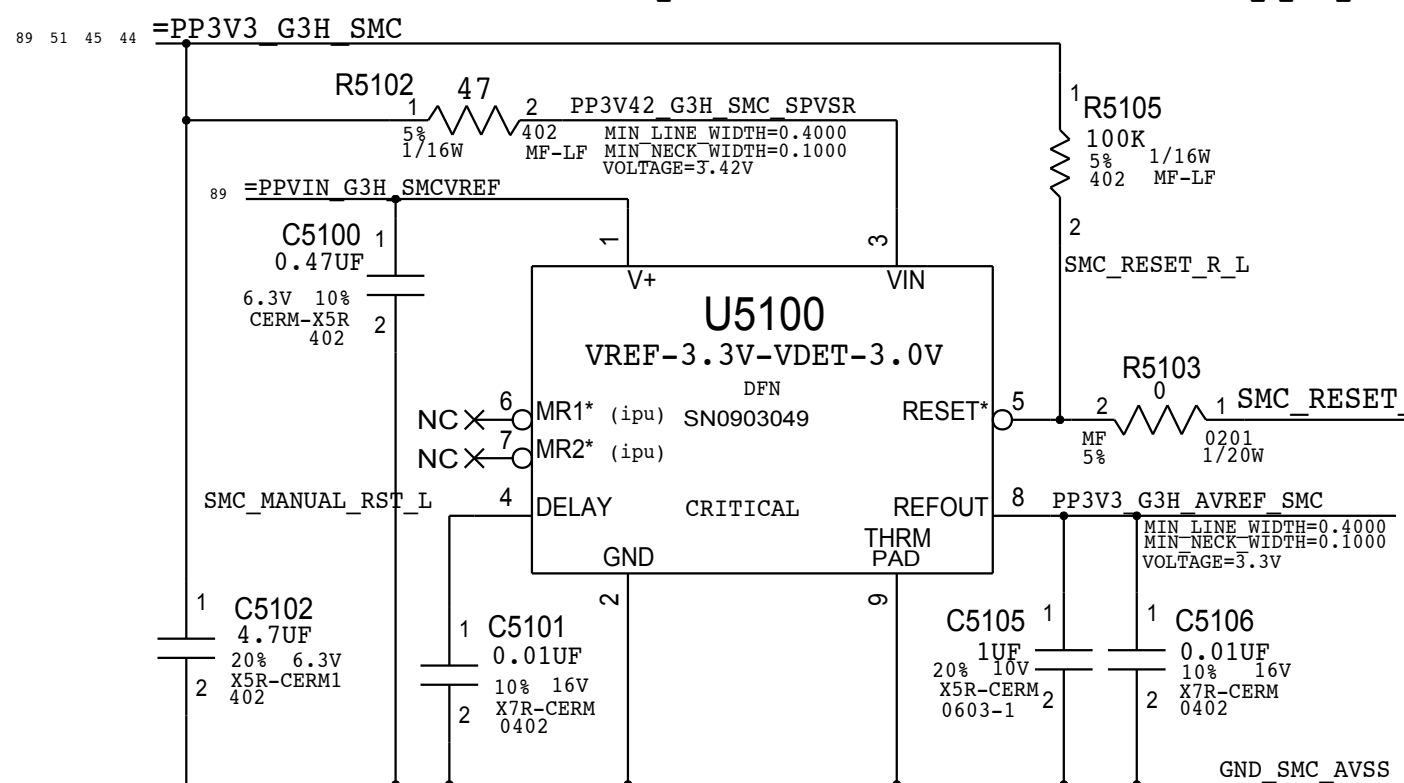
D

C

B

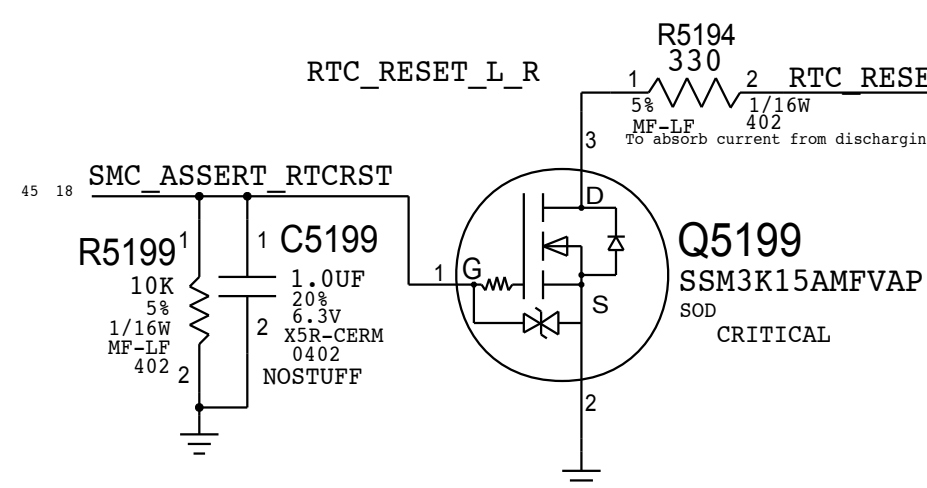
A

SMC Supervisor and AVREF Supply



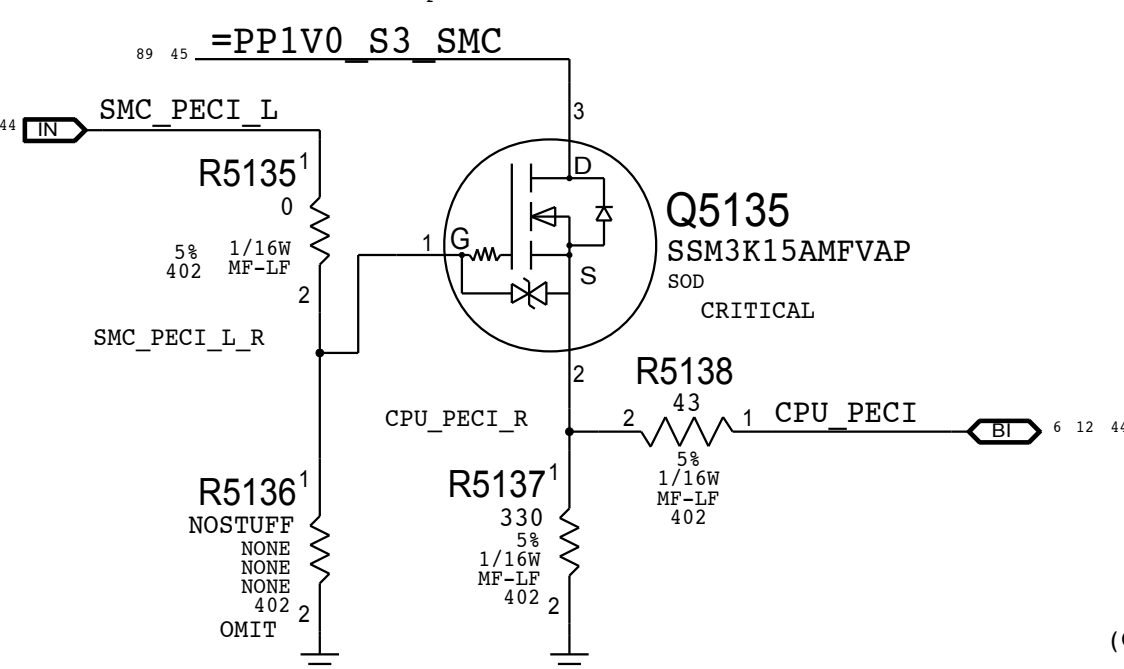
Note: IPU are pulled to VIN rail

SMC Controlled RTC Reset

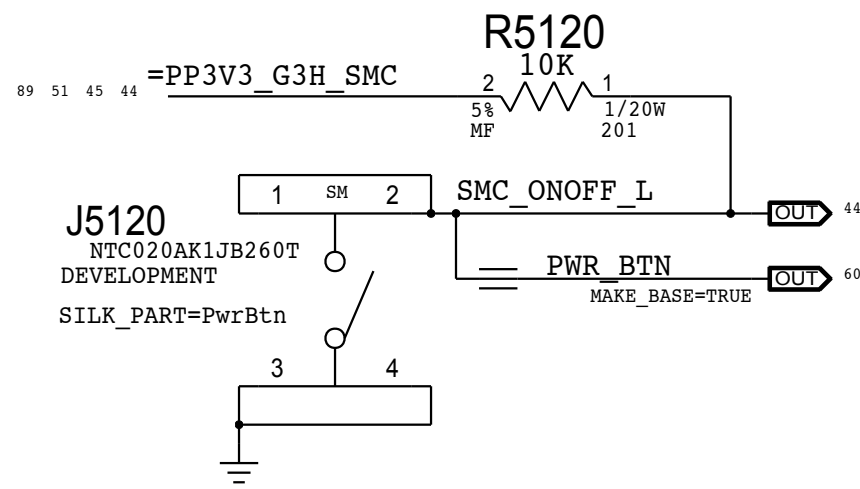


PECI Support

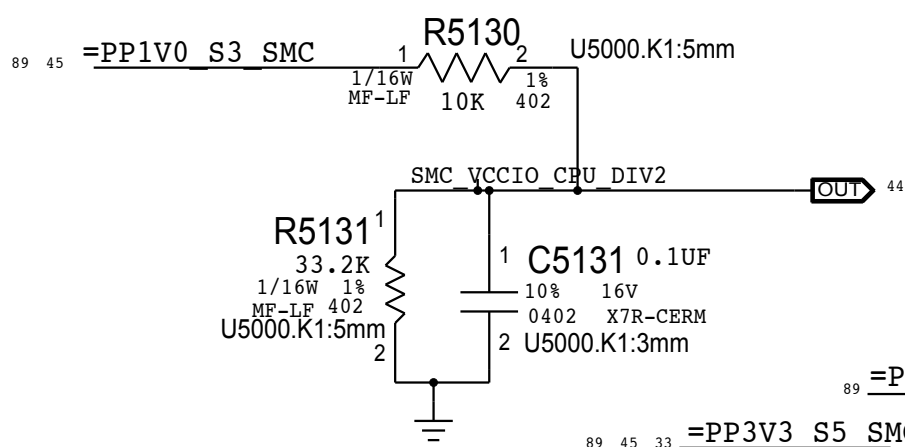
Level-shifter that allows SMC to drive PEGI
Place this circuit near the Tee point to minimize reflections



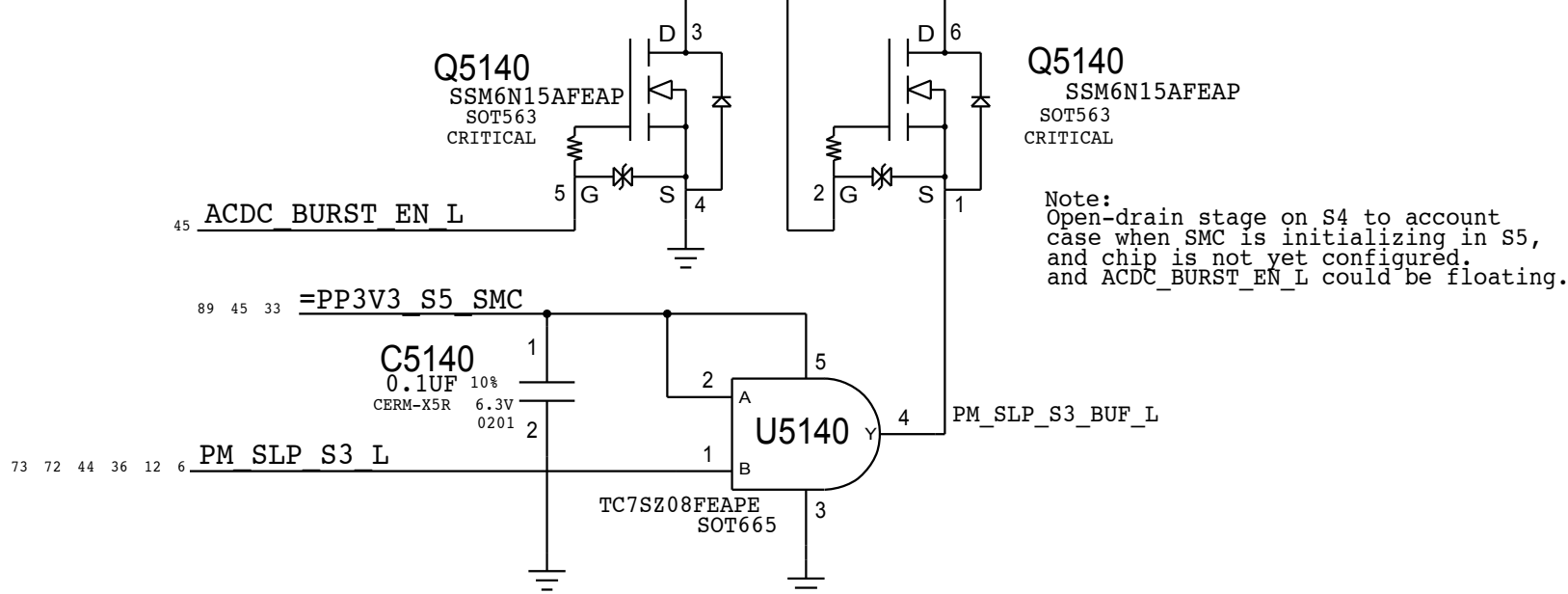
Power Button



Comparator VRef



AC/DC Burst Mode Enable



ADC Channel Aliases

SMC_ADC0	VSNS_P12VG3H	VD2R
SMC_ADC1	VSNS_P12V33H	ID2R
SMC_ADC2	VSNS_P12VS0_CPUCORE	VD20
SMC_ADC3	VSNS_P12VS0_CPUCORE	ID20
SMC_ADC4	VSNS_CPUVCC	VC0C
SMC_ADC5	VSNS_CPUVCC	IC0C
SMC_ADC6	VSNS_CPUVCC_GT	VC0G
SMC_ADC7	VSNS_CPUVCC_GT	IC0G
SMC_ADC8	VSNS_CPUVCC_IO	IC0I
SMC_ADC9	VSNS_P1V35S0	IC0M
SMC_ADC10	VSNS_CPUVCC_SA	IC0S
SMC_ADC11	VSNS_P12VS0_FBDQDQ	IG1F
SMC_ADC12	VSNS_GPUCCORE_ALT	VG0C
SMC_ADC13	VSNS_GPUCCORE_ALT	IG0C
SMC_ADC14	VSNS_GPU_VDDCI	VG0I
SMC_ADC15	VSNS_GPU_VDDCI	IG0I
SMC_ADC16	VSNS_P12VS0_GPU_AUX	IG1A
SMC_ADC17	VSNS_P12VS0_GPUCCORE	IG1C
SMC_ADC18	VSNS_P12VS0_HDD	IH02
SMC_ADC19	VSNS_HDD0S	IH05
SMC_ADC20	VSNS_SSD_S4	VH1R
SMC_ADC21	VSNS_SSD_S4	IH1R
SMC_ADC22	VSNS_VDDQ03_DDR	VM0R
SMC_ADC23	VSNS_VDDQ03_DDR	IM0R

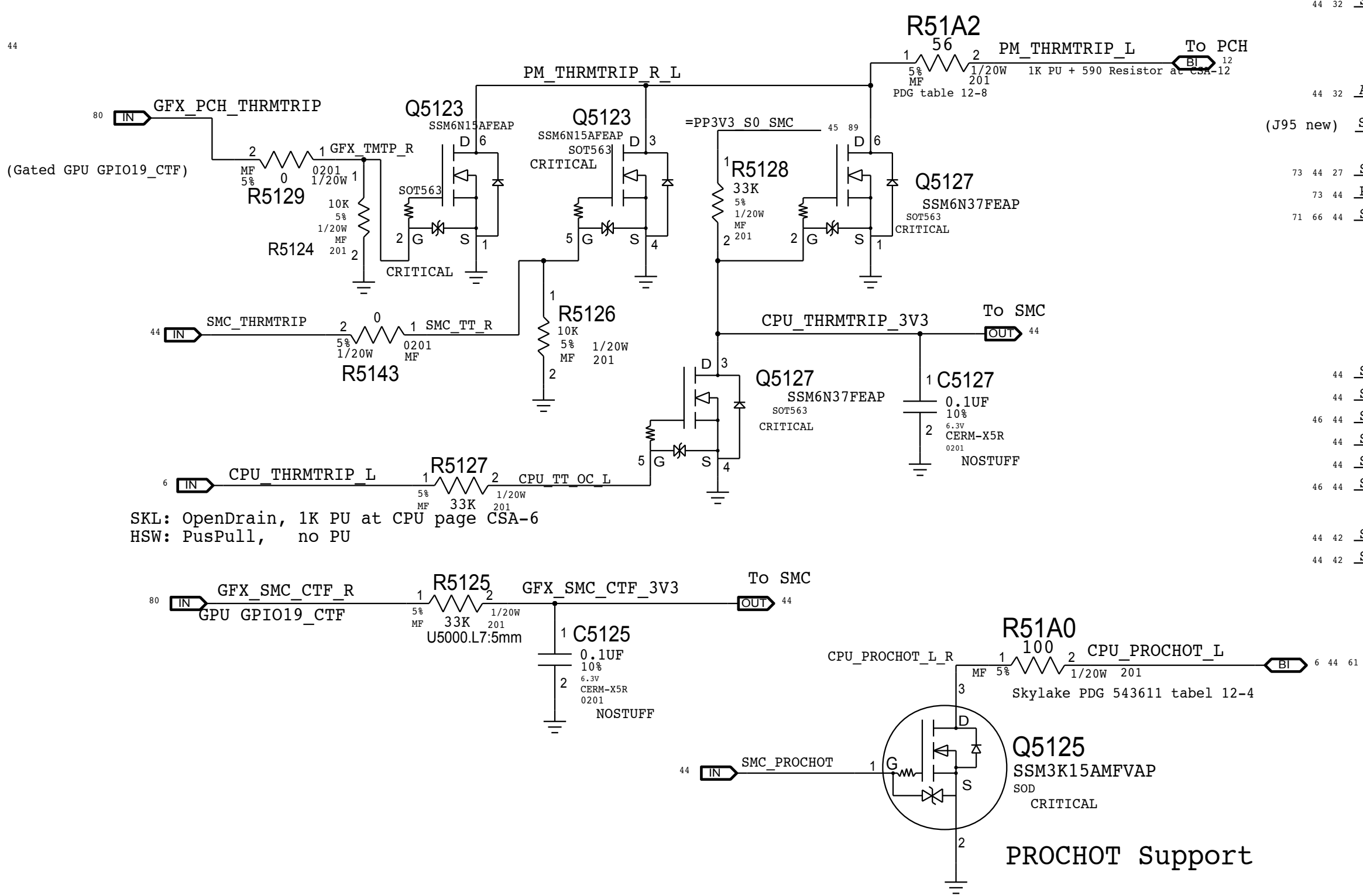
Project-specific Aliases

SMC_PN5	ACDC_BURST_EN_L	VD2R
SMC_PJ3	SMC_OOB2_R2D_L	ID2R
SMC_PJ2	SMC_OOB2_D2R_L	VD20
SMC_PP0	SMC_ACDC_ID	ID20
SMC_PH2	SMC_ASSERT_RTCRST	VC0C
SMC_PL6	SMC_WIFI_PWR_EN	IC0C
SMC_PN3	TCN_BLC_EN	(LED-4)
SMC_PH7	GPX_OK_L	(LED-3)
SMC_PN7	DP_LINK_OK	(LED-3)

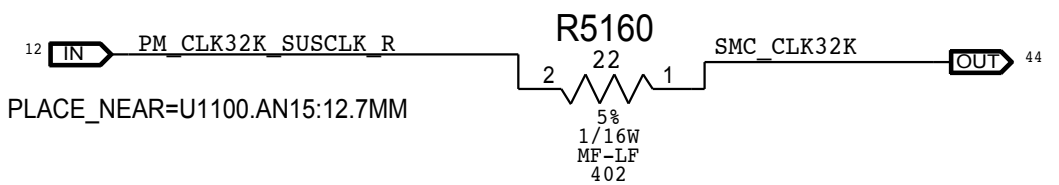
Unused Project-specific

SMC_PP0	NC_SMC_PP0	
SMC_PP1	NC_SMC_PP1	
SMC_PP2	NC_SMC_PP2	
SMC_PP3	NC_SMC_PP3	
SMC_PL7	SMC_BT_PWR_EN	(J95 new)
SMC_PP4	NC_SMC_S4_WAKESRC_EN	
SMC_PP5	NC_SMC_PP5	
SMC_PP6	NC_SMC_PP6	
SMC_PP7	NC_SMC_PP7	
SMC_DP_HPD_L	NC_SMC_DP_HPD_L	
SMC_PME_S4_DARK_L	NC_SMC_PME_S4_DARK_L	
SMC_PC4	NC_SMC_S5_PWRGD_VIN	
SMC_PQ3	NC_G3_POWERON_L	
SMC_PN6	NC_SMC_G3_WAKESRC_EN	
SMBUS_SMC_4_ASF_SCL	NC_SMBUS_SMC_4_ASF_SCL	
SMBUS_SMC_4_ASF_SDA	NC_SMBUS_SMC_4_ASF_SDA	
SMBUS_SMC_5_G3H_SCL	NC_SMBUS_SMC_5_G3H_SCL	
SMBUS_SMC_5_G3H_SDA	NC_SMBUS_SMC_5_G3H_SDA	
SMC_OOB1_R2D_L	NC_SMC_OOB1_R2D_L	
SMC_BATLOW_L	NC_SMC_SMC_BATLOW_L	
SMC_PH3	NC_SMC_PH3	

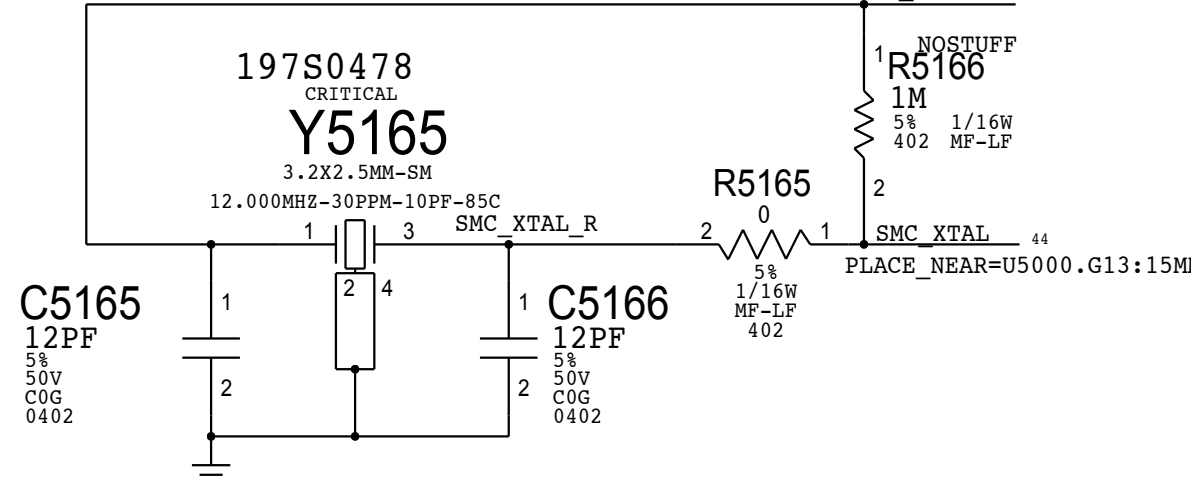
Platform Thermal Control



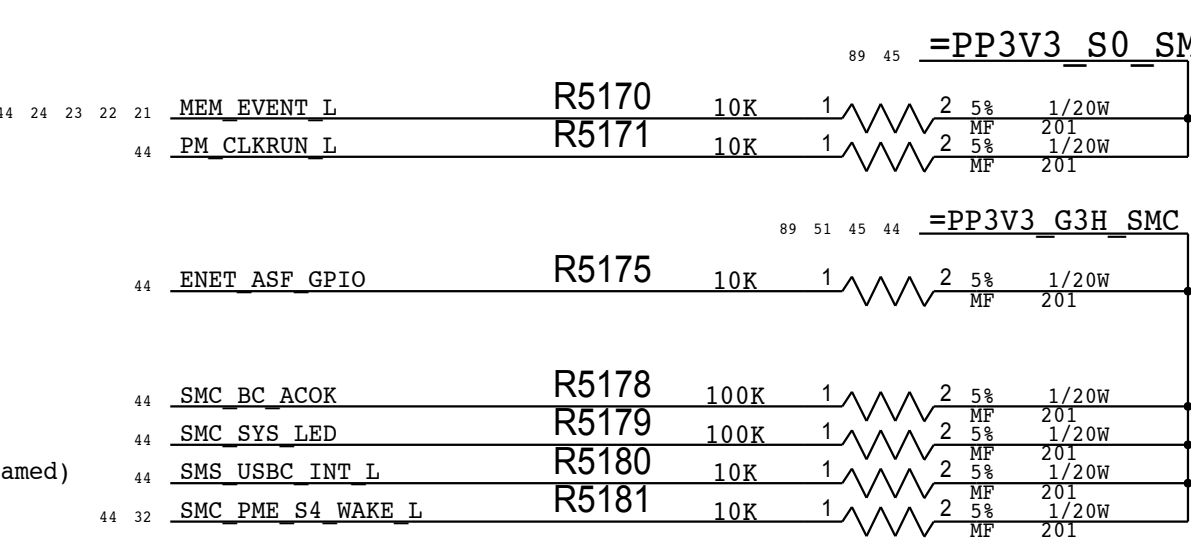
SMC 32KHz Clock



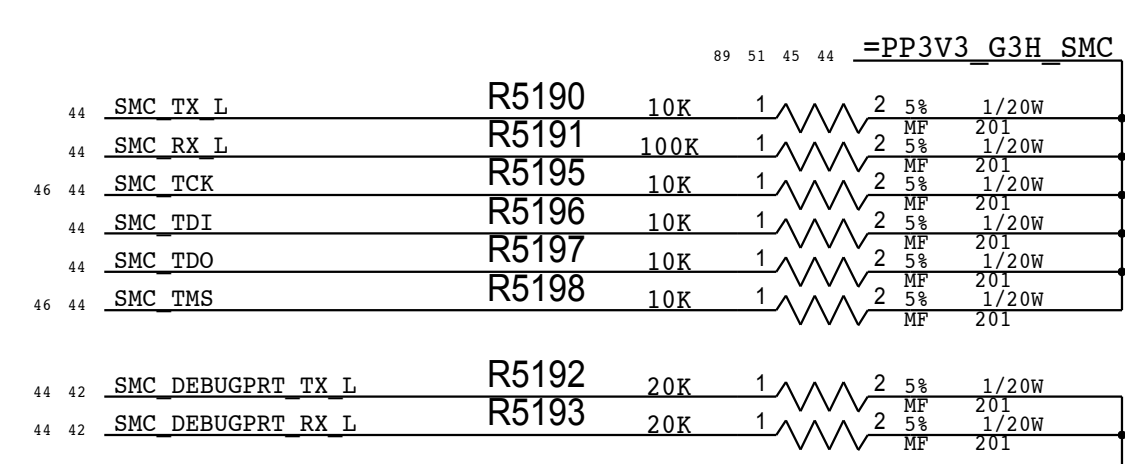
SMC Crystal



Arch Pull Up/Down



Serial/JTAG Interface Pull-ups



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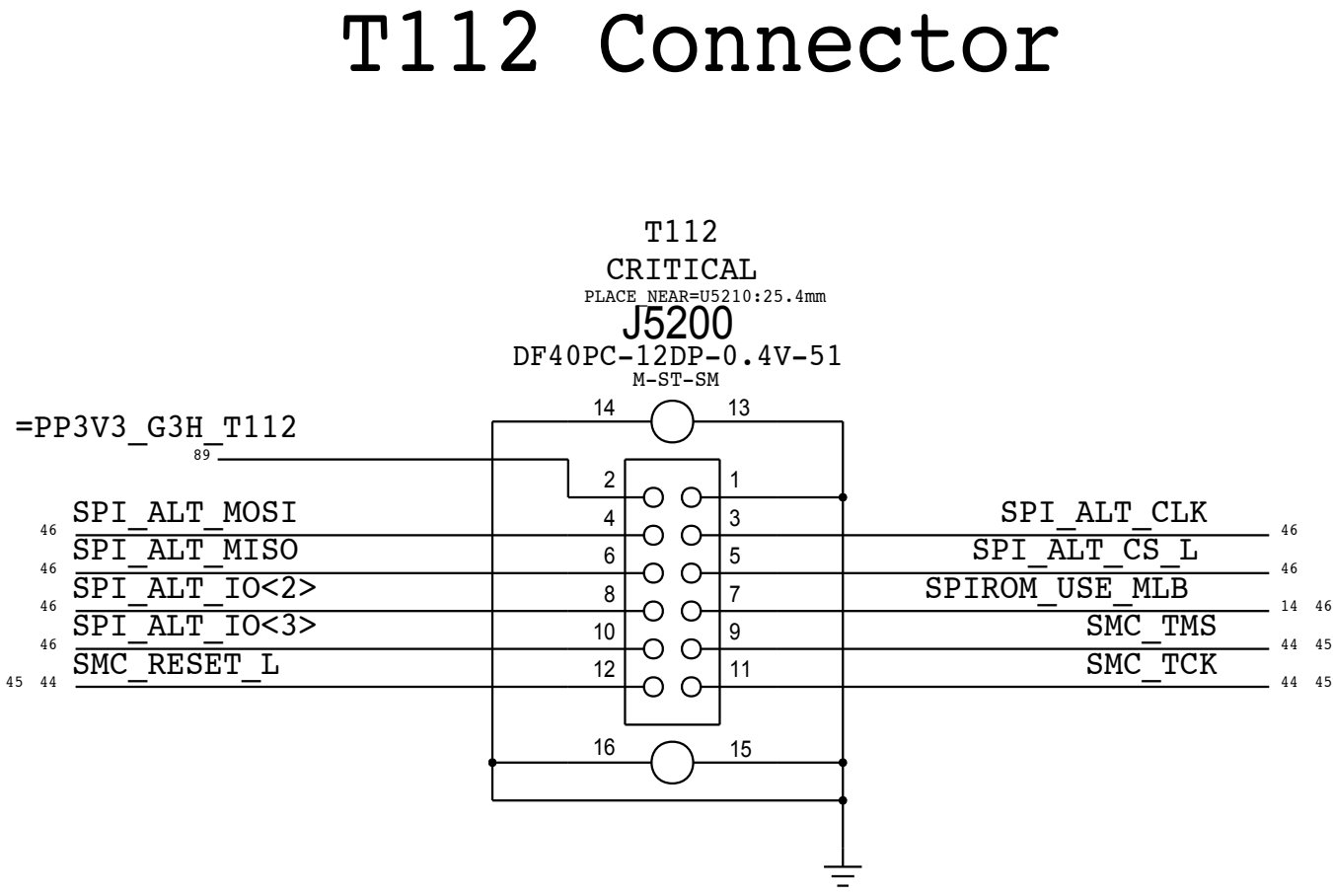
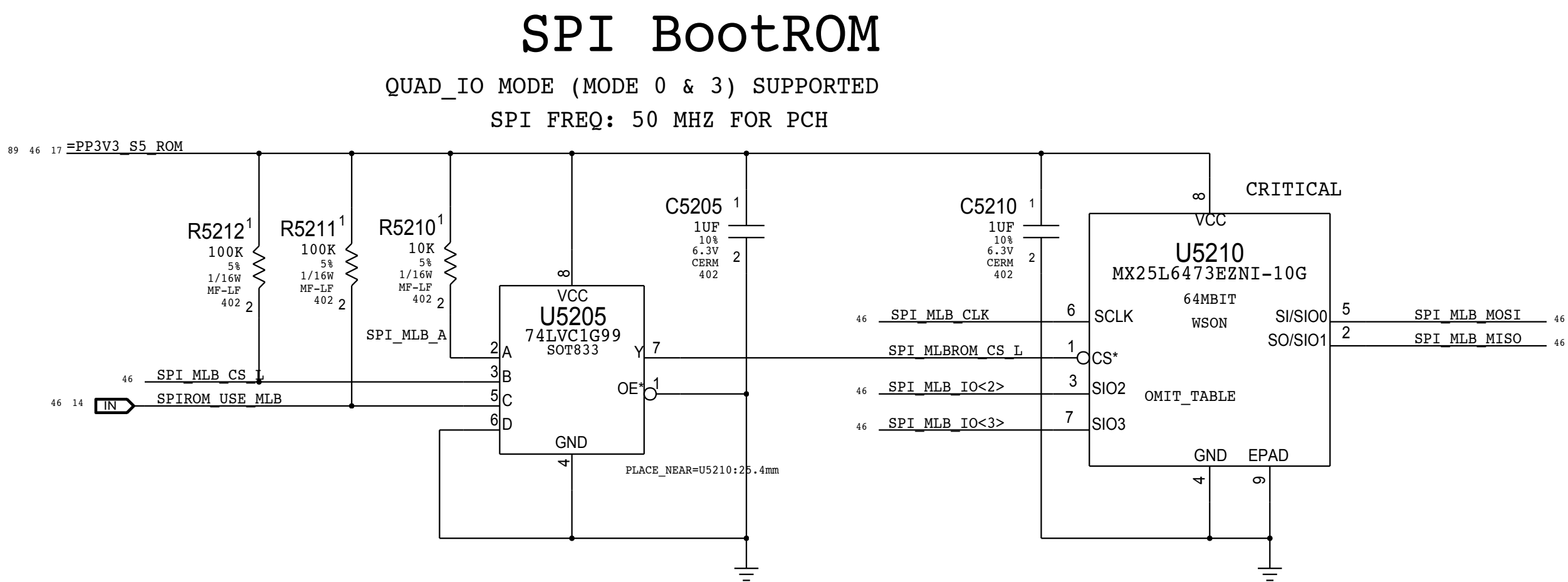
A

D

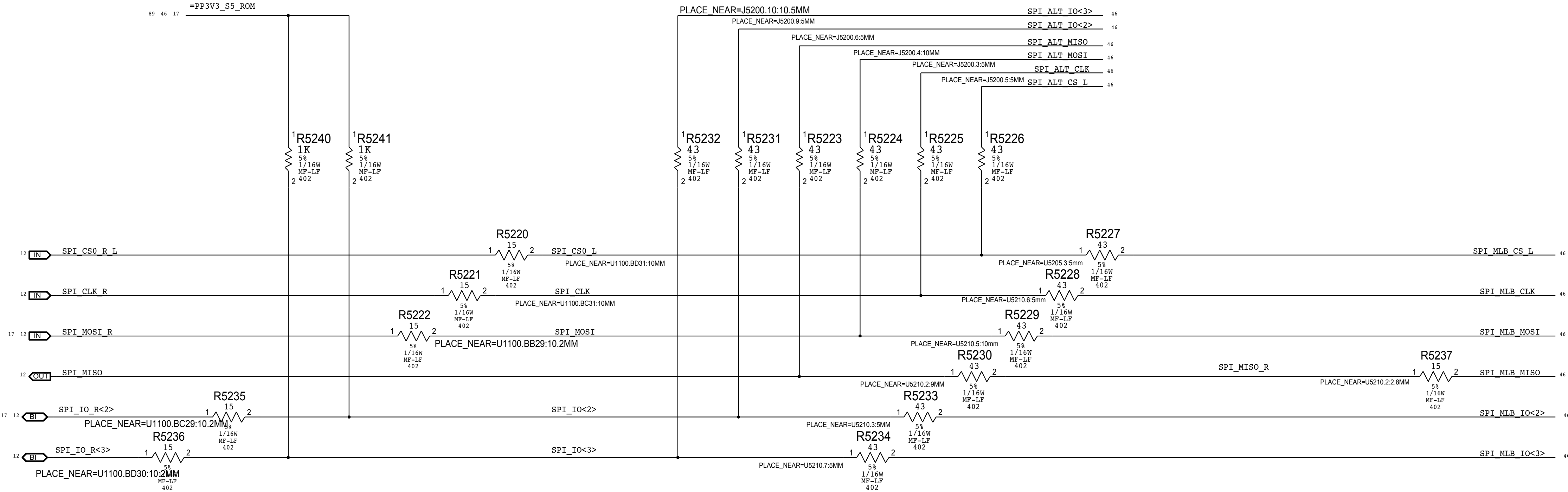
C


B

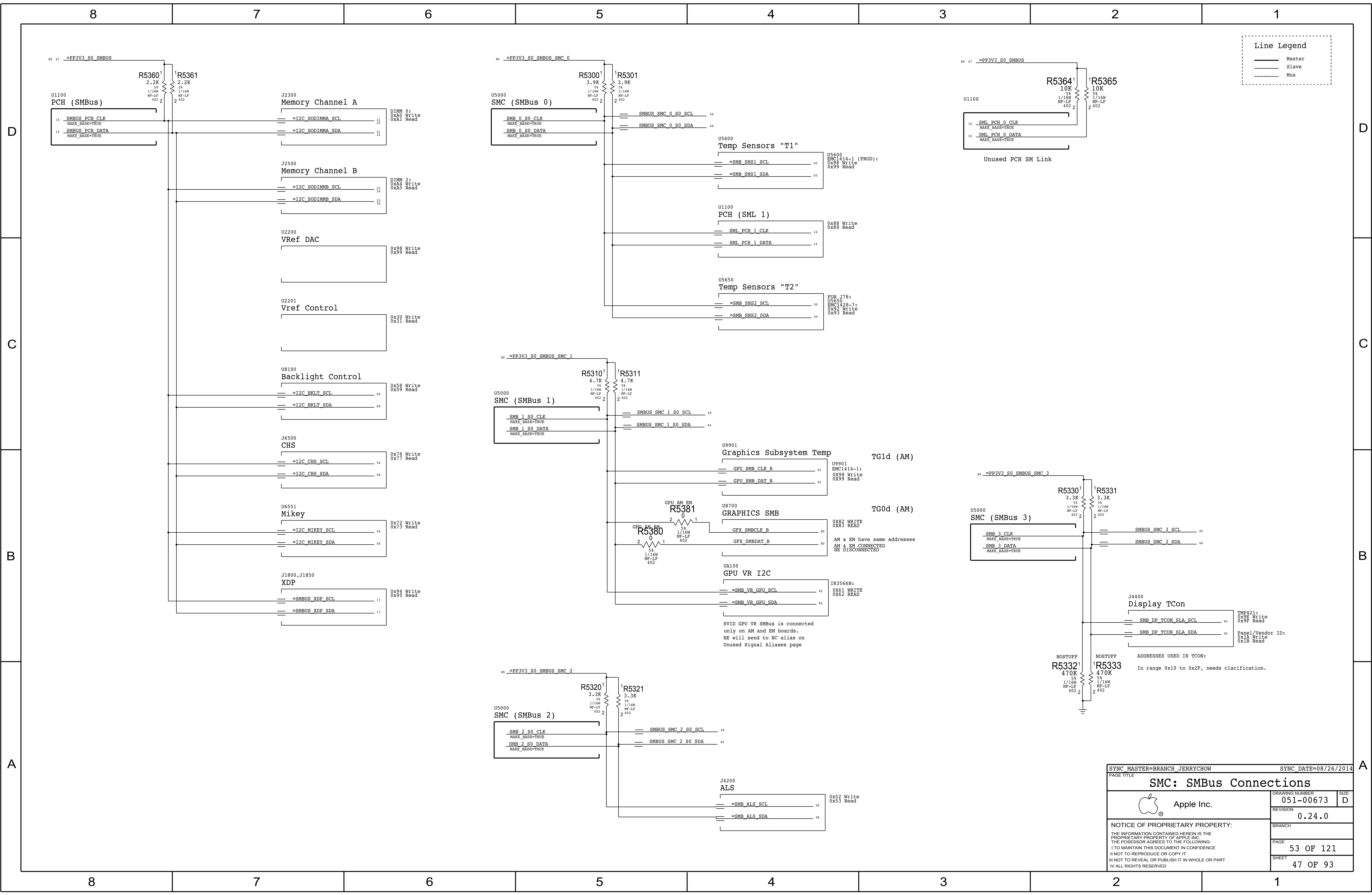
A



SPI Series Termination



SYNC_MASTER=J17_TONY		SYNC_DATE=03/13/2013	
PAGE TITLE			
CPU & CHIPSET: SPI and Debug Connector			
 Apple Inc.	DRAWING NUMBER	051-00673	SIZE
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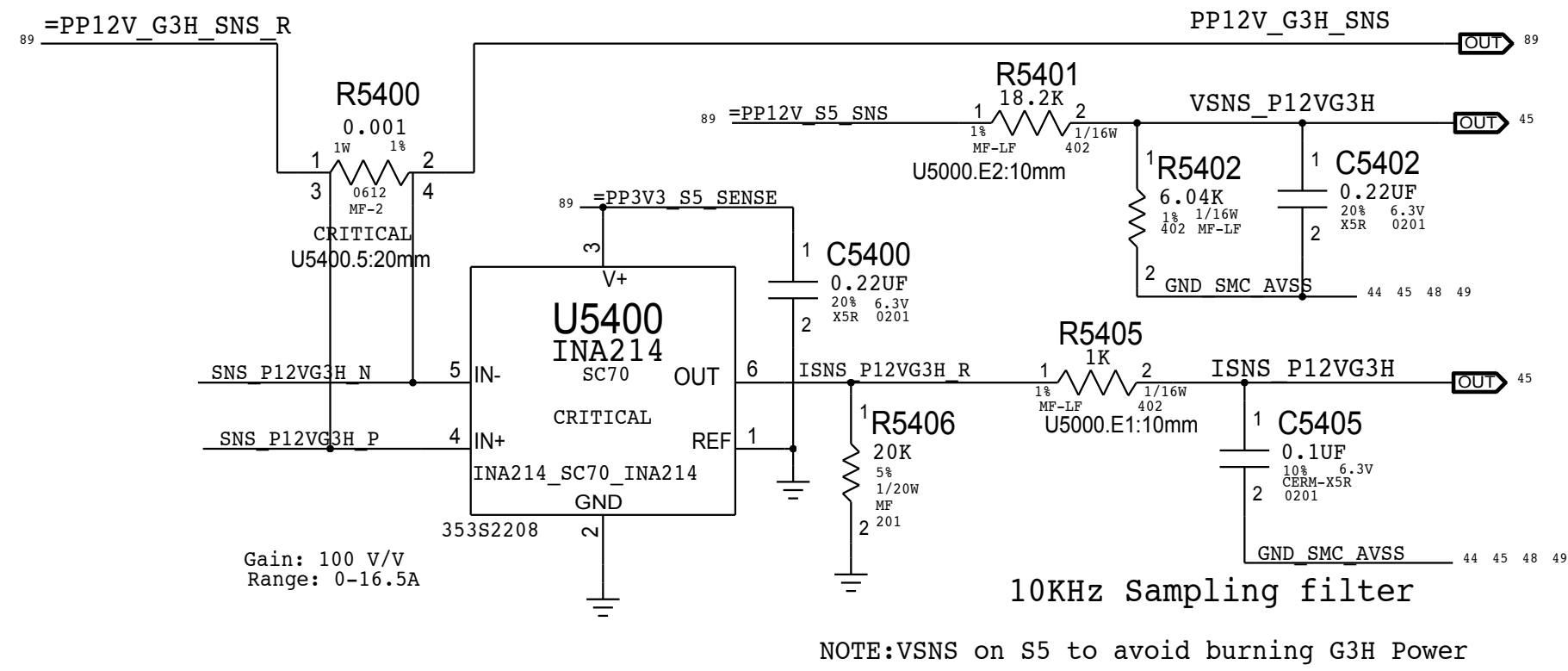
D

C

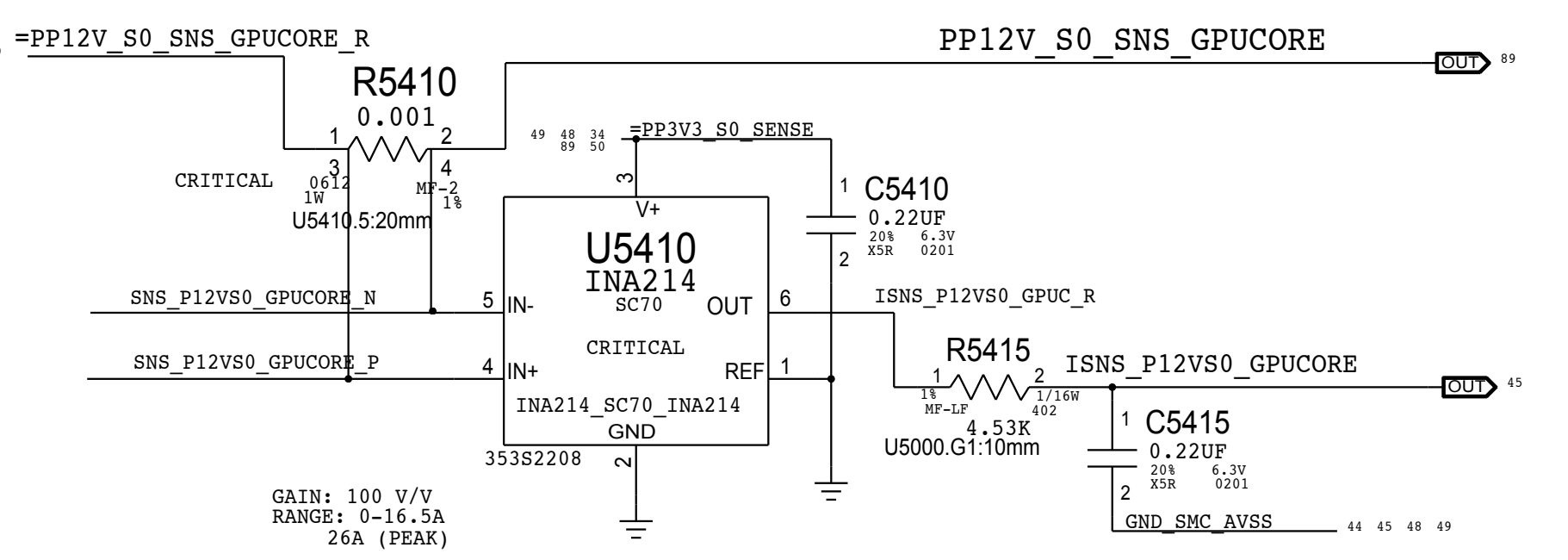
B

A

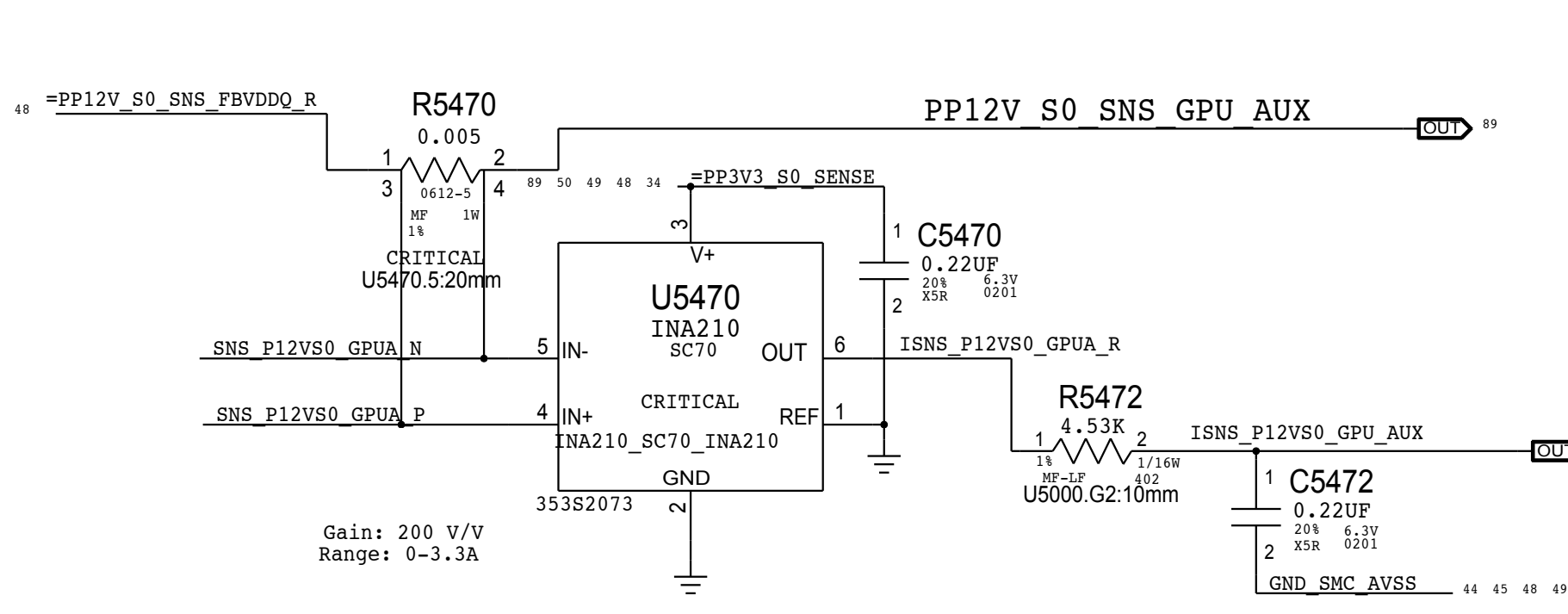
12V G3H (VD2R:ADC0/ID2R:ADC1)



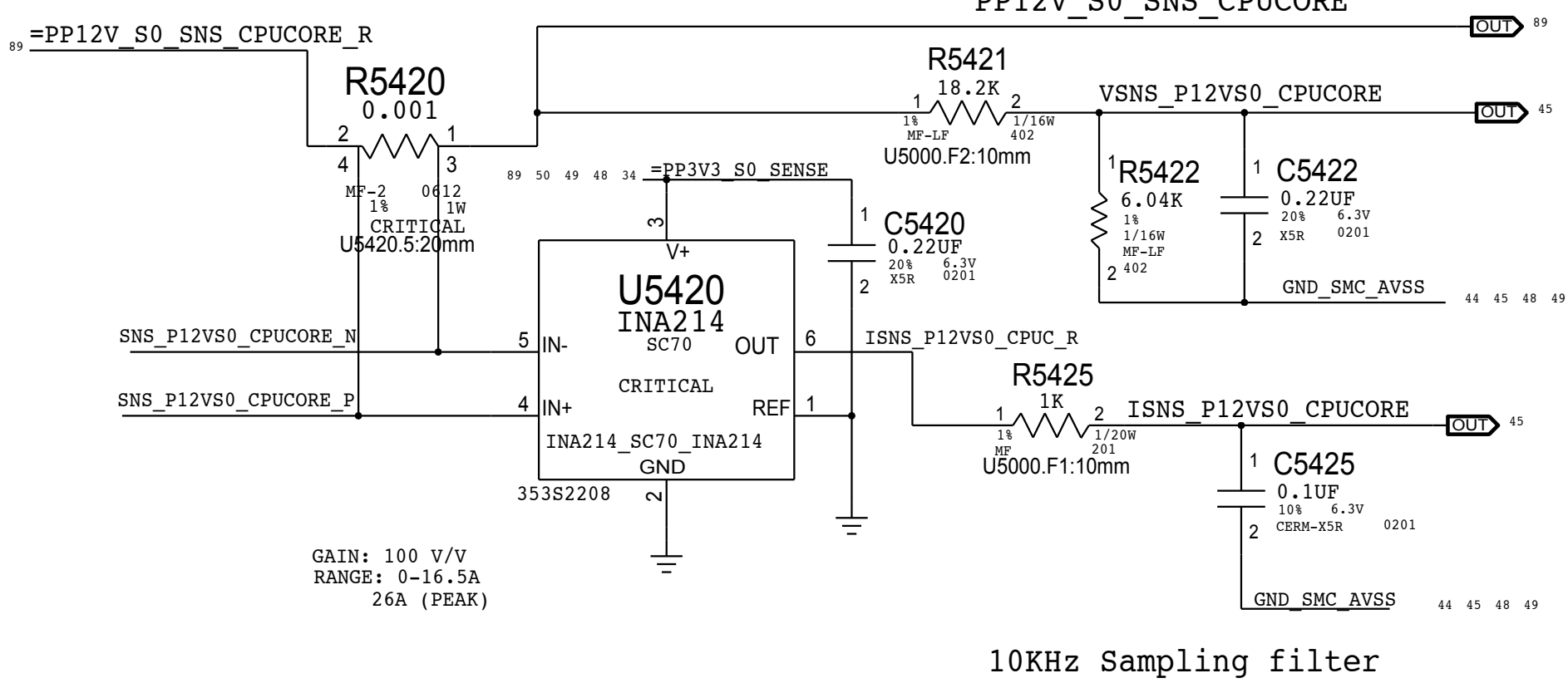
PP12V_S0_GPU (VG1C=VD20, IG1C:ADC17)



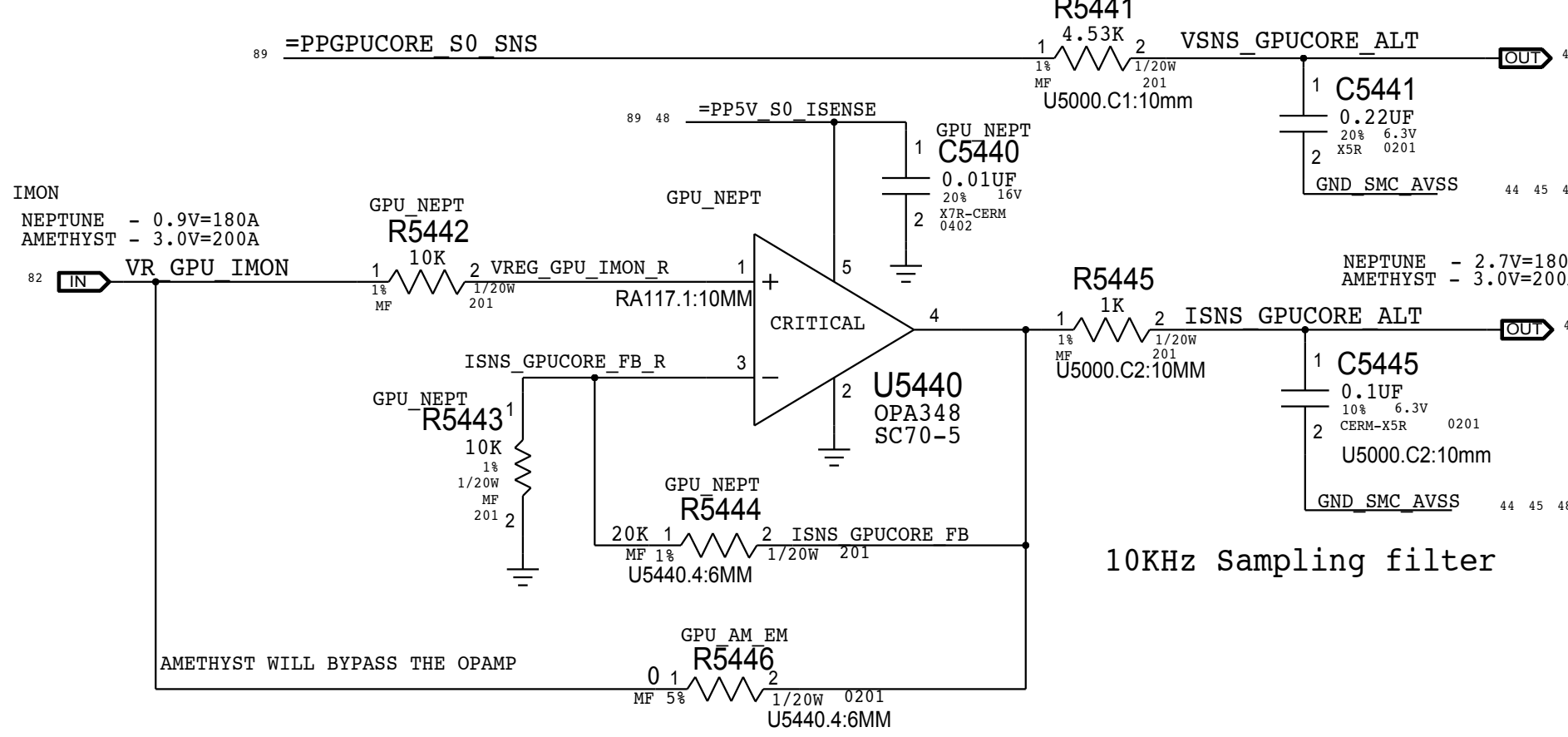
GPU AUX RAILS (VG1A=VD20, IG1A:ADC16)



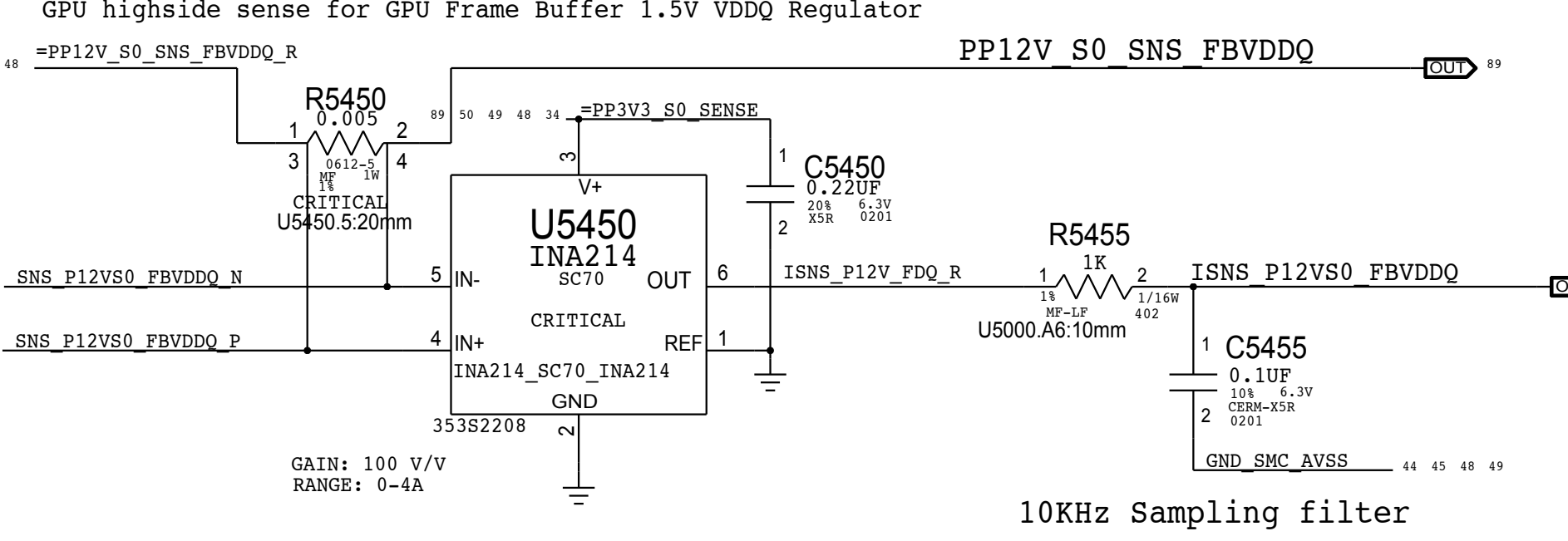
PP12V_S0_CPU (VD20:ADC2 /ID20:ADC3)



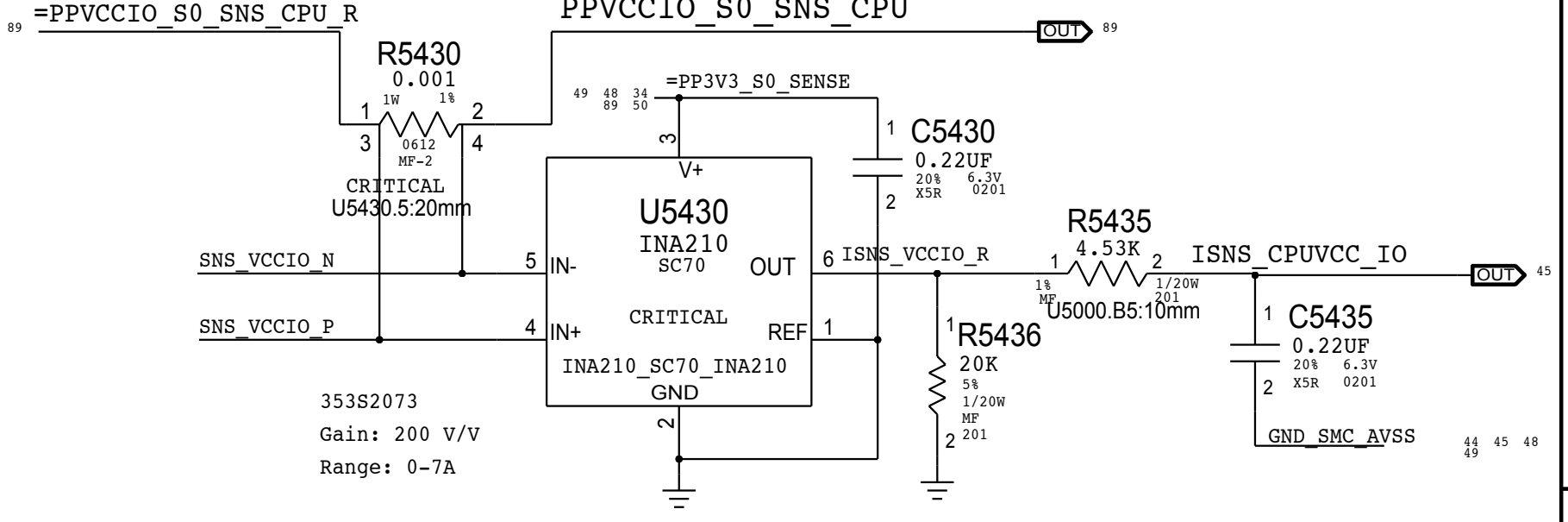
GPU Core - Alt (VG0C:ADC12/IG0C:ADC13)



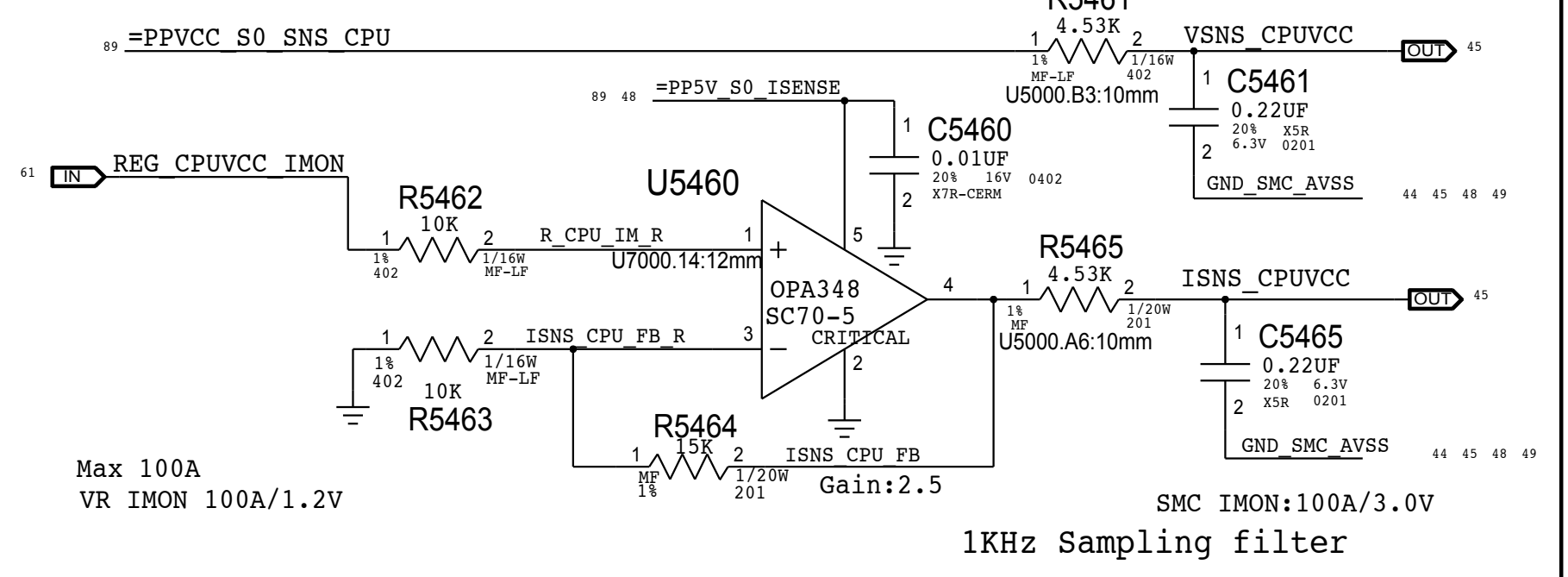
GPU FB (VG1F=VD20, IG1F:ADC11)



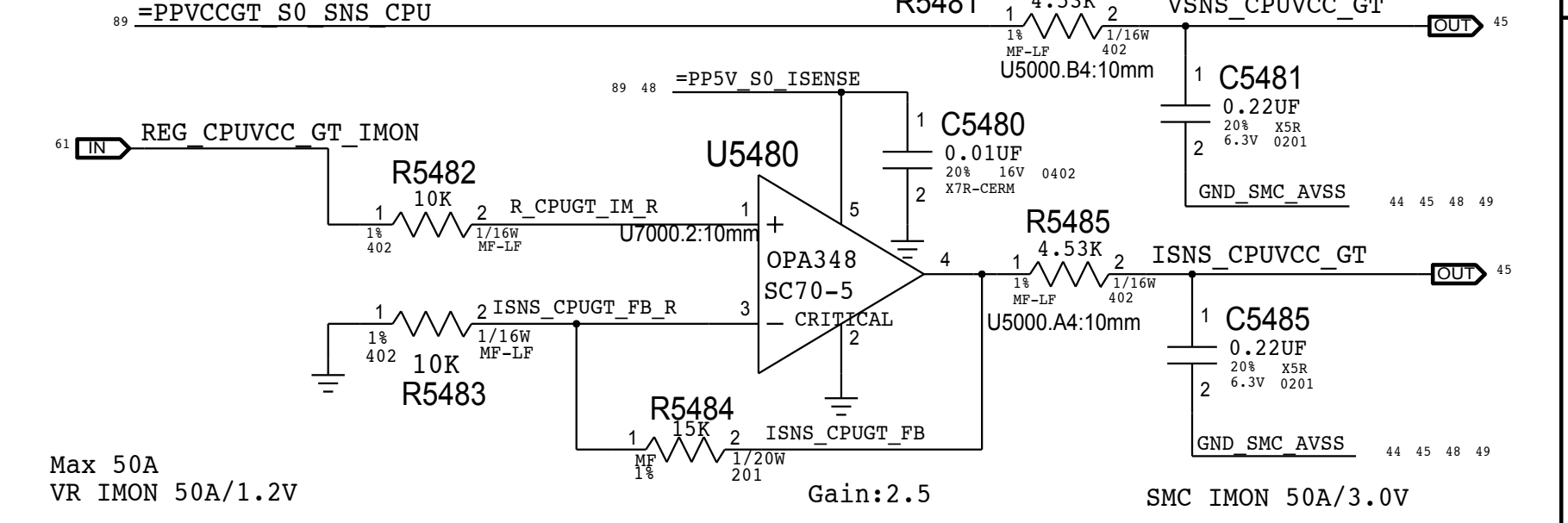
CPU VCCIO (VC0I=tbid, IC0I:ADC8)



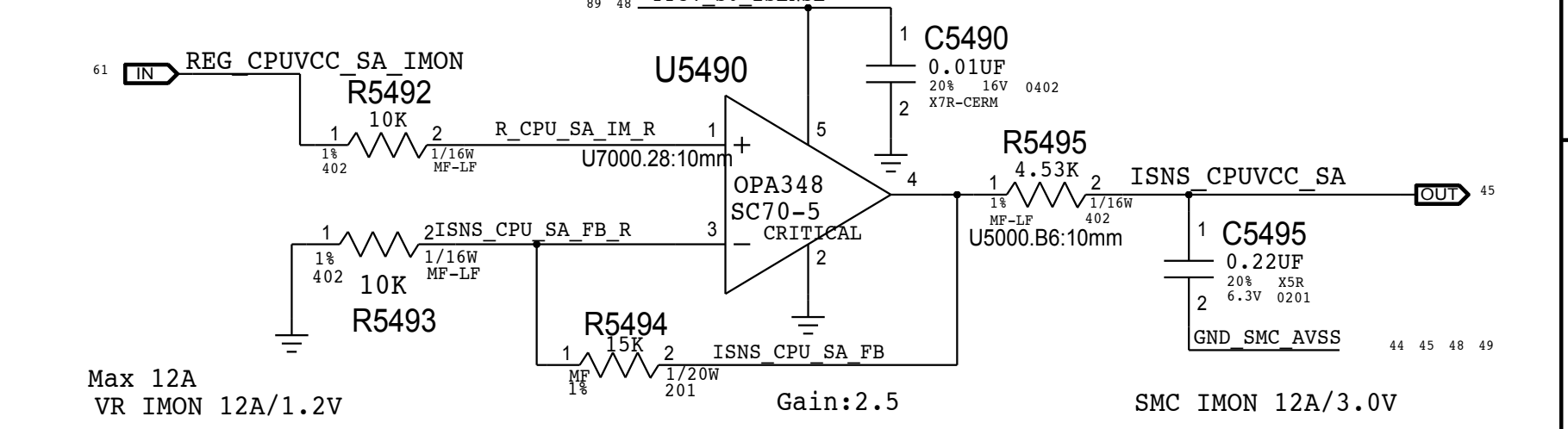
CPU Core (VC0C:ADC4/IC0C:ADC5)




CPU Core GT (VC0G:ADC6/IC0G:ADC7)



CPU Core VCC_SA (VC0S=1.05V, IC0S:ADC10)



SYNC_MASTER=BRANCH JERRYCHOW		SYNC_DATE=09/10/2014	
PAGE TITLE			
SENSORS: I and V Sense			
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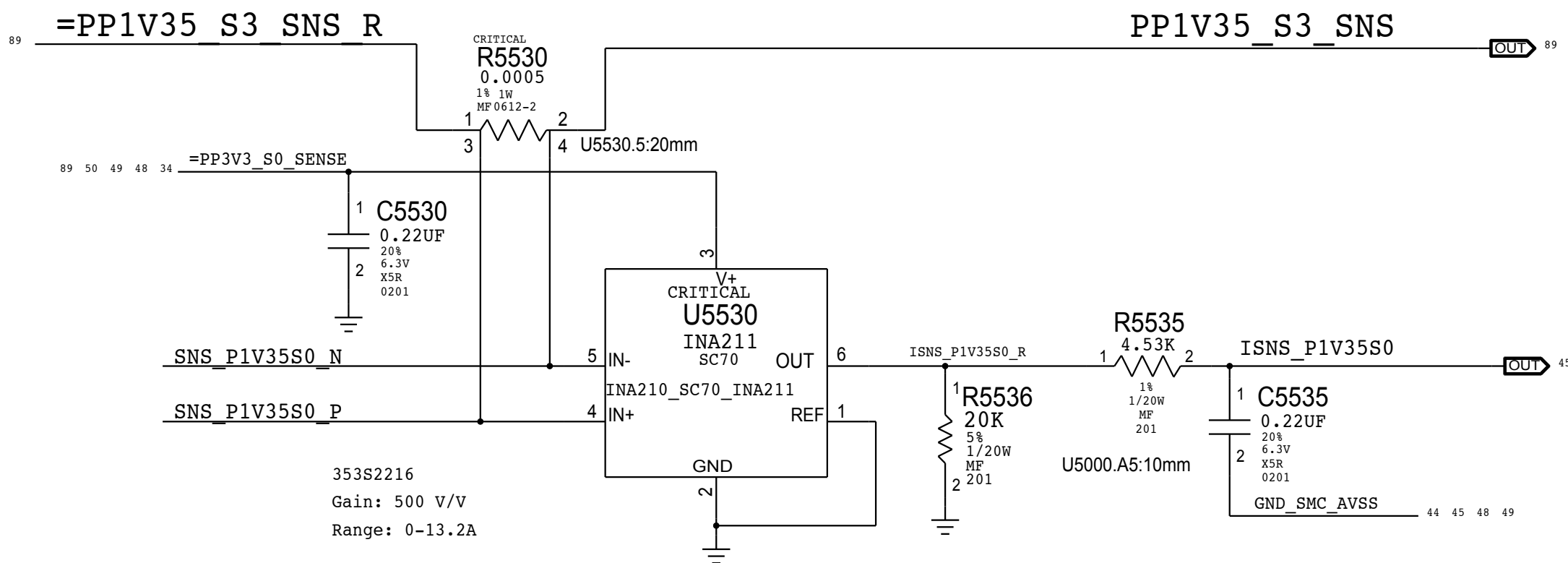
B

A

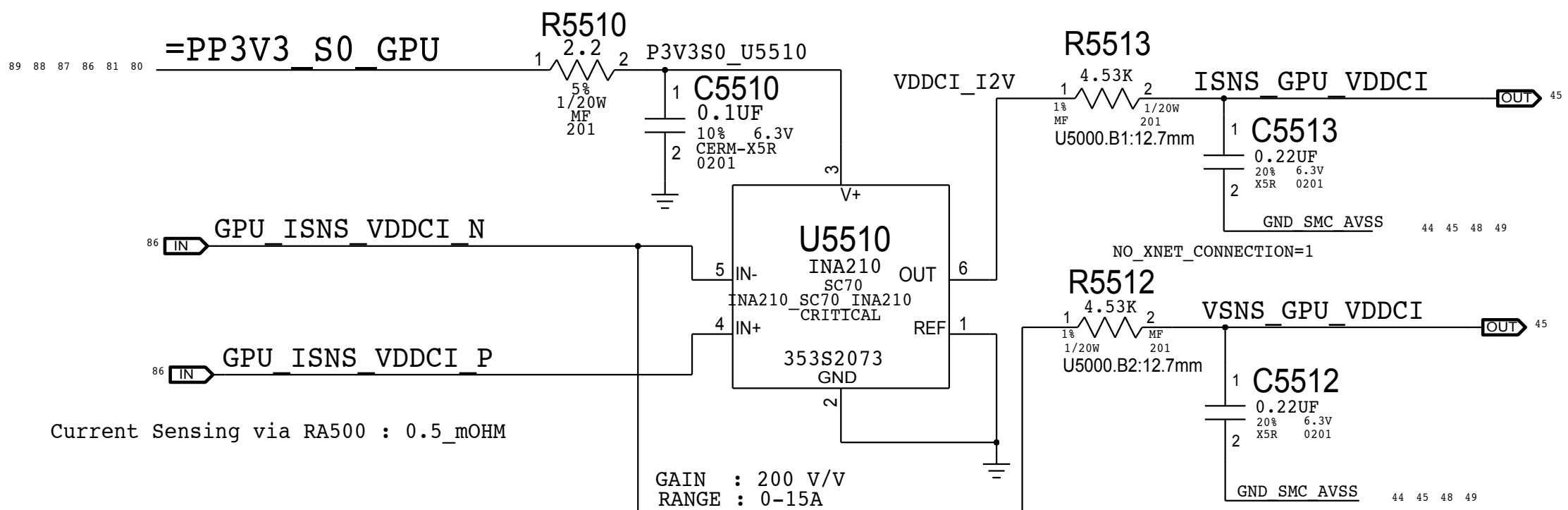
D

VDDQ S3 (VCOM=VM0R, IC0M:ADC9)

VDDQ lowside sense for SO-DIMM modules



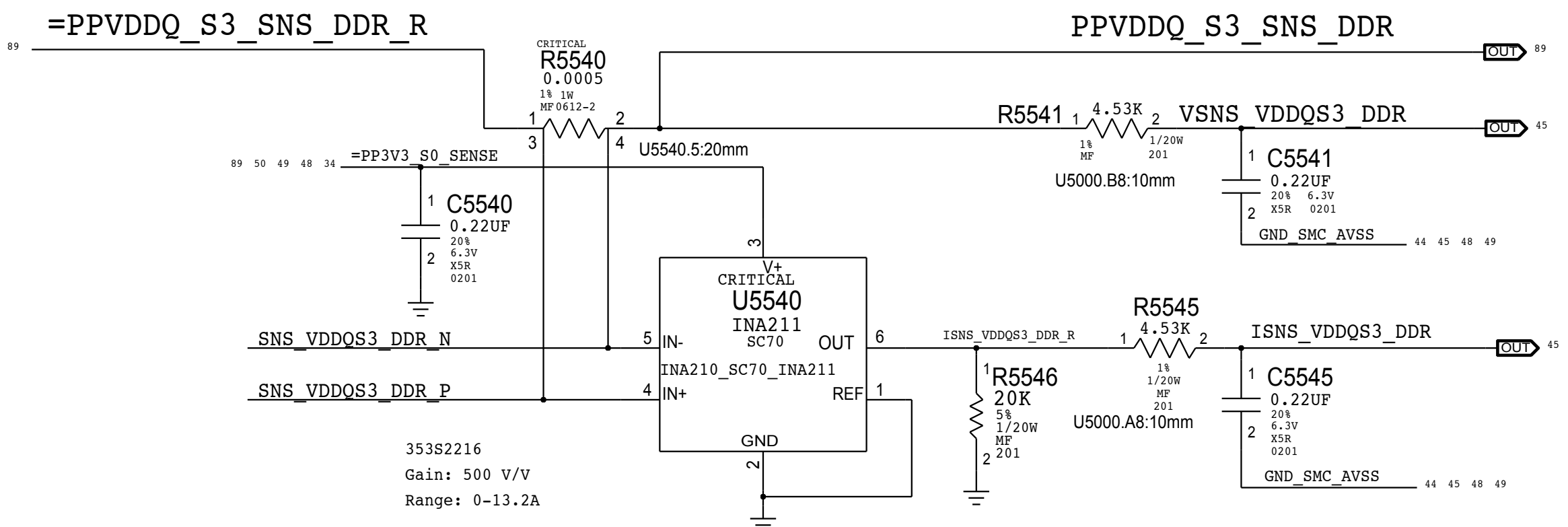
GPU_VDDCI S0 (VG0I:ADC14 /IG0I: ADC15)



C

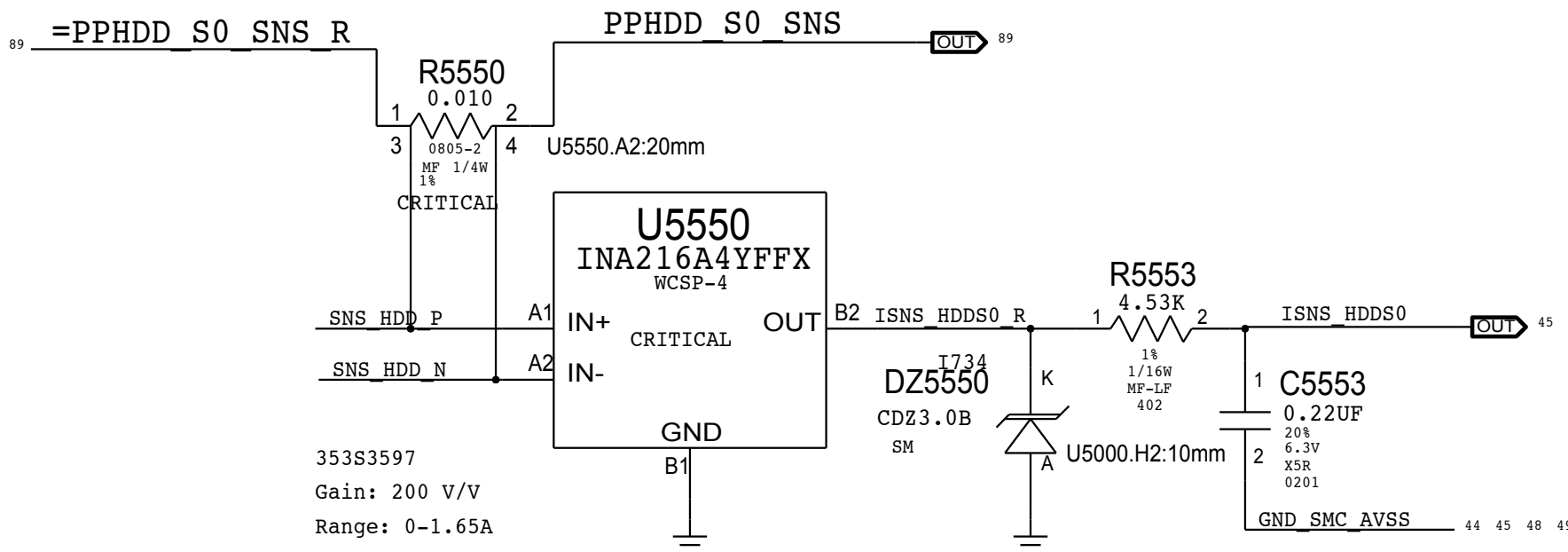
VDDQ S3 (VM0R:ADC22/ IM0R:ADC23)

VDDQ lowside sense for SO-DIMM modules



HDD S0 (VH05=5V, IH05:ADC19)

I/V-sense for HDD 5V

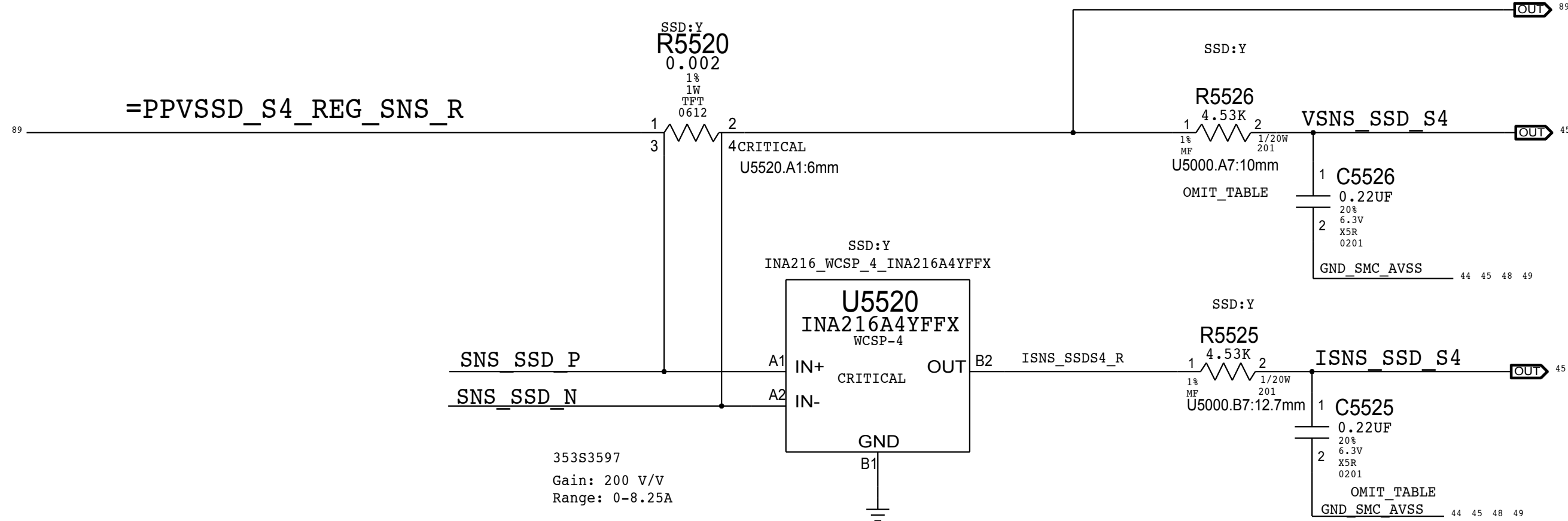


B

SSD S4 (VR1R:ADC20 / IH1R:ADC21)

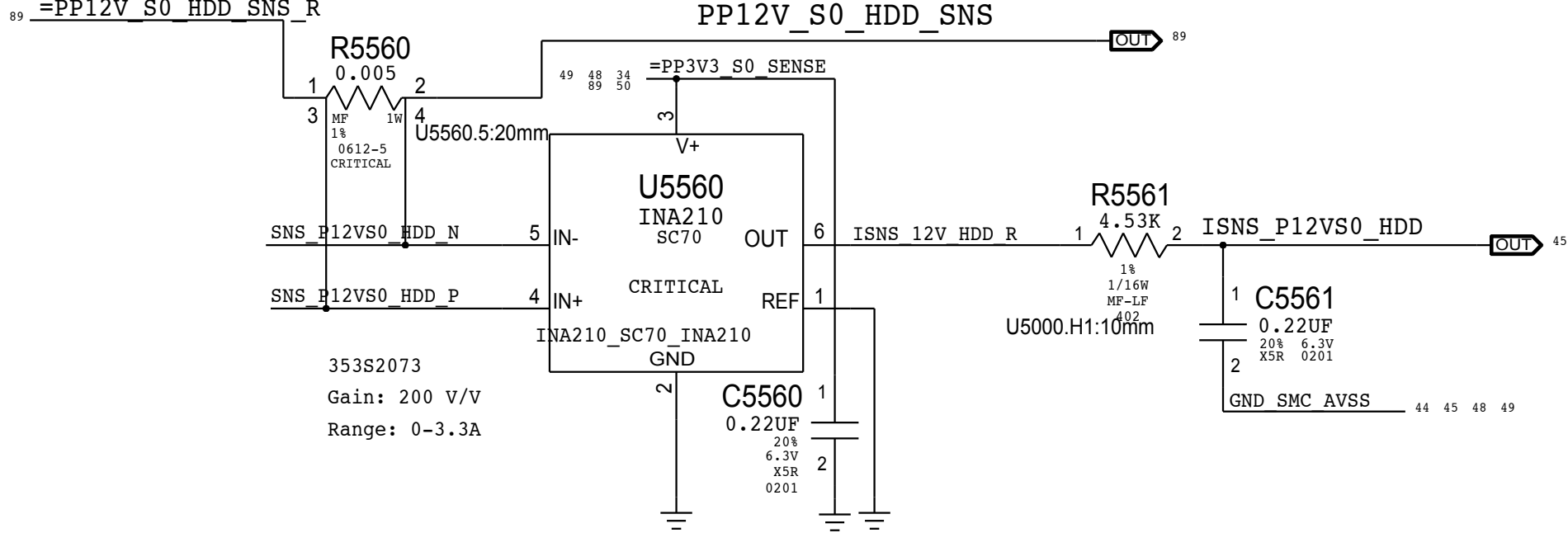
I-SENSE FOR SSD / V-SENSE FOR PPSSD_S4)

PPVSSD_S4_REG_SNS



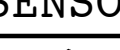
PP12V_S0_HDD (VH02=VD20, IH02:ADC18)

HDD 12V CURRENT SENSE



A

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
13280304	2	CAP, 0.22UF, 201	C5525,C5526	SSD:Y
11780201	2	RES, 0 OHM, 201	C5525,C5526	SSD:N

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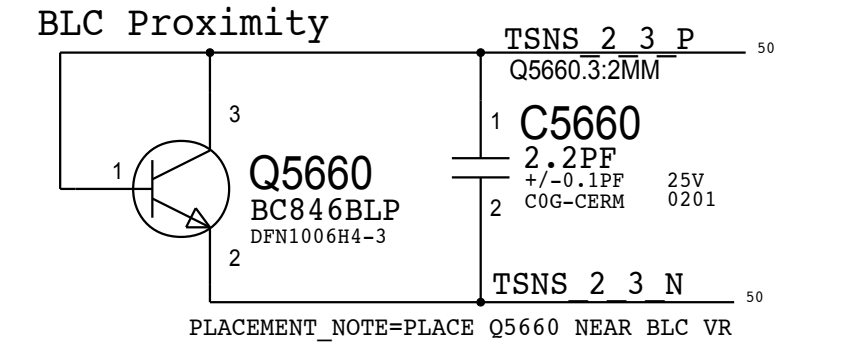
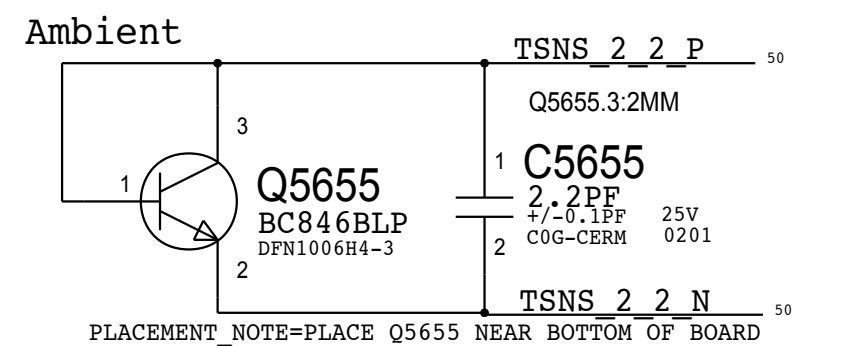
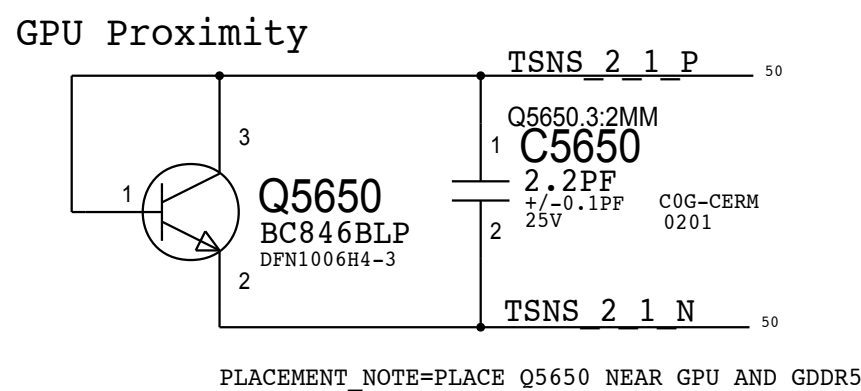
A

D

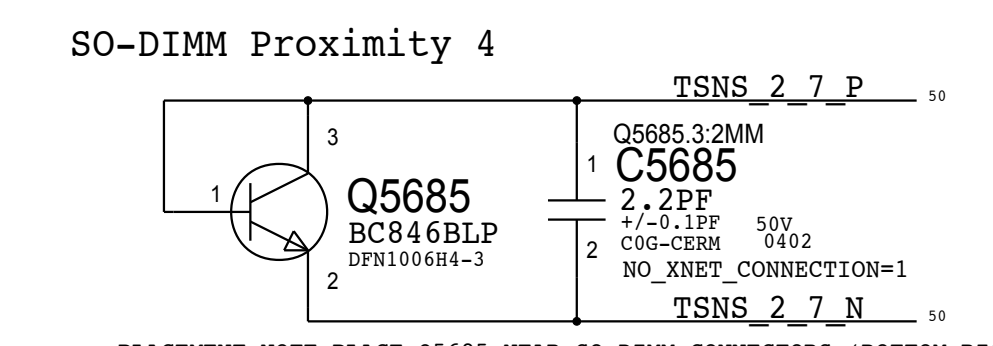
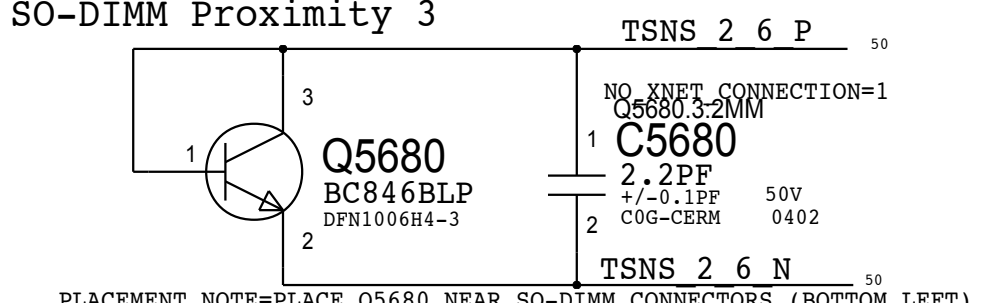
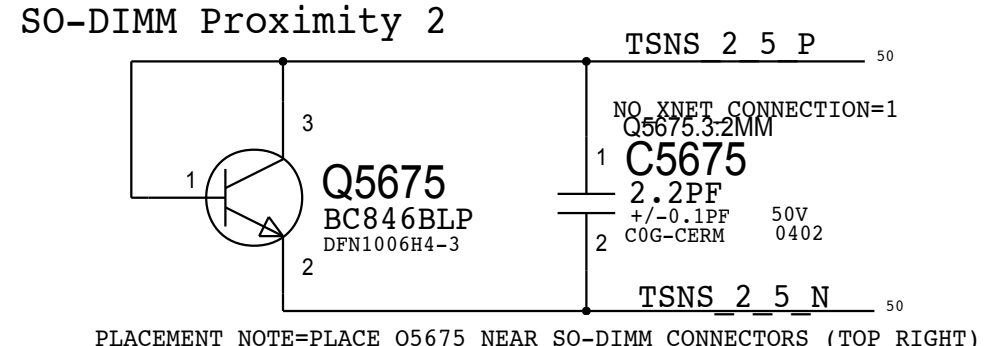
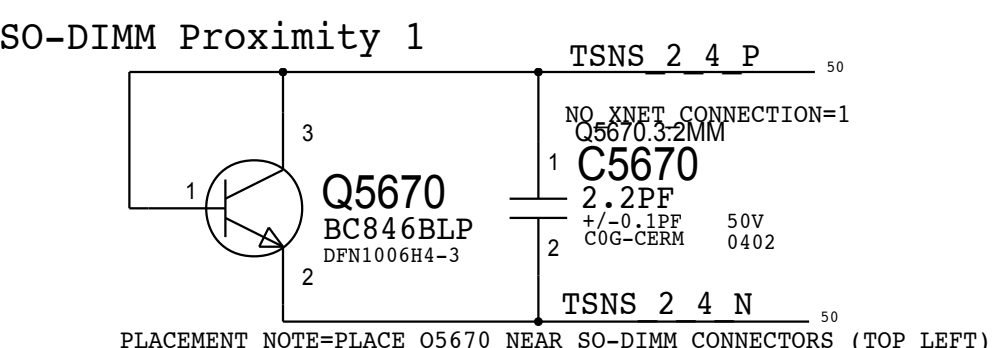
C

B

A

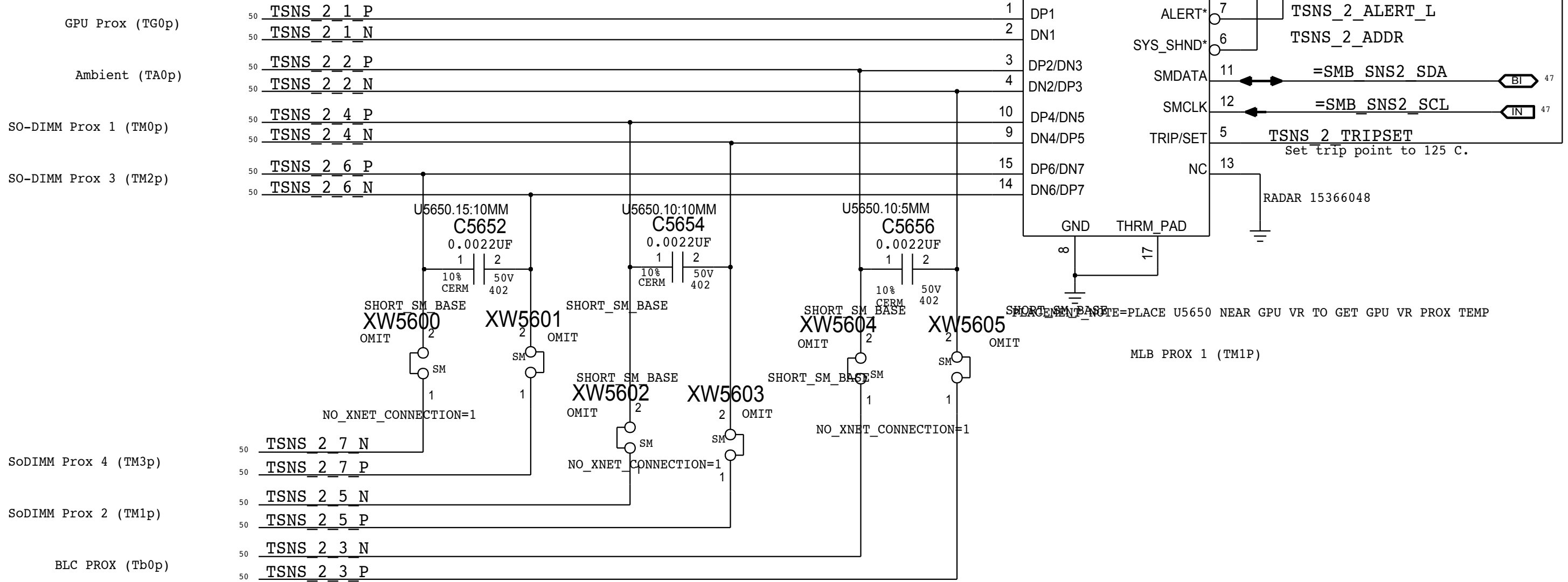


NEED TO FIND LOCATION

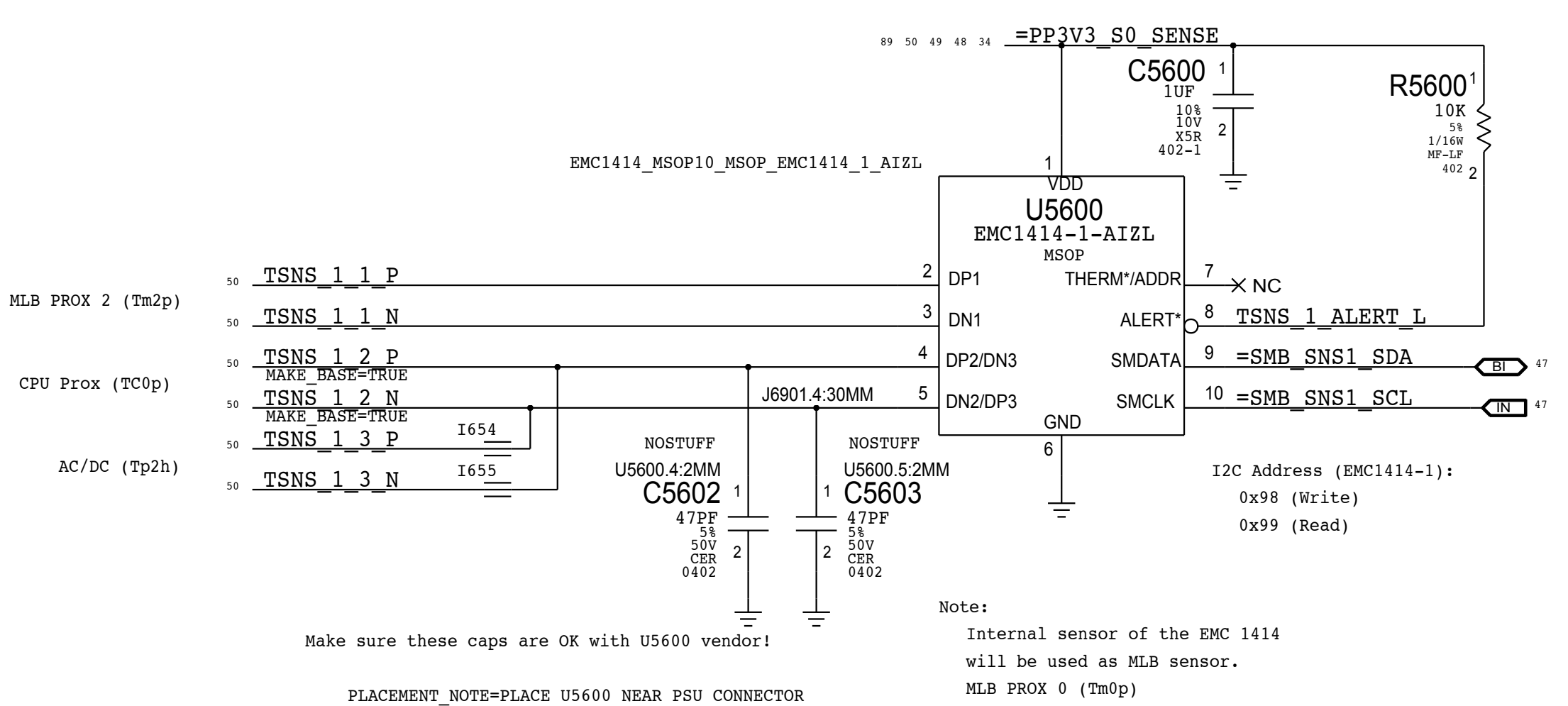
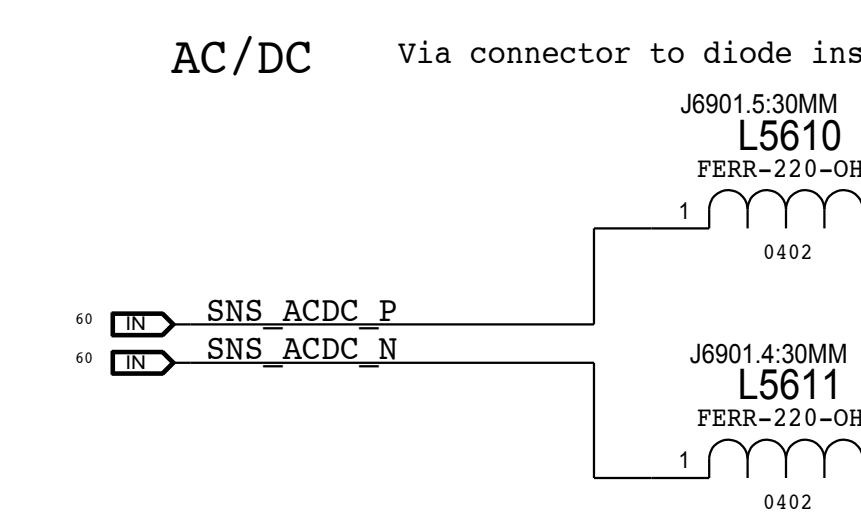
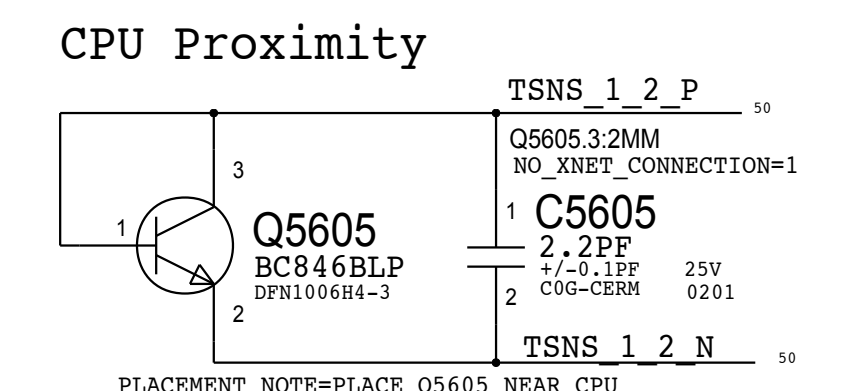
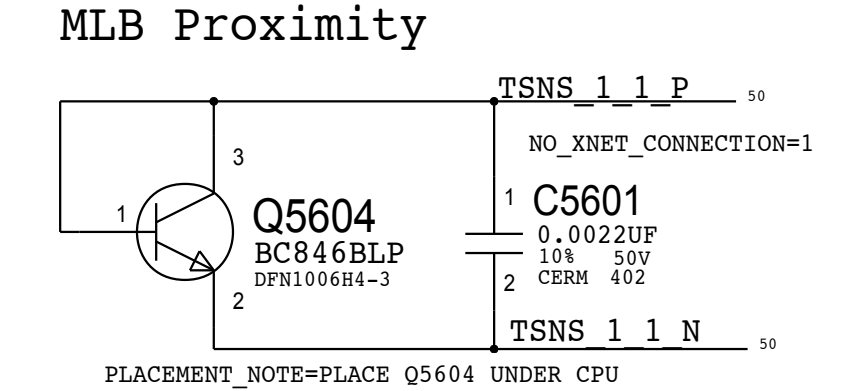


TEMP SENSOR T2 EMC1428: NEAR GPU VR

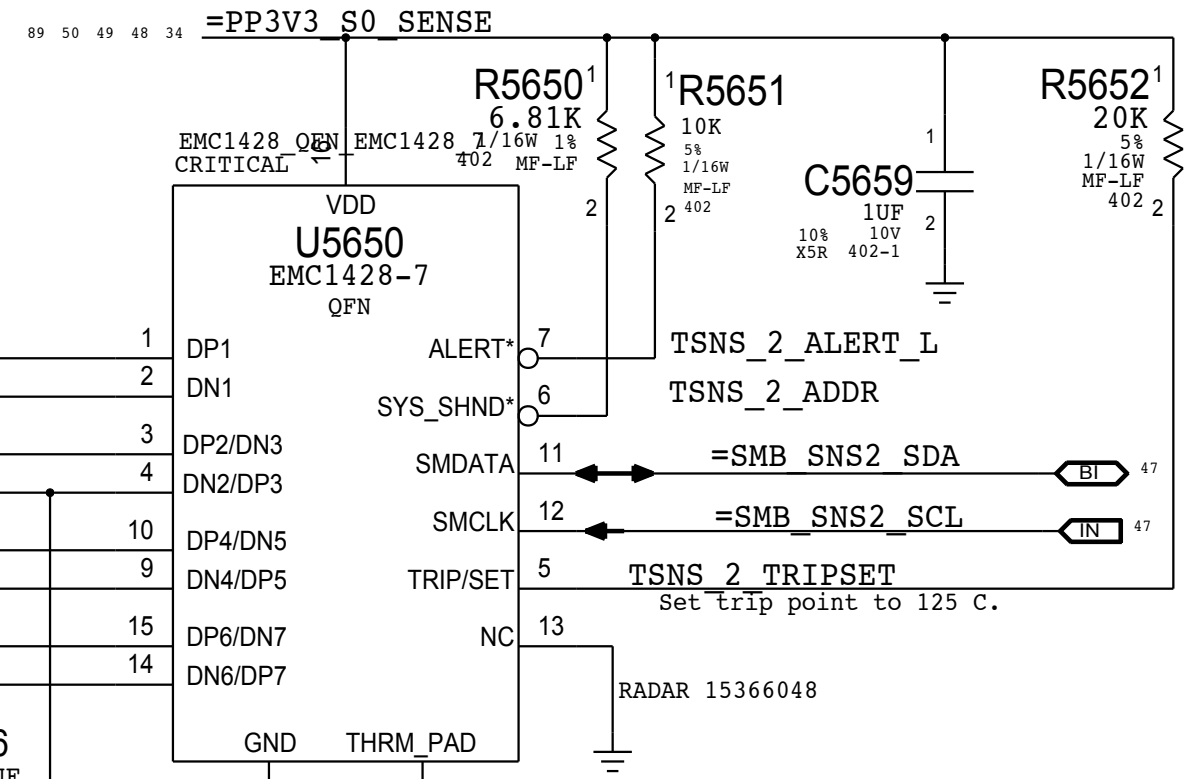
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
372S0186	372S0185		ALL	Alternate Temp Diode



Temperature Sensor T1 EMC1414: Near PSU Conn




SNS T2: TEMP SENSOR IC



PLACE U5650 NEAR GPU VR TO GET GPU VR PROX TEMP

MLB PROX 1 (TM1P)

SYNC_MASTER=BRANCH JERRYCHOW		SYNC_DATE=09/10/2014	
PAGE TITLE			
SENSORS: Temperature Sensors			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-00673		D
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	0.24.0		
	BRANCH		
	PAGE		
	56 OF 121		
SHEET			
50 OF 93			

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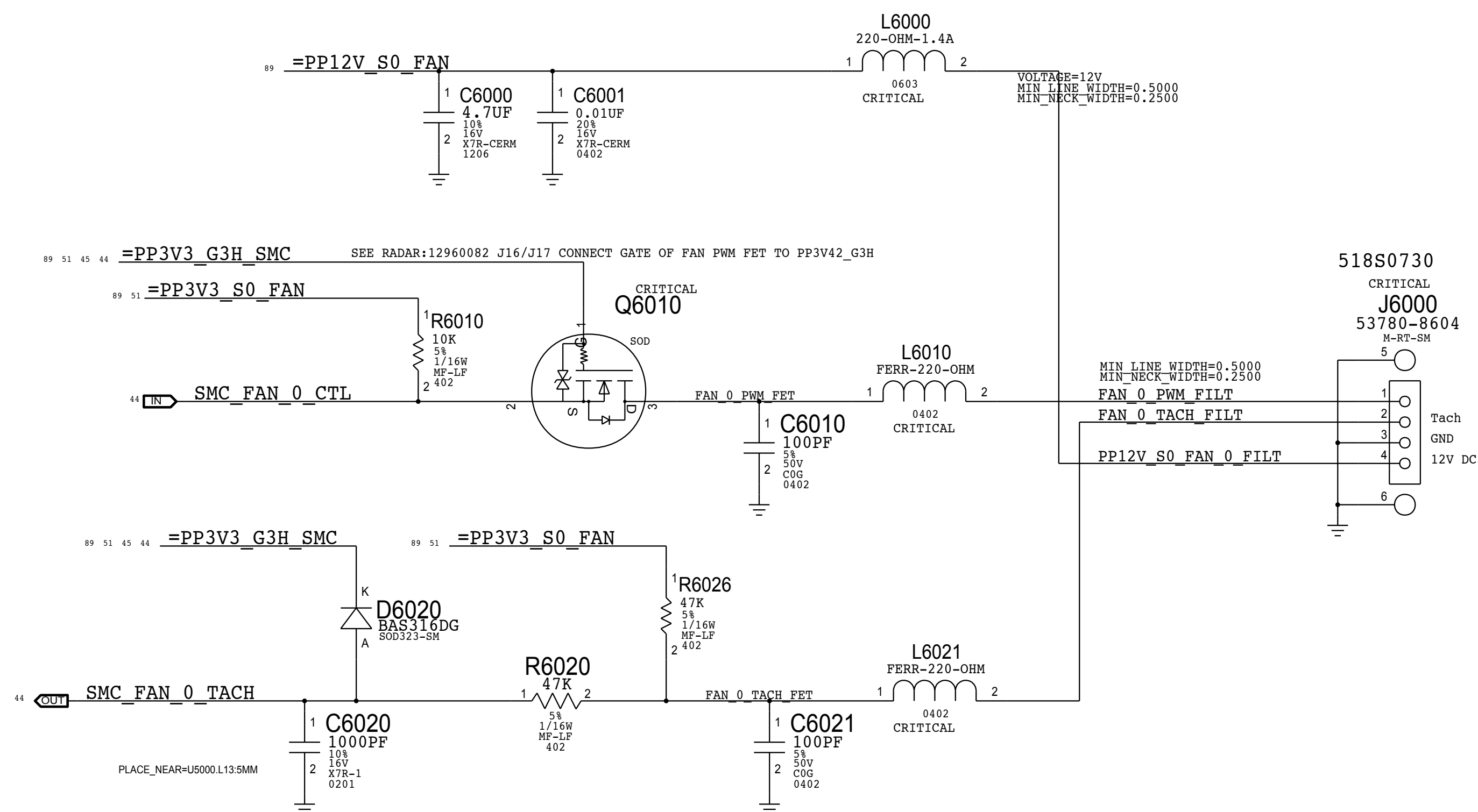
SMC Fan 0 (System)

Note:

The circuit for the PWM input to the fan acts as a non-inverting level-shifter to protect the SMC. It is assumed there is a pull-up to 5V/12V inside the fan, otherwise when the SMC PWM goes low and Q6010 turns on, there would be 5V/12V present on the SMC pin! Then by definition, the drain of Q6010 is at common and the SMC sinks current when Q6010 is on.

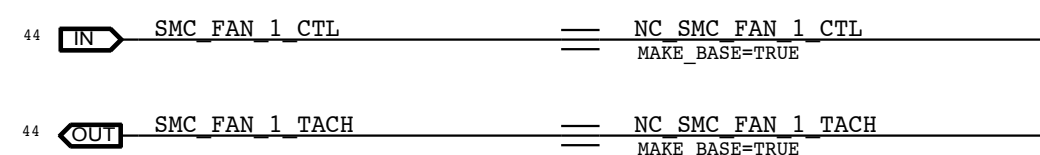
This resembles an open-drain if there is a pull-up, going to a Hi-Z FET input.


Otherwise, this is simply a pass-FET.
See RADAR: 10565825- D7: Need schematic and PCB file of fan(All Vendors).

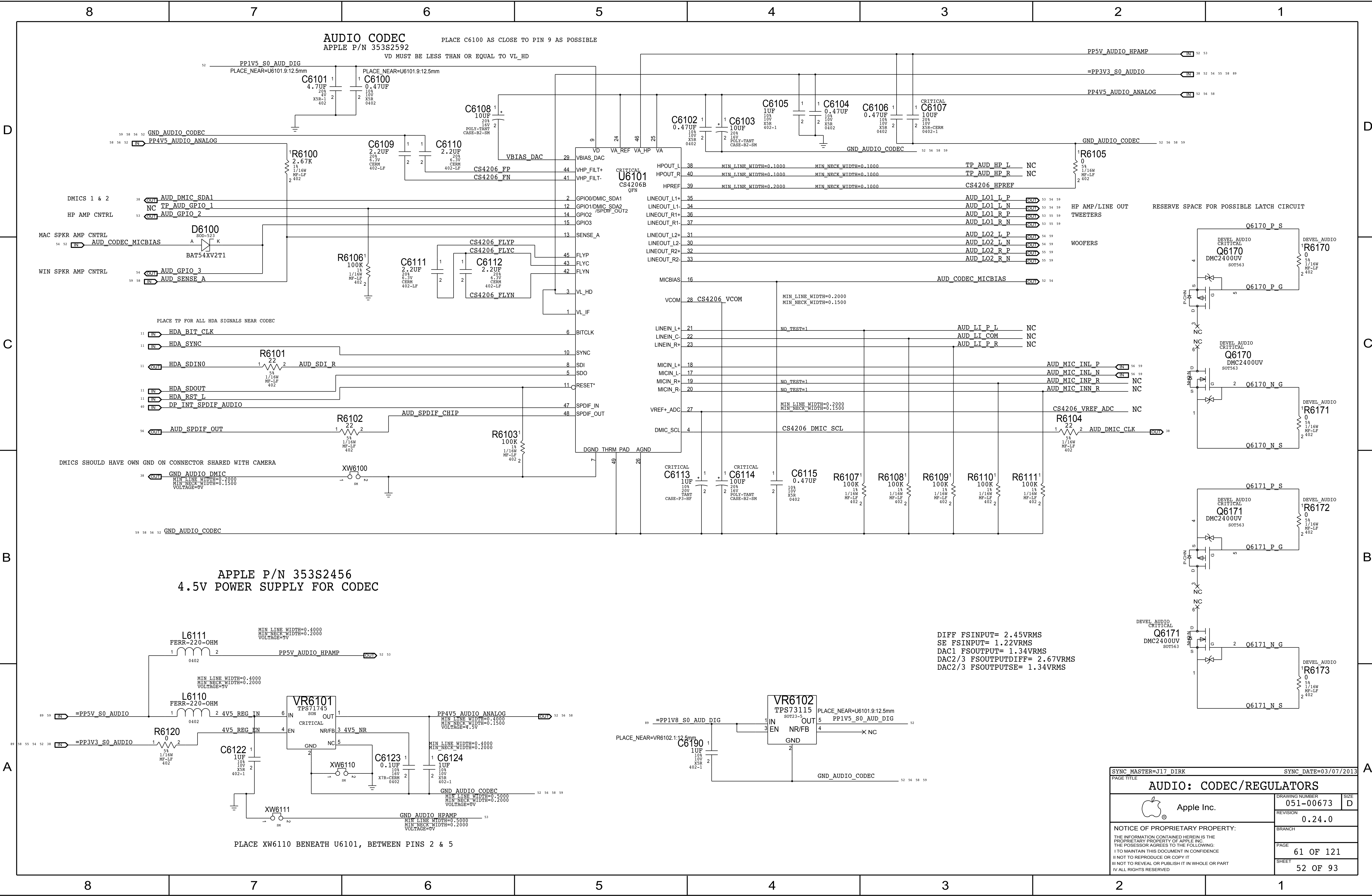



Add C6020 1000pF Cap, Change R6020 to 47K -- Radar 11661918 D8 Protol Fan Tach instability.

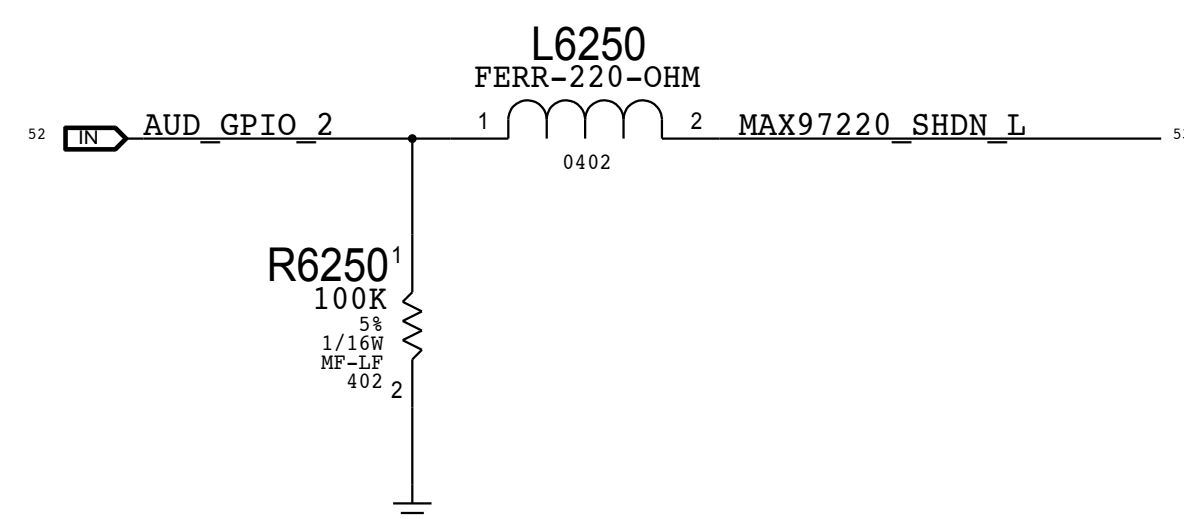
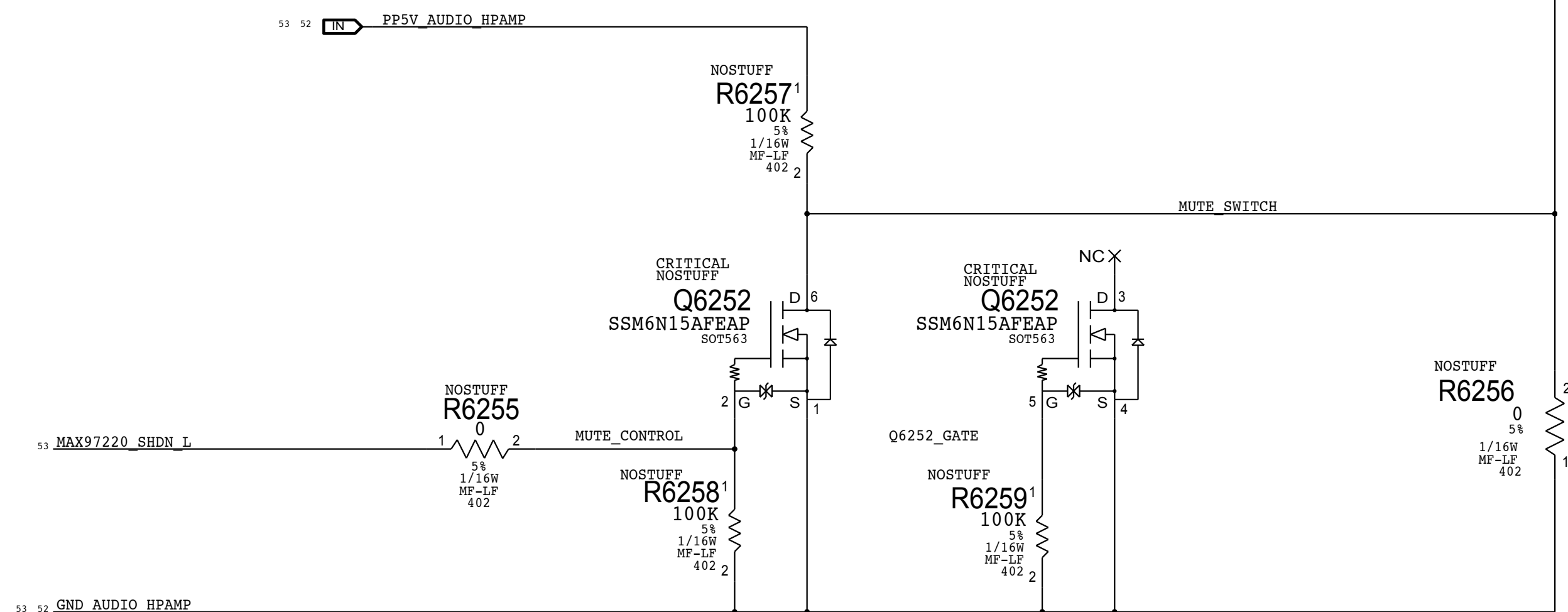
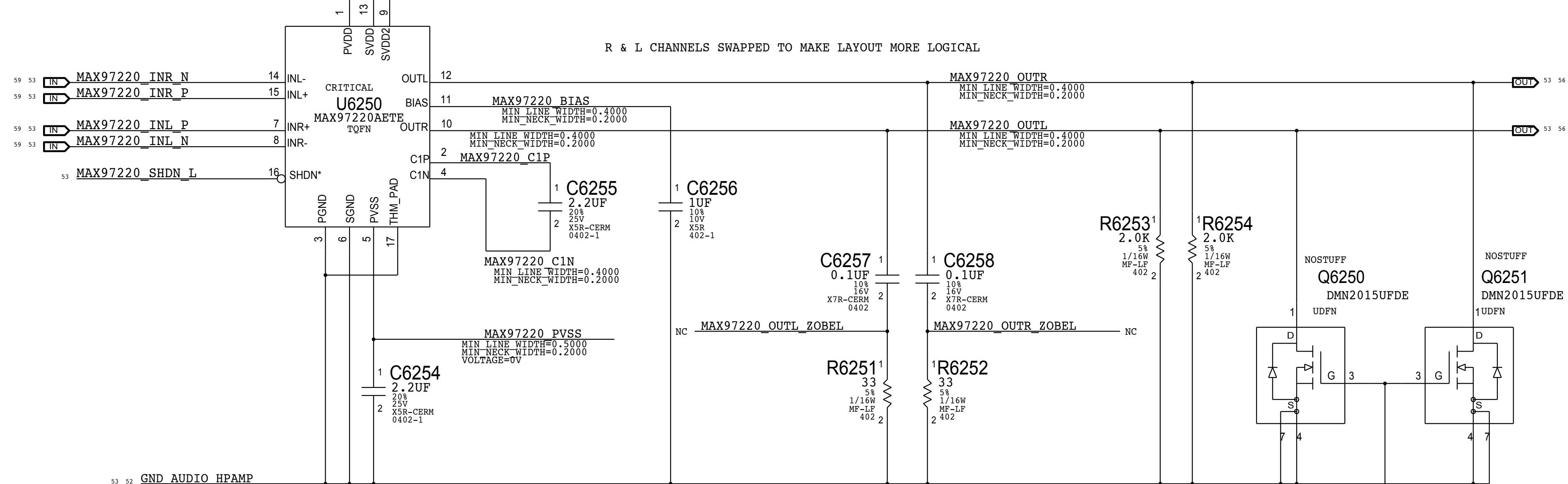
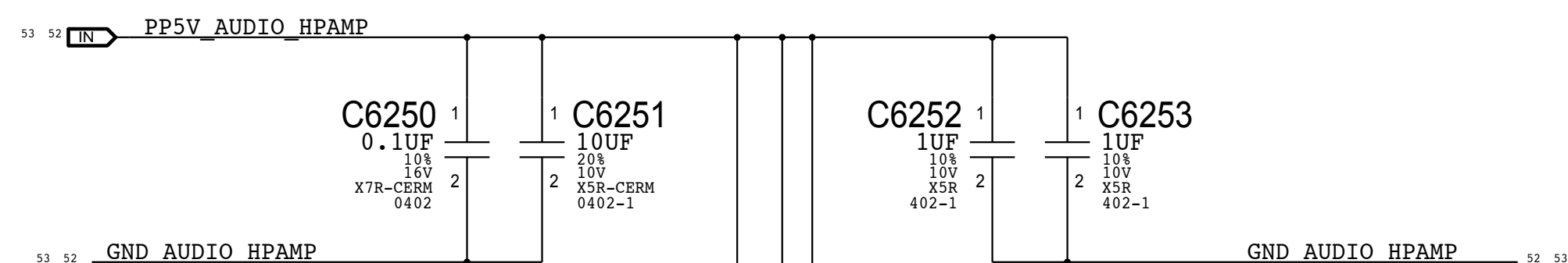
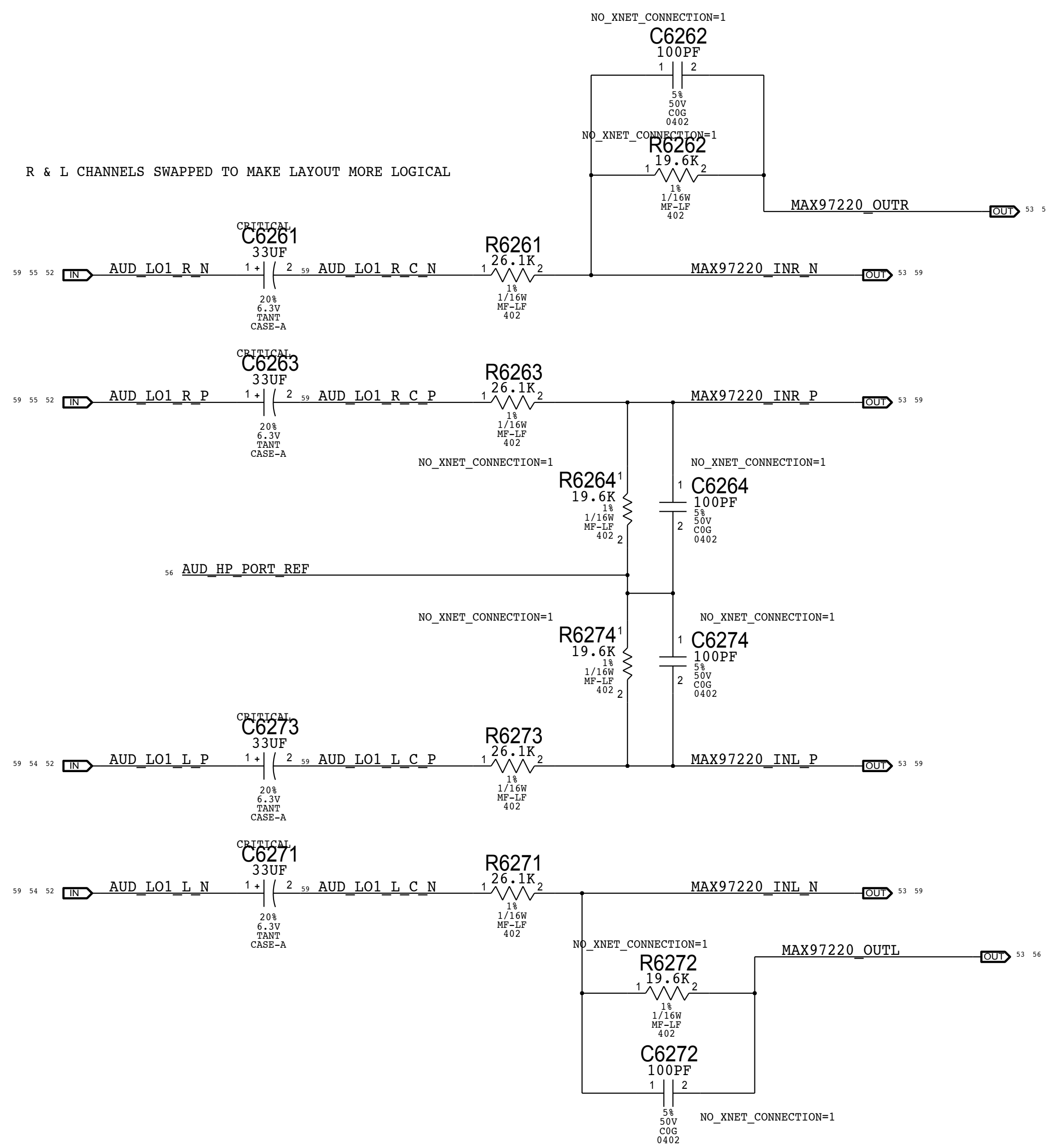
SMC Fan 1 (Unused)




SYNC MASTER=J16 IG		SYNC DATE=04/29/2013	
PAGE TITLE			
FAN: System Fan			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-00673		D
	REVISION		
	0.24.0		
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BRANCH		PAGE	
		60 OF 121	
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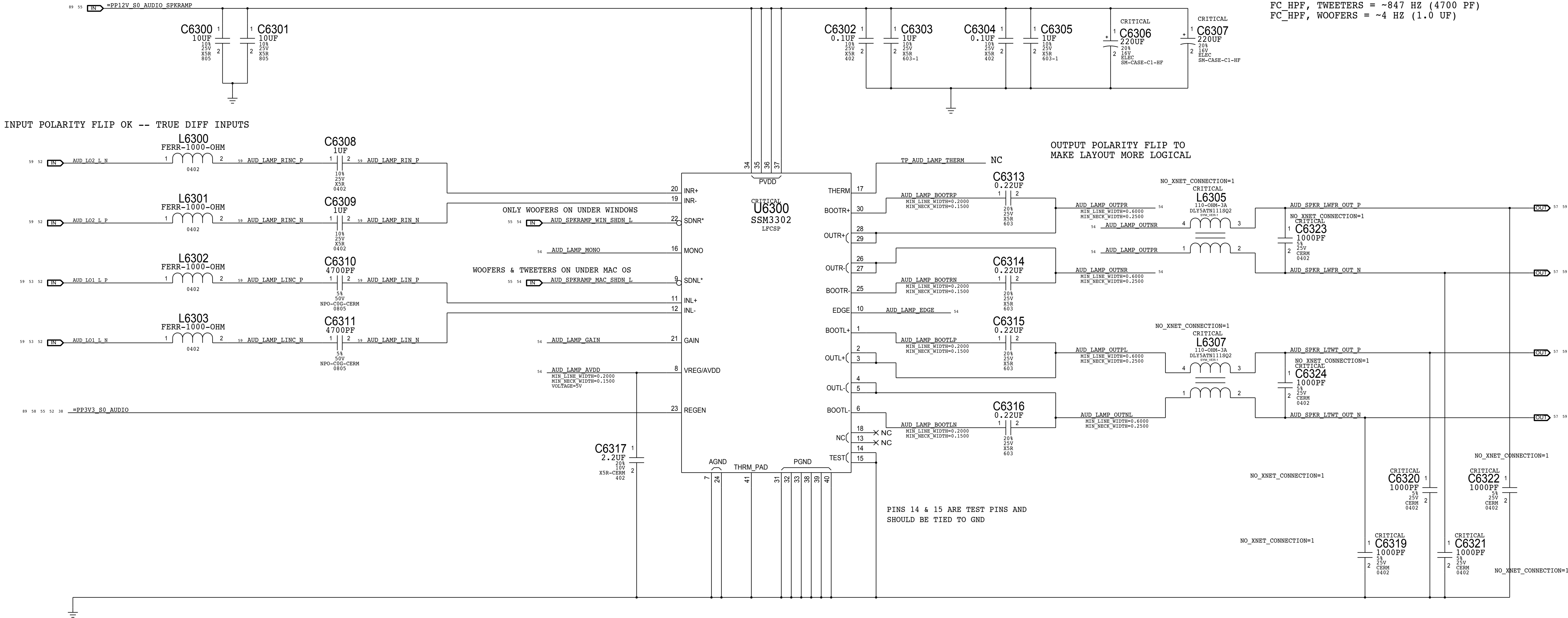
SYNC_MASTER=J17 DIRK		SYNC_DATE=03/07/2013		
PAGE TITLE				
AUDIO: CODEC/REGULATORS				
 Apple Inc.		DRAWING NUMBER	051-00673	D
		REVISION	0.24.0	
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		PAGE	61 OF 121	
		SHEET	52 OF 93	



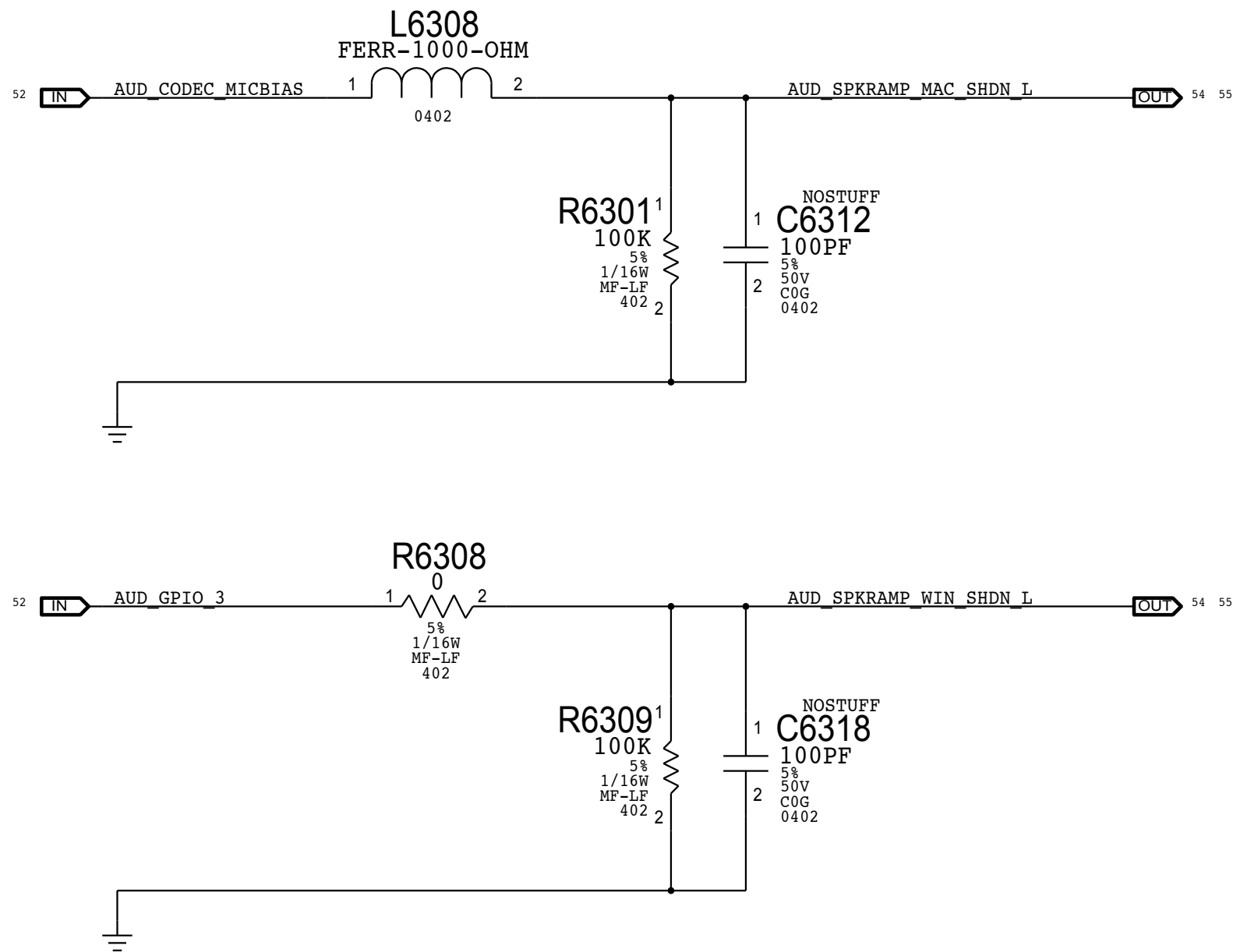
SYNC MASTER=J78 DAVID		SYNC DATE=11/18/2013	
PAGE TITLE			
AUDIO: HEADPHONE AMP			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-00673		D
	REVISION		
			0.24.0
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		53 OF 93	

LEFT CH SPEAKER AMP
APPLE P/N 353S3163

SPEAKER AMP GAIN = +12 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~4 HZ (1.0 UF)



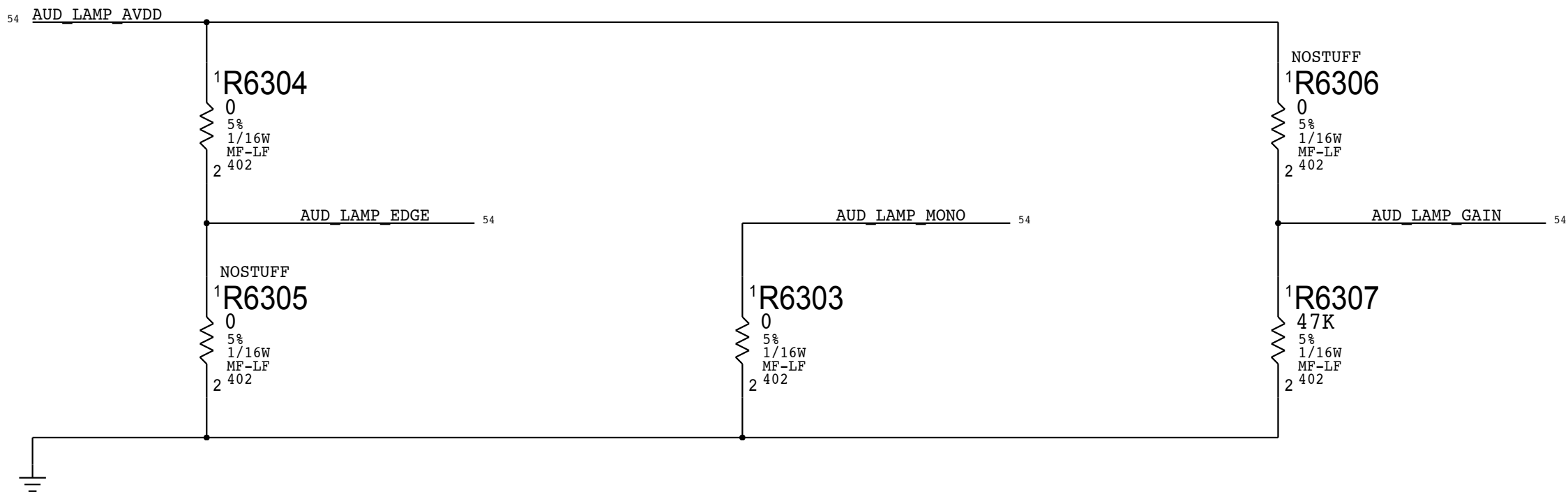
PINS 14 & 15 ARE TEST PINS AND
SHOULD BE TIED TO GND




EDGE RATE
CONTROL R6304 R6305
ON 0 OHM NOSTUFF
OFF NOSTUFF 0 OHM

AUD_RAMP_MONO_NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

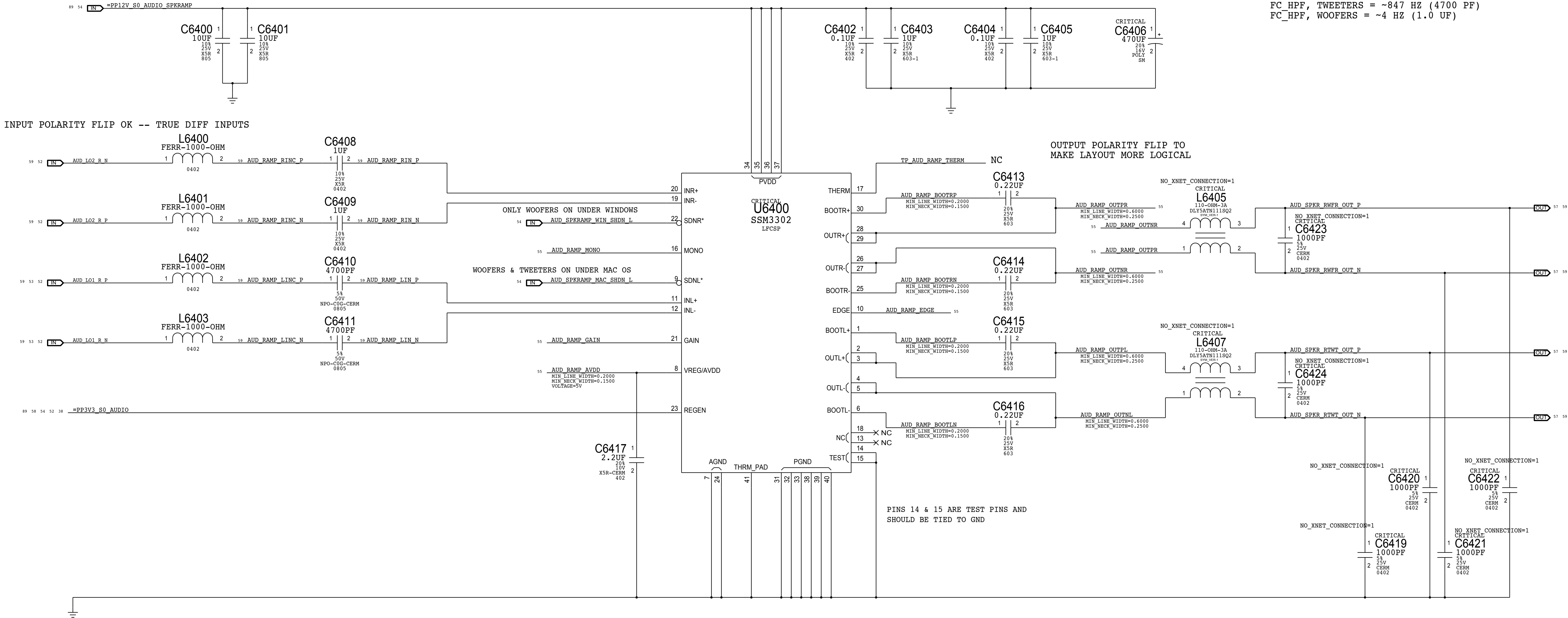
GAIN R6306 R6307
+9 DB NOSTUFF 0 OHM
+12 DB NOSTUFF 47 KOHM
+15 DB NOSTUFF NOSTUFF
+18 DB 47 KOHM NOSTUFF
+24 DB 0 OHM NOSTUFF



SYNC MASTER=J78 DAVID		SYNC DATE=11/18/2013	
PAGE TITLE			
AUDIO: LEFT SPKR AMP			
	DRAWING NUMBER		SIZE
	051-00673		D
REVISION		0.24.0	
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		SHEET	
		54 OF 93	

RIGHT CH SPEAKER AMP
APPLE P/N 353S3163

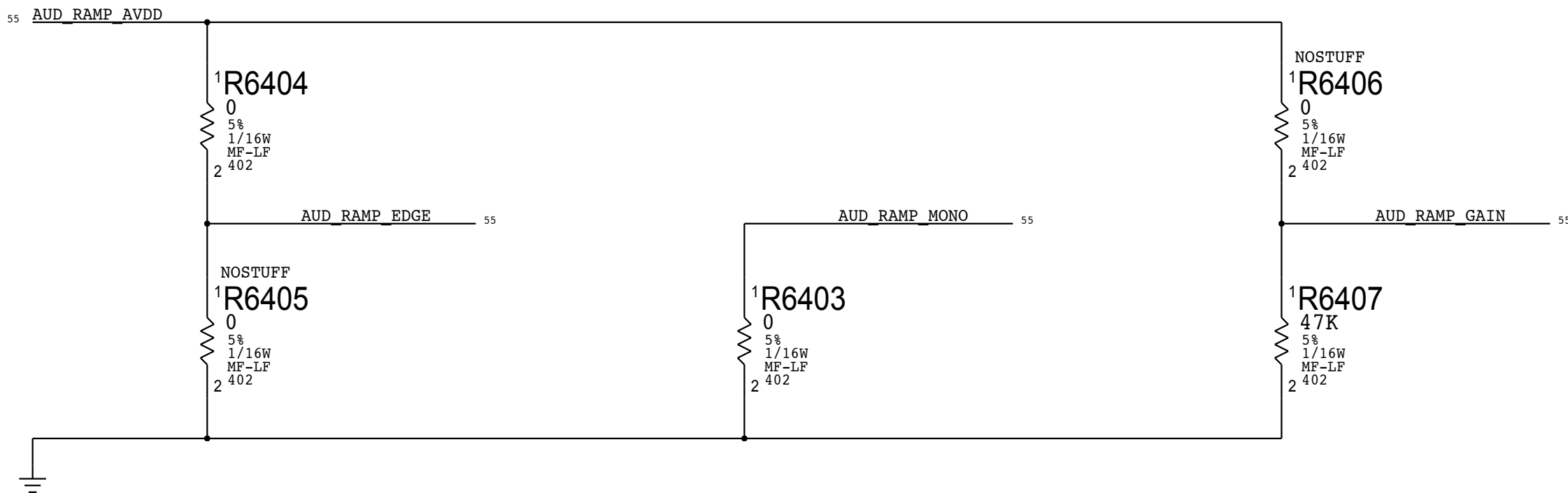
SPEAKER AMP GAIN = +12 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~4 HZ (1.0 UF)




EDGE RATE CONTROL R6404 R6405
ON 0 OHM NOSTUFF
OFF NOSTUFF 0 OHM

AUD_RAMP_MONO_NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

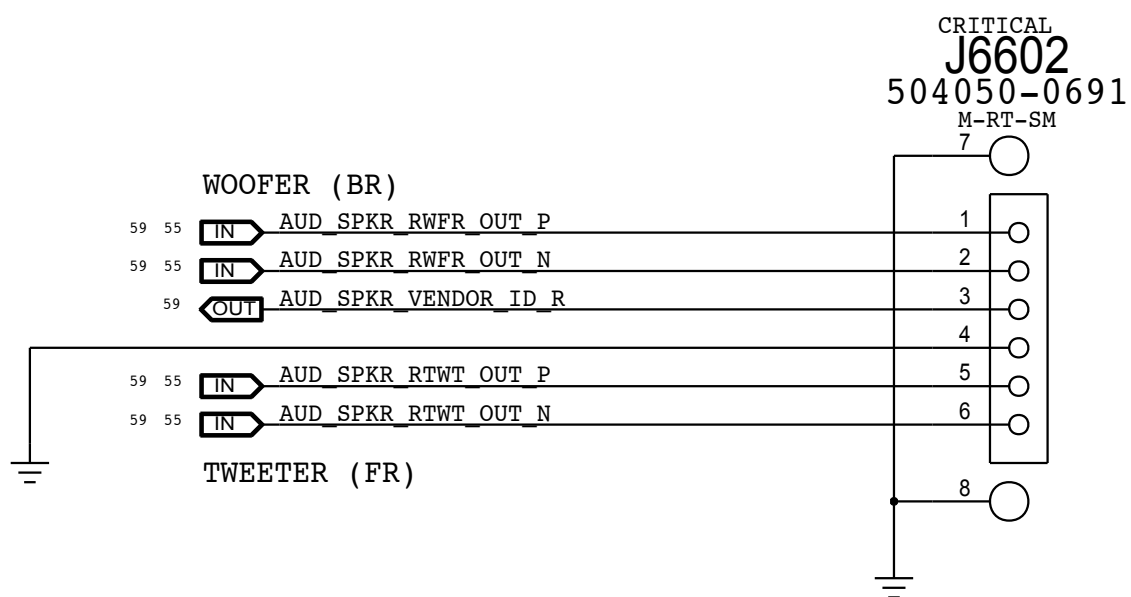
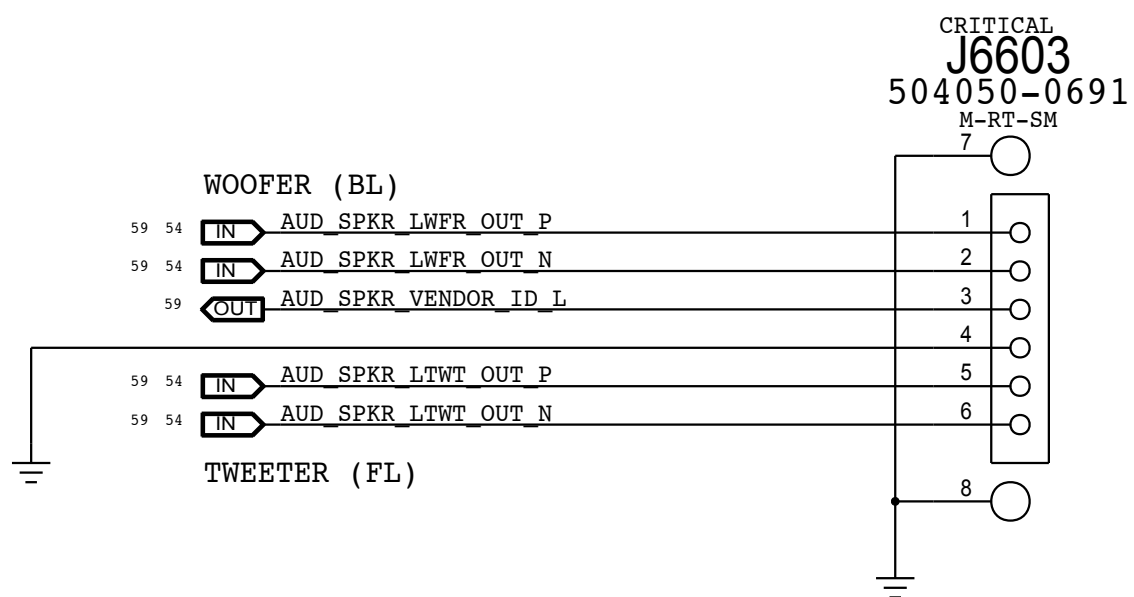
GAIN R6406 R6407
+9 DB NOSTUFF 0 OHM
+12 DB NOSTUFF 47 KOHM
+15 DB NOSTUFF NOSTUFF
+18 DB 47 KOHM NOSTUFF
+24 DB 0 OHM NOSTUFF



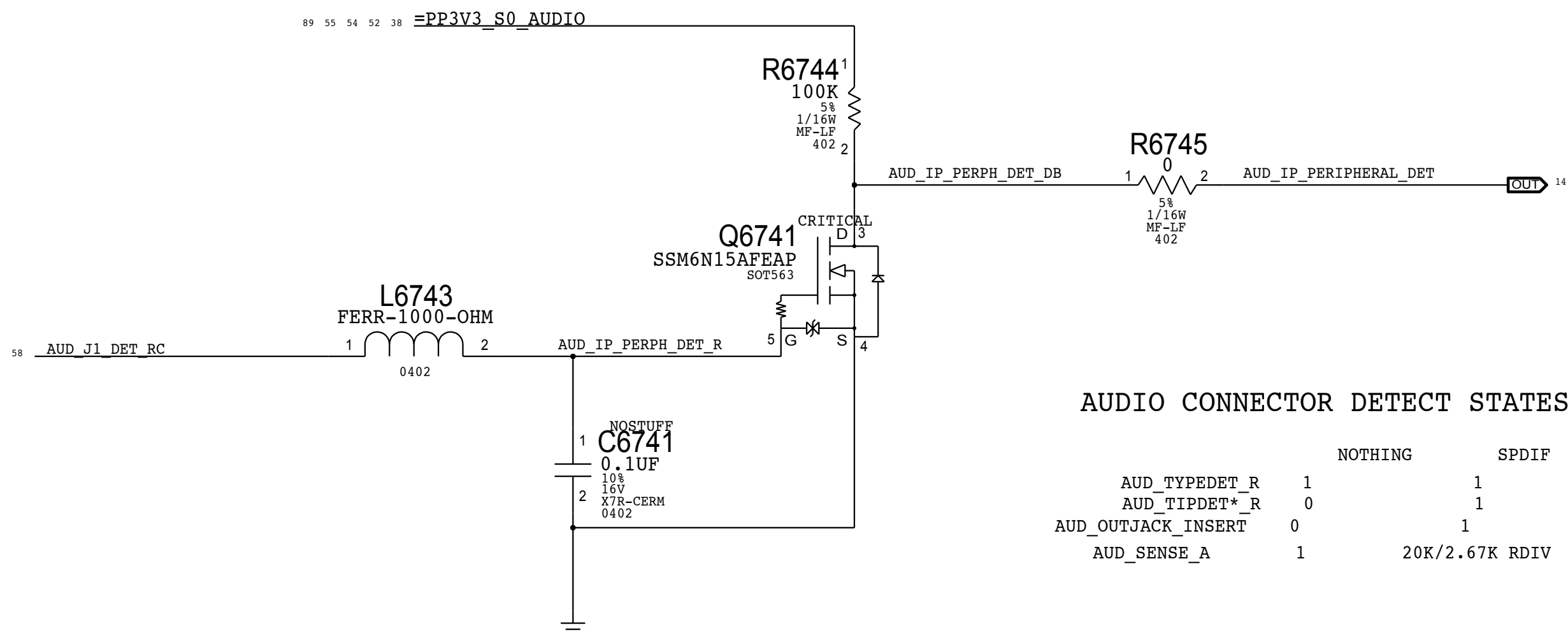
SYNC MASTER=J78 DAVID		SYNC DATE=11/18/2013	
PAGE TITLE			
AUDIO: RIGHT SPKR AMP			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-00673		D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	REVISION		0.24.0
	BRANCH		
	PAGE		
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SPEAKER CABLE CONNECTORS

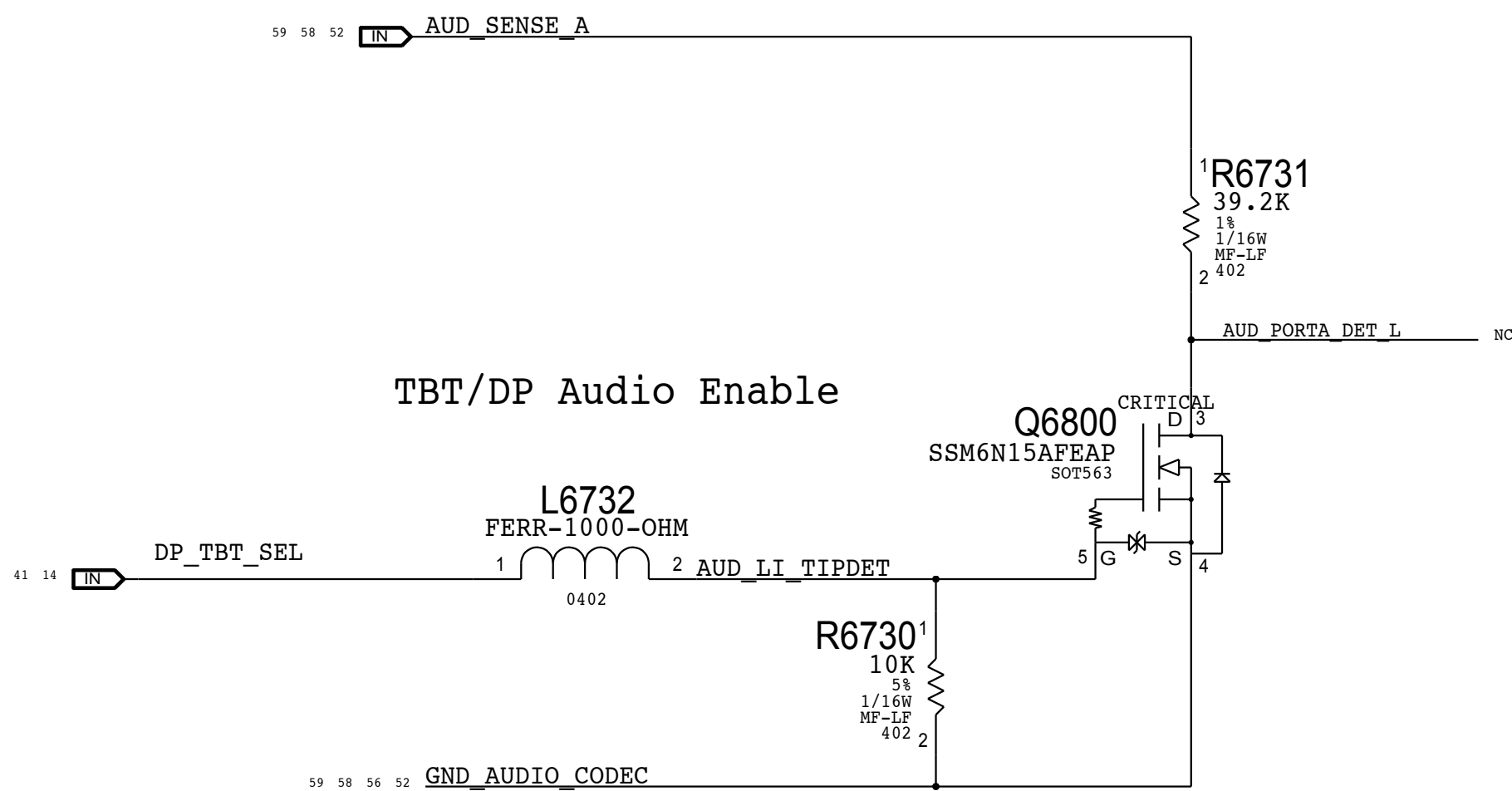
APPLE P/N 518S0862



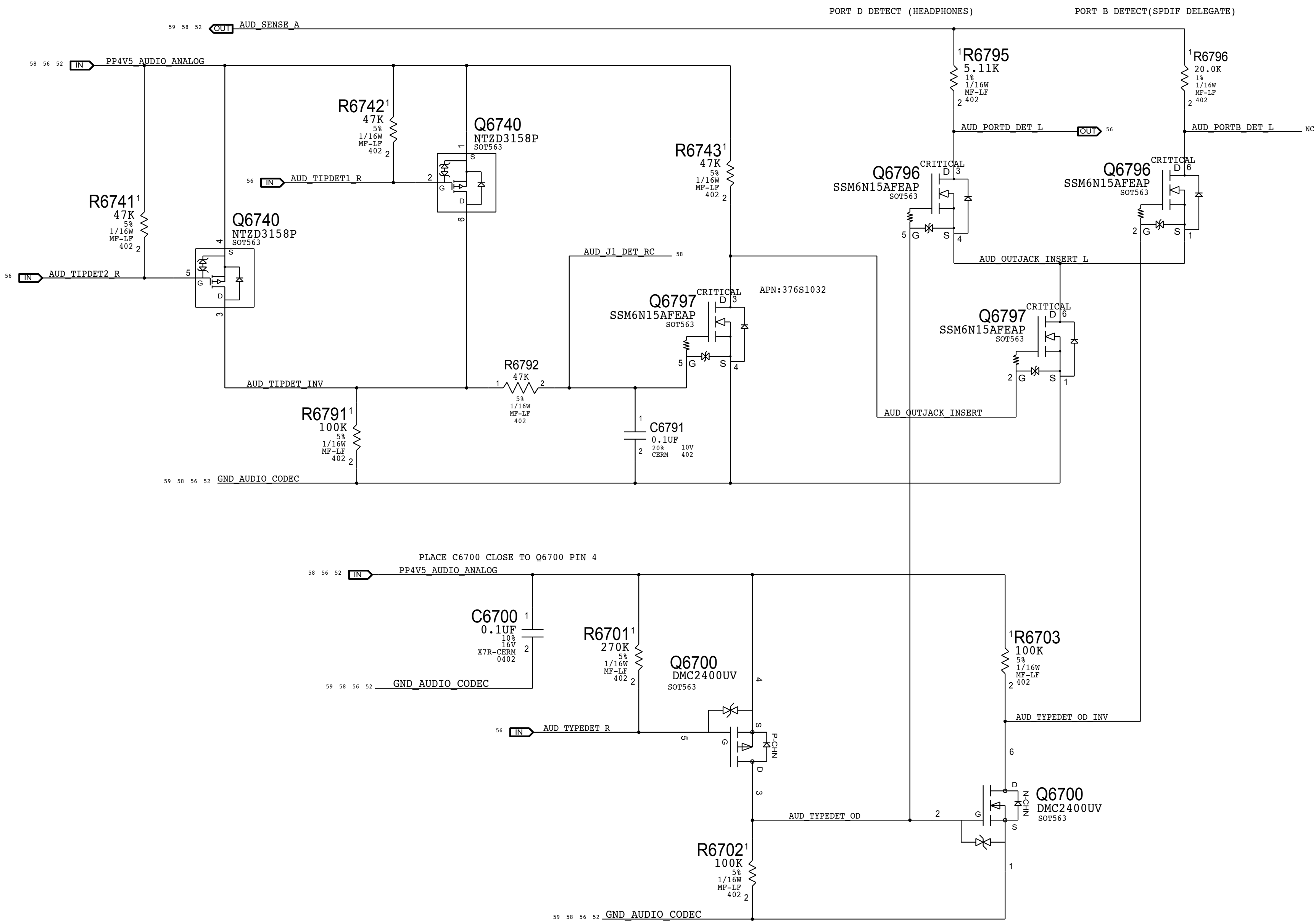
IPHS HS Detect Debounce CKT



Target Display Mode Detect



TBT/DP Audio Enable



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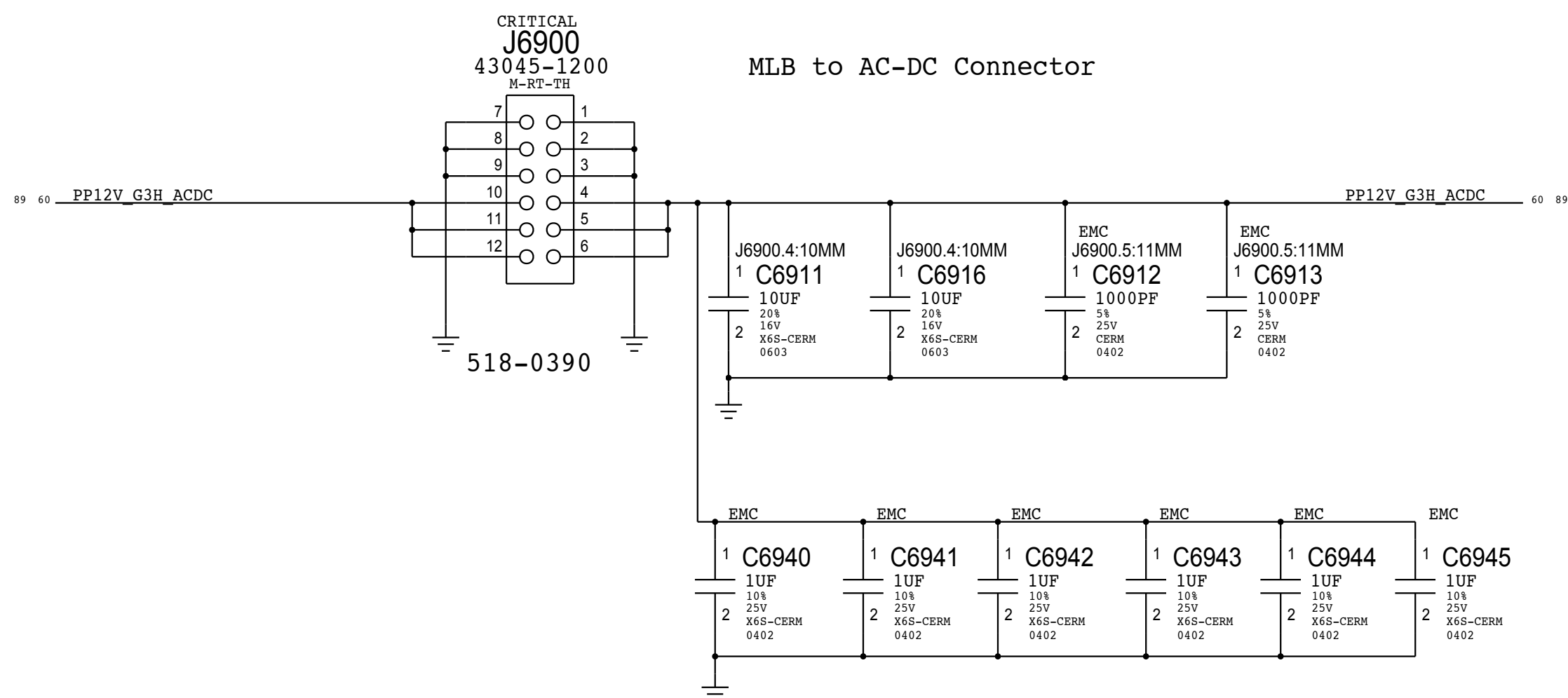
A

D

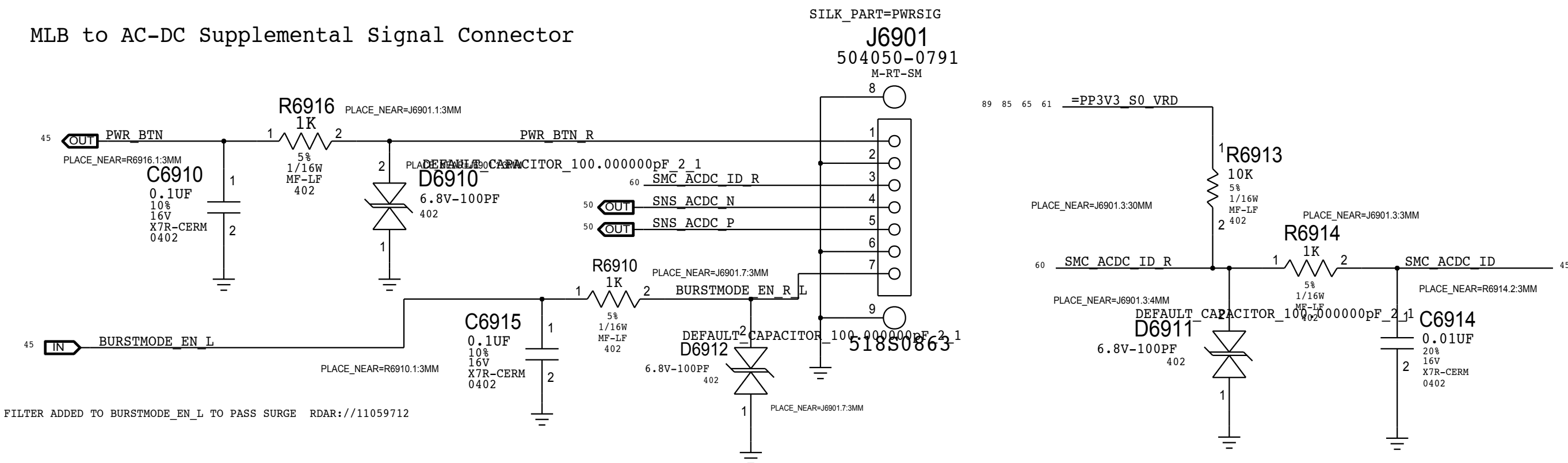
C

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A

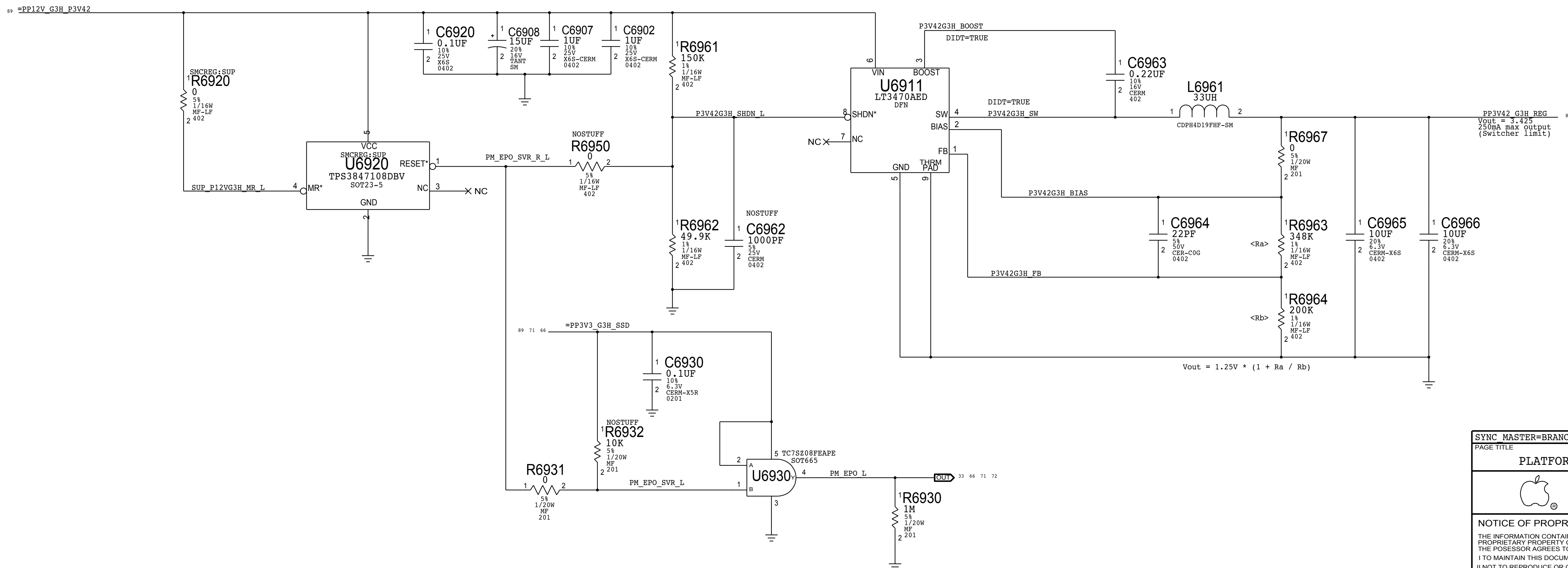



MLB to AC-DC Supplemental Signal Connector

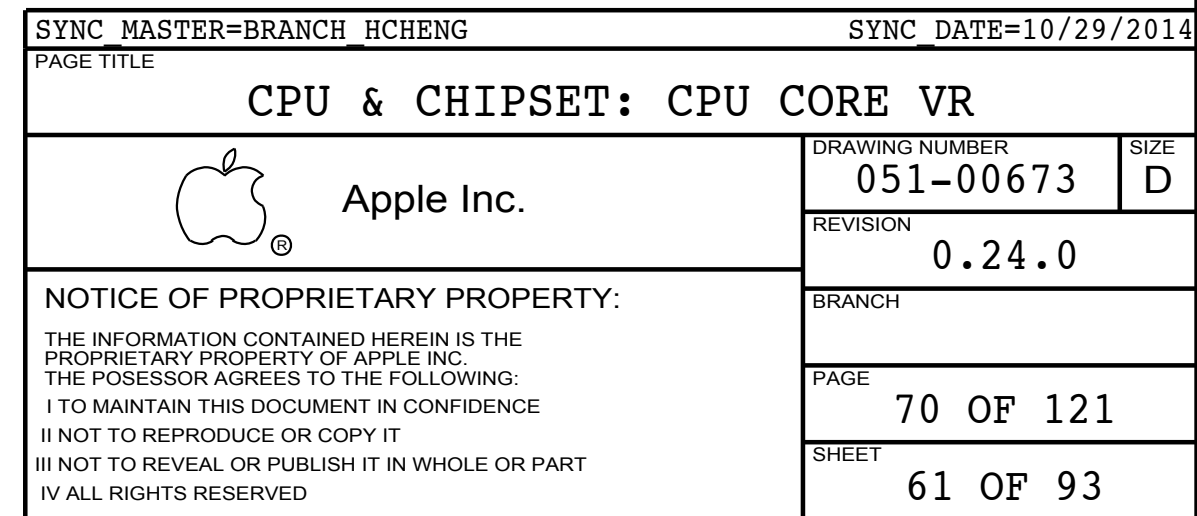


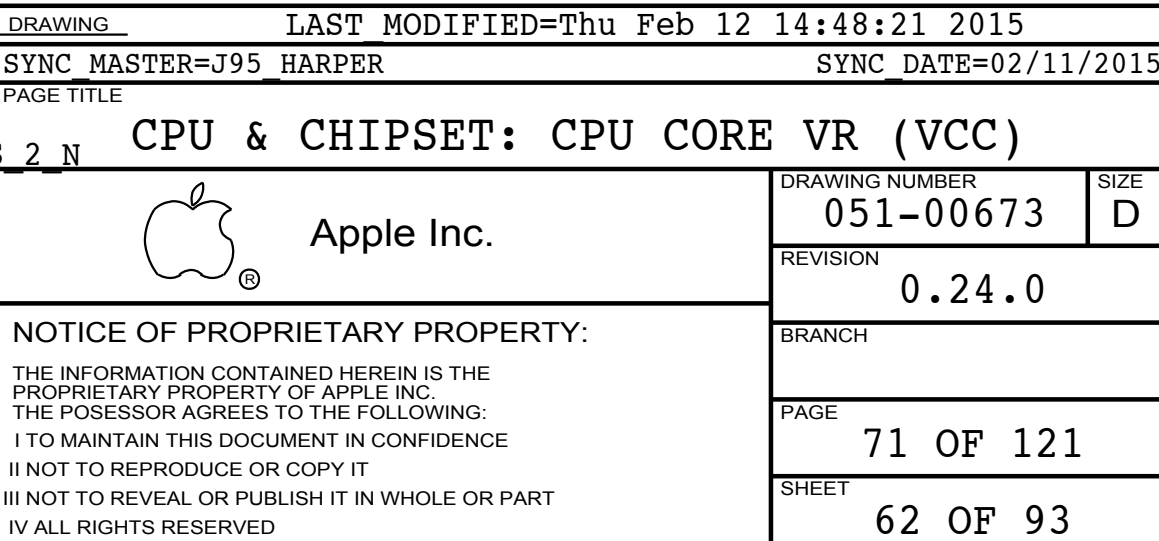
3.425V "G3Hot" Regulator

Max avg current: 0.04 A (BUDGET)
Max peak current: 0.10 A (BUDGET)



SYNC_MASTER=BRANCH_HCHENG		SYNC_DATE=10/29/2014	
PAGE TITLE			
PLATFORM POWER: Connectors / VReg G3Hot			
 Apple Inc.	DRAWING NUMBER 051-00673		SIZE D
	REVISION 0.24.0		
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		SHEET 60 OF 93	





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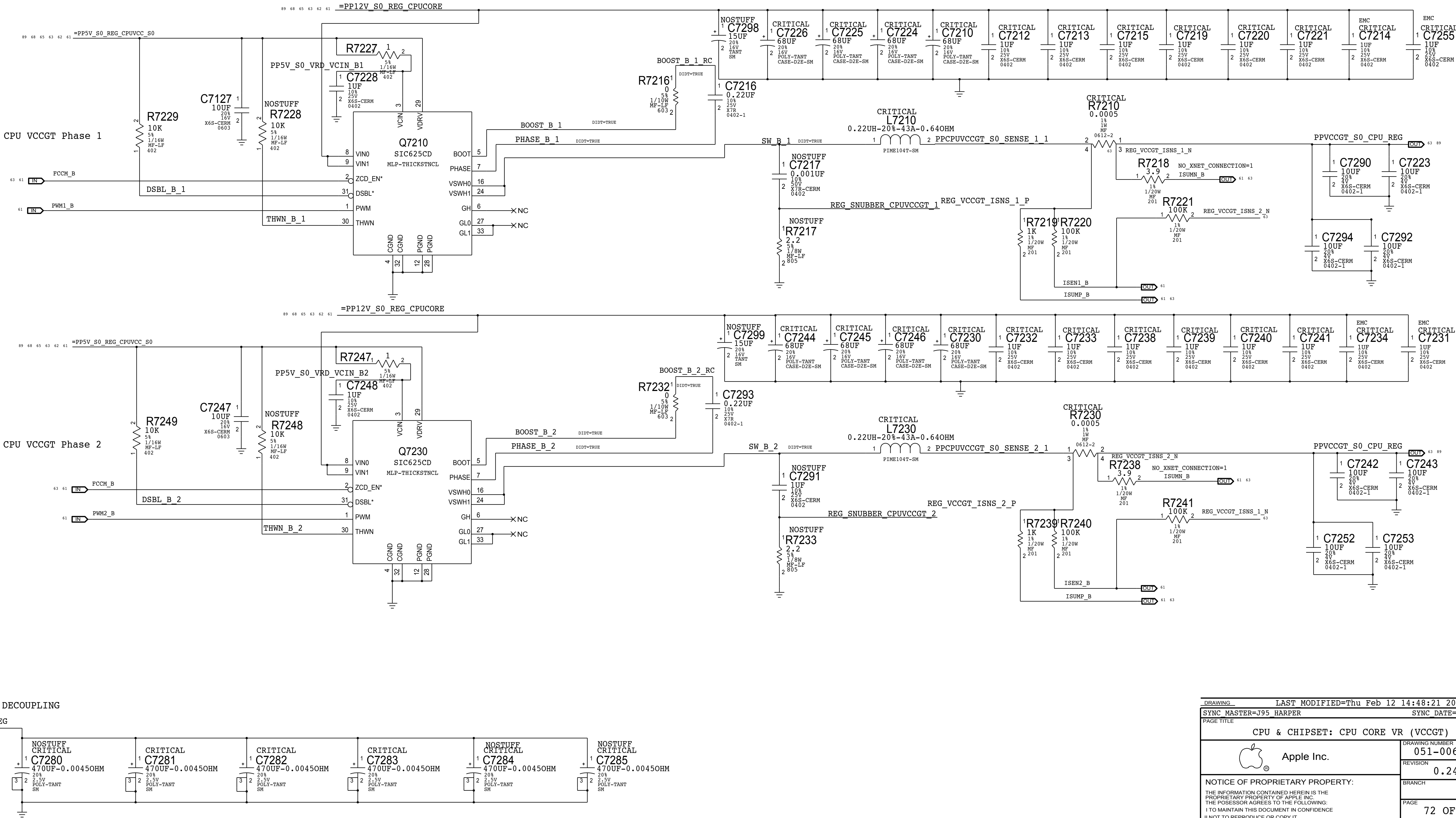
2


1

CPU VCCGT Regulator

EDC = 51A

TDC = 37A



DRAWING	LAST MODIFIED=Thu Feb 12 14:48:21 2015		
SYNC MASTER=J95 HARPER	SYNC DATE=02/11/2015		
PAGE TITLE	CPU & CHIPSET: CPU CORE VR (VCCGT)		
 Apple Inc.	DRAWING NUMBER	051-00673	SIZE
	REVISION	0.24.0	D
	BRANCH		
	PAGE	72 OF 121	
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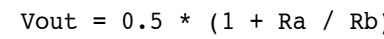
C

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SYNC MASTER=BRANCH HCHENG		SYNC DATE=10/29/2014	
PAGE TITLE			
CPU & CHIPSET: CPU VDDQ VR			
 Apple Inc.		DRAWING NUMBER	SIZE
		051-00673	D
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			0.24.0
		BRANCH	
		PAGE	73 OF 121
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EDC = 5.5A
TDC = 5.5A



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
12880358	2	CAP, 470uF, 0.0060HM, 2V, D2	C7540, C7541	VR_BULKCAP:CURRENT
12880381	2	CAP, 470uF, 0.00450HM, 2.5V, SM	C7540, C7541	VR_BULKCAP:FUTURE

DRAWING _____		LAST MODIFIED=Thu Feb 12 14:48:22 2015	
SYNCH MASTER=378_MLB		SYNCH DATE=08/02/2014	
PAGE TITLE			
CPU & CHIPSET: CPU VCCIO VR			
 Apple Inc.	DRAWING NUMBER 051-00673		SIZE D
	REVISION 0.24.0		
	BRANCH		
NOTICE OF PROPRIETARY PROPERTY:			
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PAGE		75 OF 121	
SHEET		65 OF 93	

3.3V S5 Regulator

EDC = 12.46A


TDC = 9.4A

5V S4 Regulator

EDC = 6.5A

TDC = 5.9A

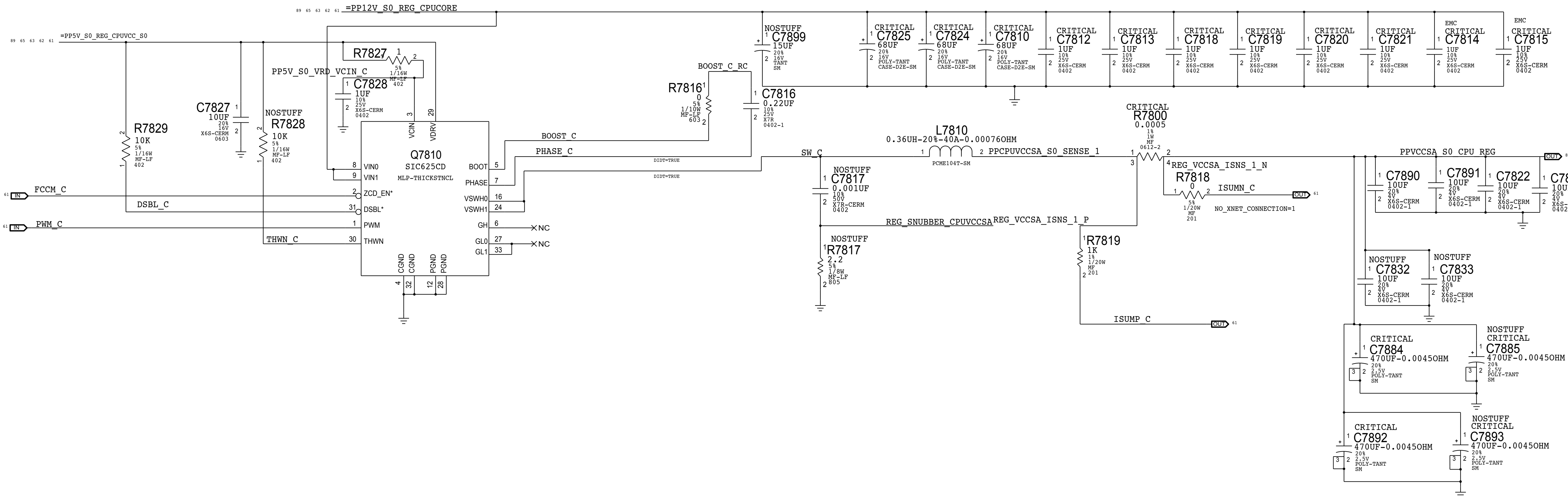
3V3 S5 FET NON SSD


SYNC_MASTER=J95_HARPER		SYNC_DATE=02/11/2015	
PAGE TITLE			
PLATFORM POWER: 3.3V S5/5V S4 VR			
	Apple Inc.	DRAWING NUMBER	SIZE
		051-00673	D
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		BRANCH	
		PAGE	76 OF 121
		SHEET	66 OF 93

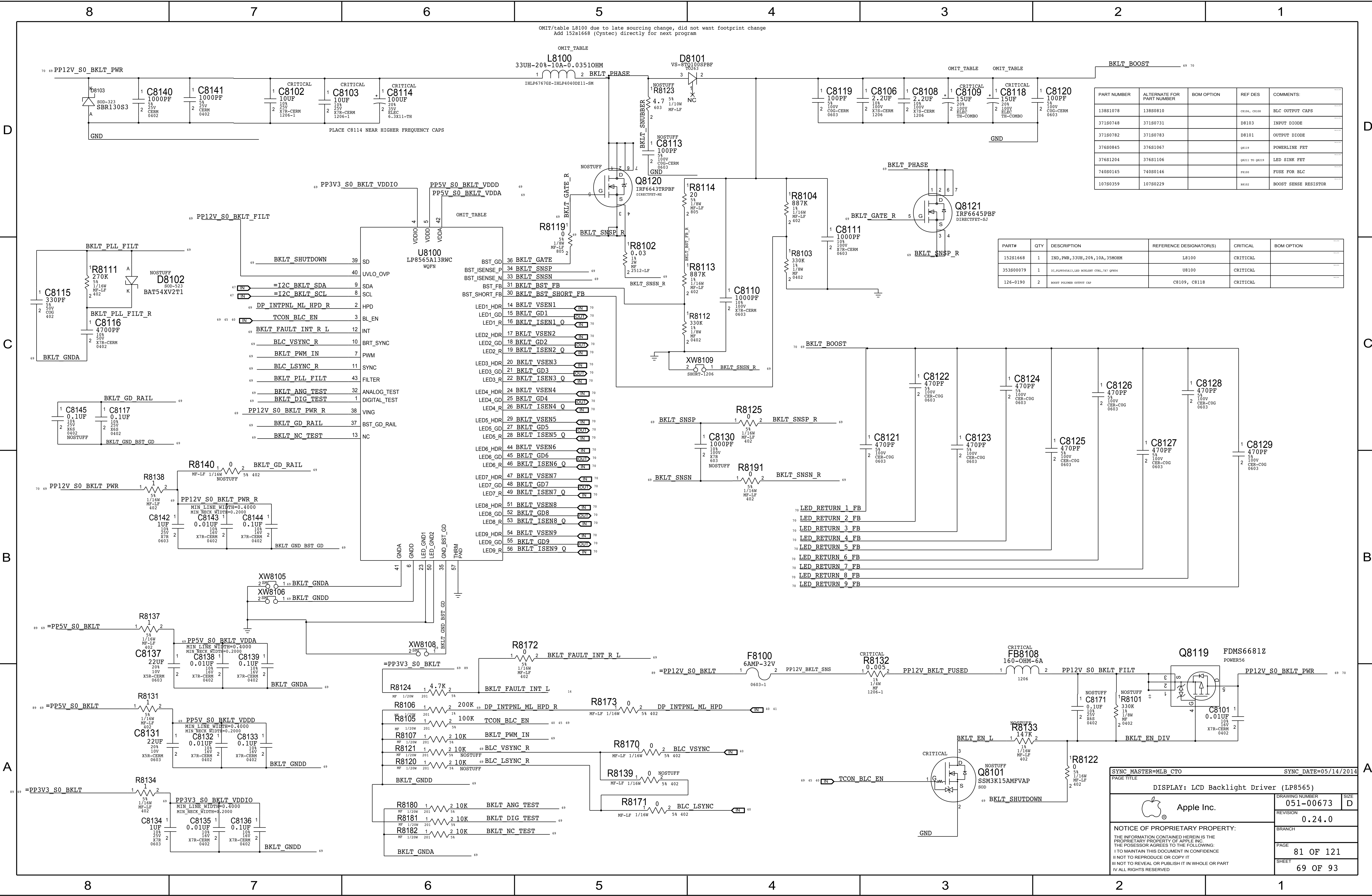
CPU VCCSA Regulator

EDC = 11.1A

TDC = 10A




DRAWING		LAST MODIFIED=Thu Feb 12 14:48:22 2015	
SYNC MASTER=J95 HARPER		SYNC DATE=02/11/2015	
PAGE TITLE			
CPU & CHIPSET: CPU CORE VR (VCCSA)			
 Apple Inc.		DRAWING NUMBER	051-00673
		REVISION	0.24.0
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		PAGE	78 OF 121
		SHEET	68 OF 93

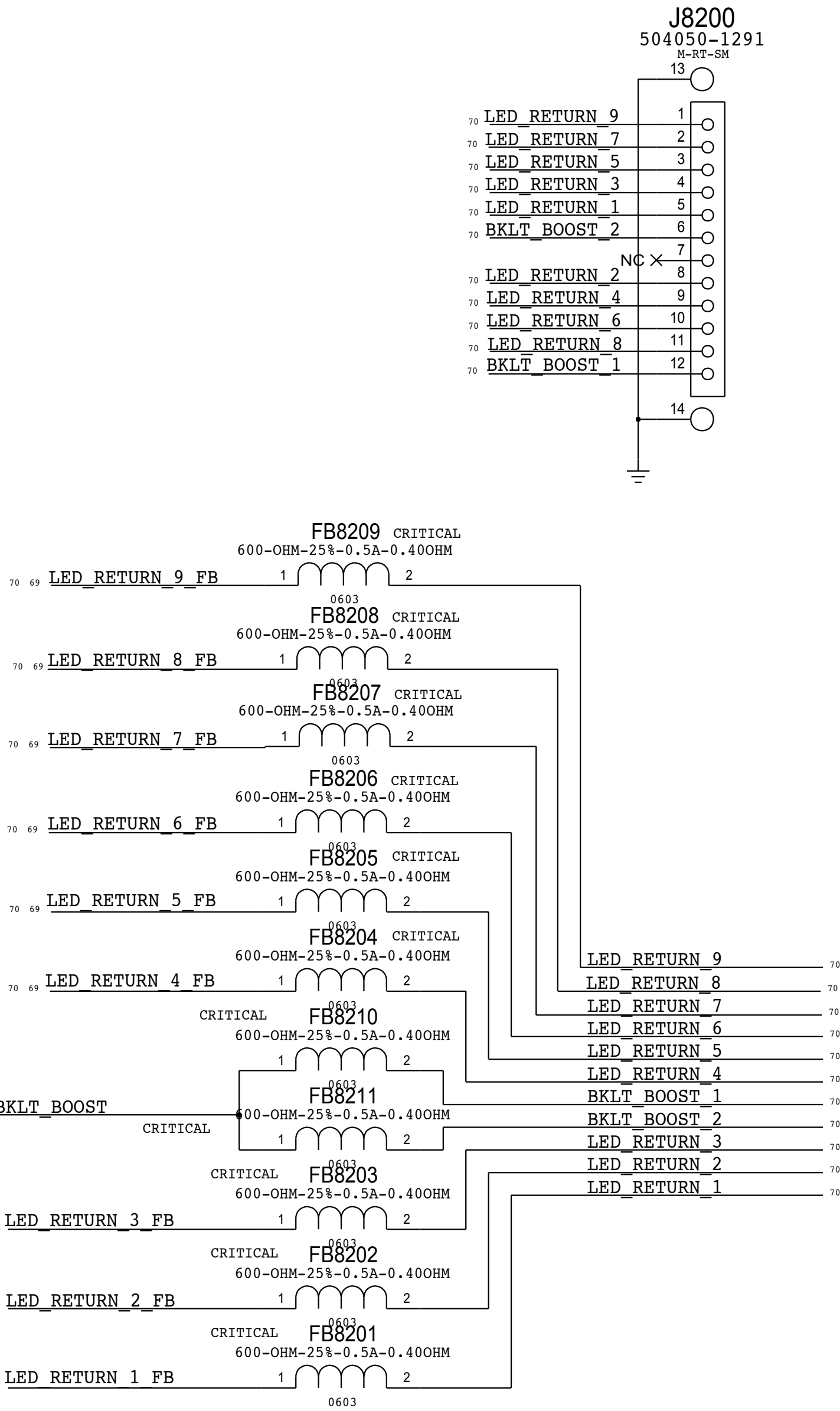
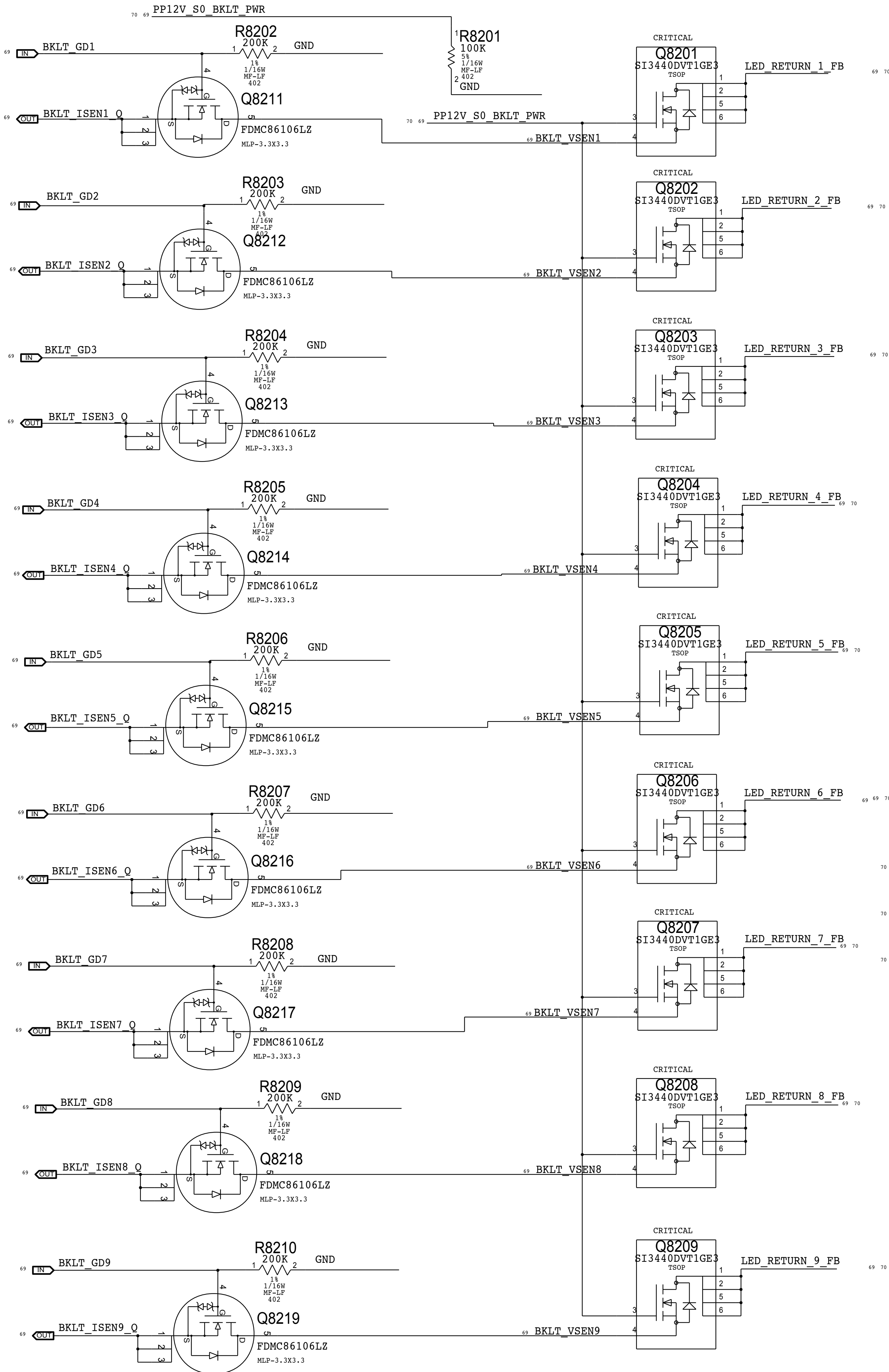



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
136S1078	136S0810		CR106, CR108	BLC OUTPUT CAPS
371S0748	371S0731		D8103	INPUT DIODE
371S0782	371S0783		D8101	OUTPUT DIODE
376S0845	376S1067		Q8119	POWERLINE FET
376S1204	376S1106		Q8111 TO Q8119	LED SINK FET
740S0145	740S0146		F8100	FUSE FOR BLC
107S0359	107S0229		R8102	BOOST SENSE RESISTOR

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S1668	1	IND, PWR, 33UH, 20%, 10A, 35MORM	L8100	CRITICAL	
353S00079	1	IC, LP8565A13, LED BACKLIGHT CTRL, 7X1 QFN56	U8100	CRITICAL	
126-0190	2	BOOST POLYMER OUTPUT CAP	C8109, C8118	CRITICAL	


SYNC MASTER=MLB_CTO		SYNC DATE=05/14/2014	
PAGE TITLE			
DISPLAY: LCD Backlight Driver (LP8565)			
 Apple Inc.		DRAWING NUMBER	SIZE
		051-00673	D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		REVISION	0.24.0
		BRANCH	
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		SHEET	
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1256	376S1073		ALL	Short Protection FET
155S0831	155S0797		ALL	FB8201 TO FB8211

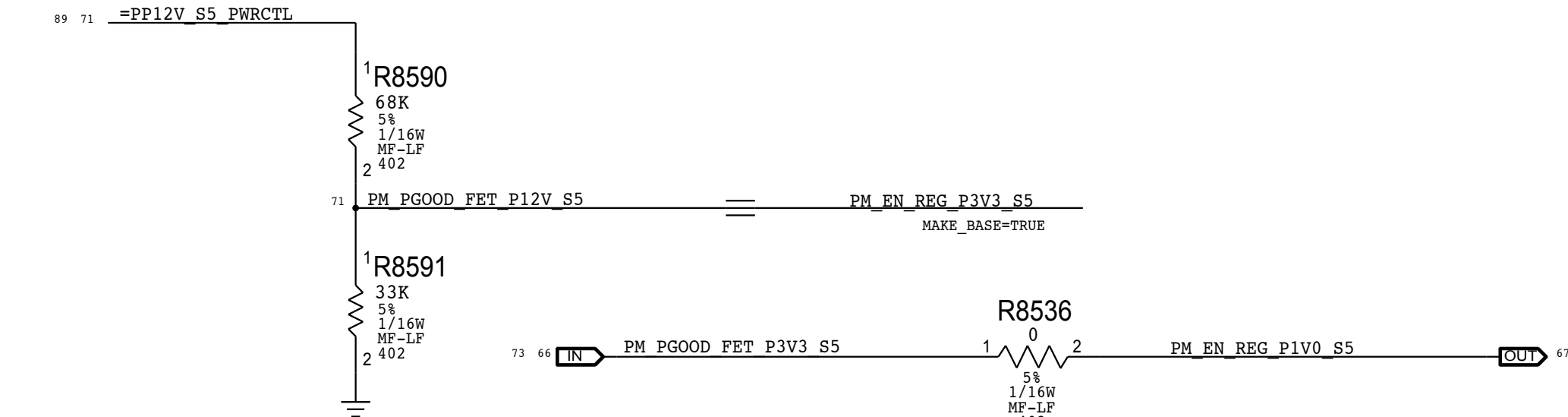


SYNC MASTER=MLB CTO		SYNC DATE=05/14/2014		
PAGE TITLE				
DISPLAY: Backlight Driver 2				
 Apple Inc.		DRAWING NUMBER	051-00673	D
		REVISION	0.24.0	
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		PAGE	82 OF 121	
		SHEET	70 OF 93	

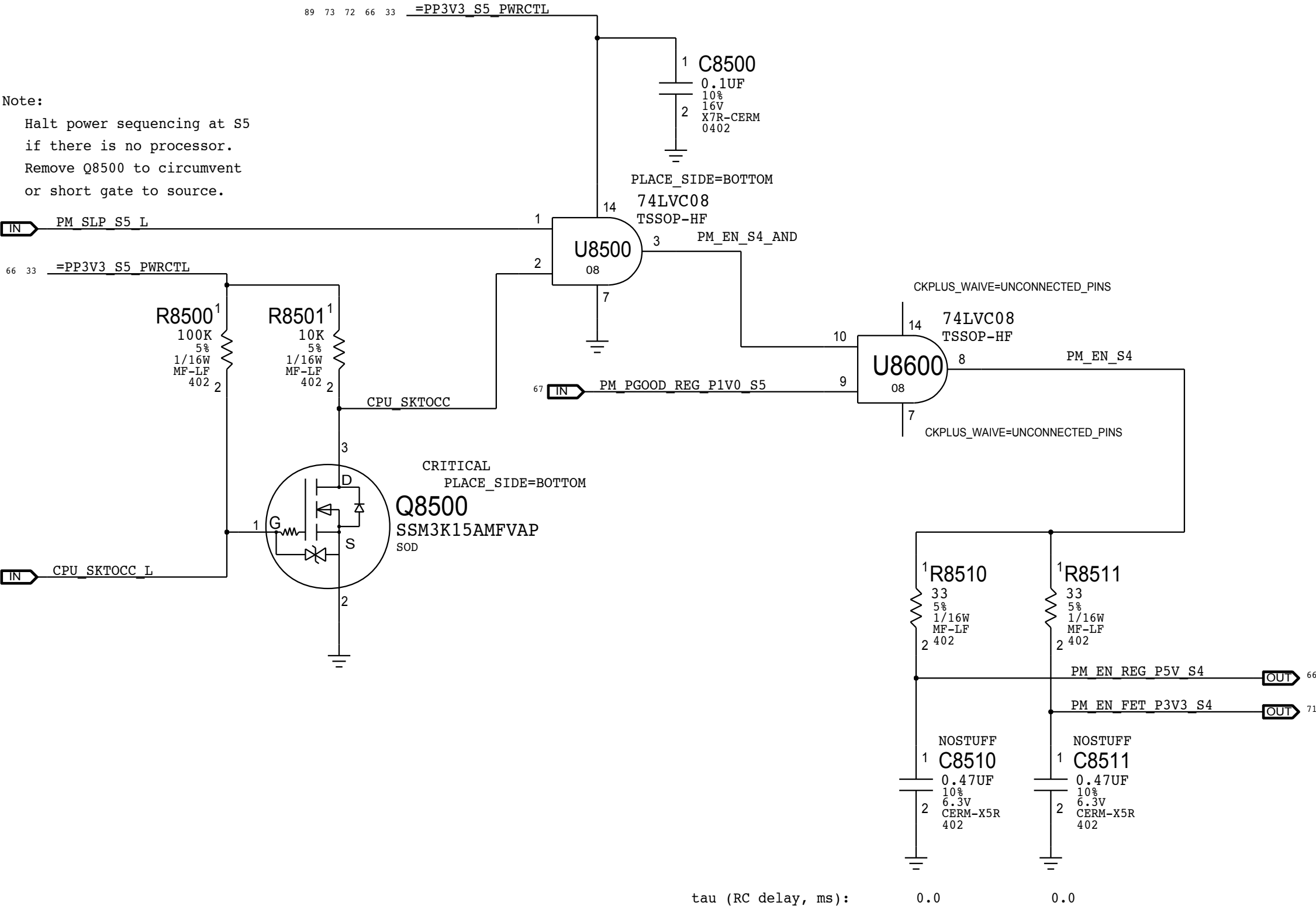


SYNC MASTER=J17 MAX		SYNC DATE=02/11/2013	
PAGE TITLE			
PLATFORM POWER: FET-Controlled S0 and S4			
 Apple Inc.		DRAWING NUMBER	
		051-00673	
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		0.24.0	
		BRANCH	
		PAGE	
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		71 OF 93	

S5 Enable

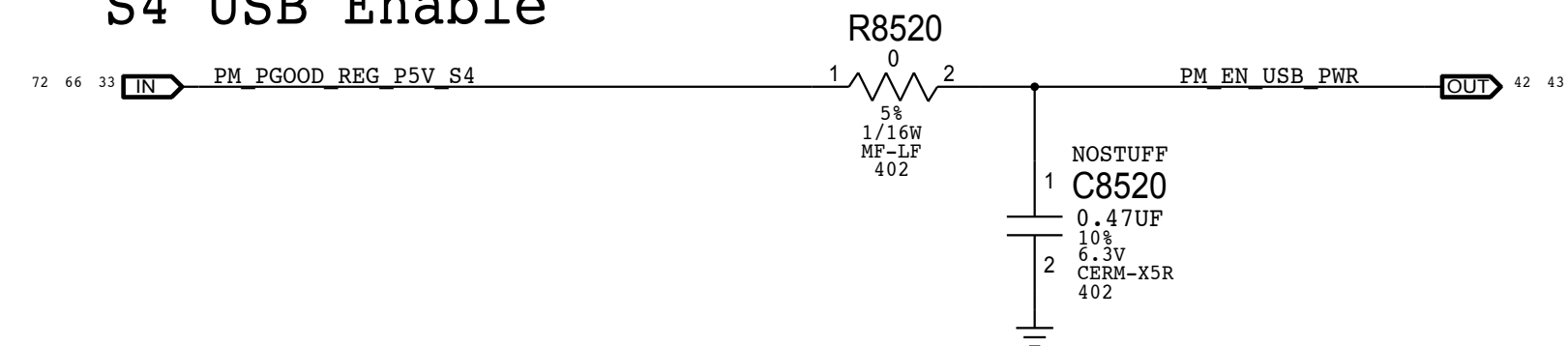


S4 Enables



Note:
Halt power sequencing at S5
if there is no processor.
Remove Q8500 to circumvent
or short gate to source.

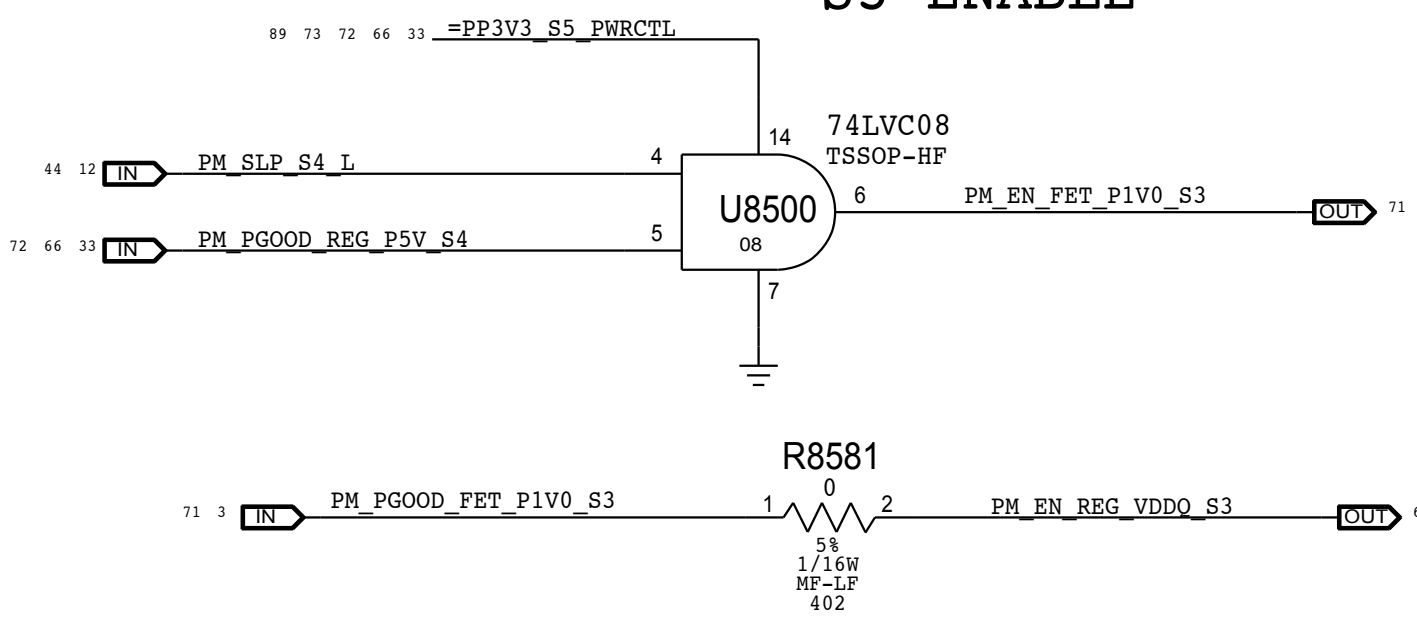
S4 USB Enable



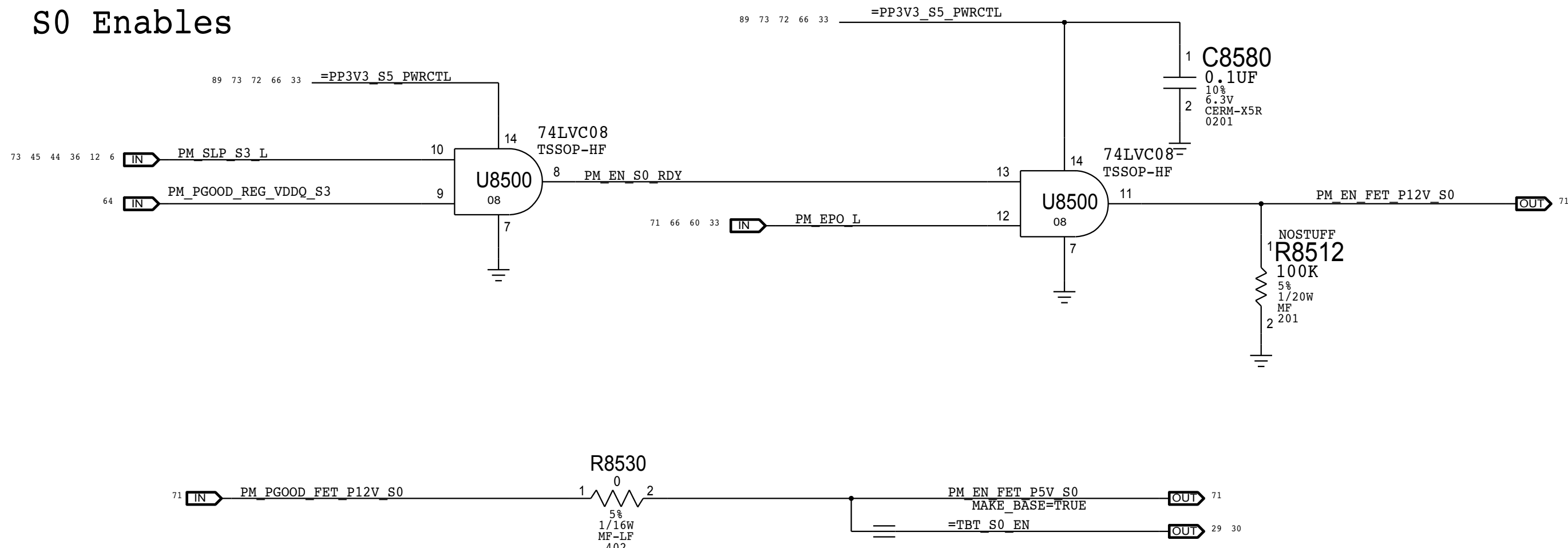
S4 TBT S4 Port Enable



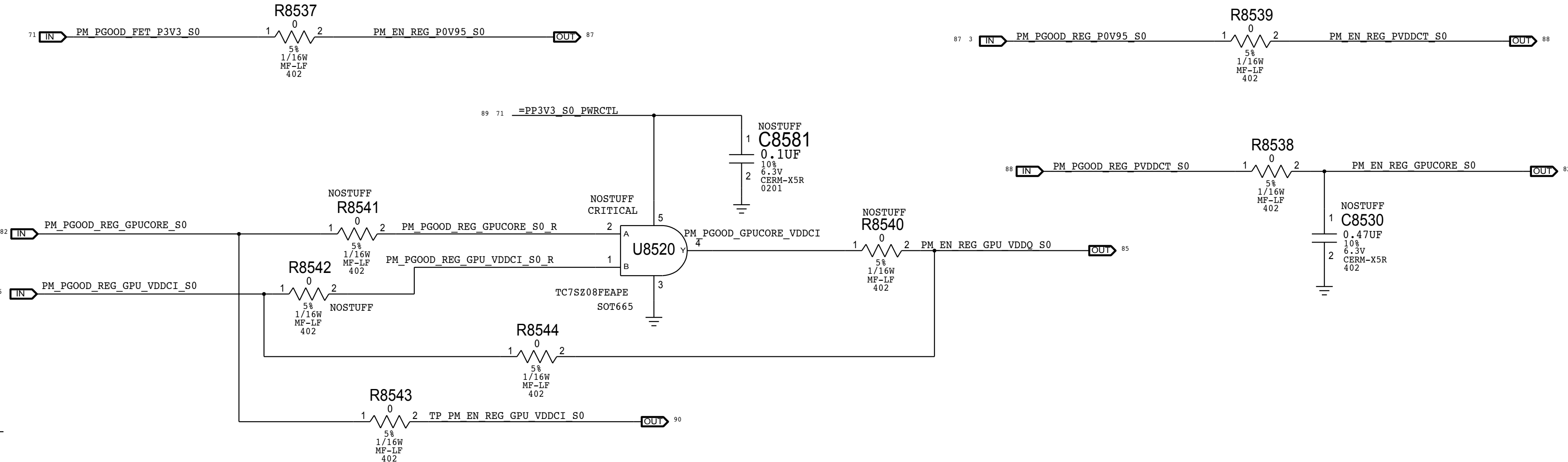
S3 ENABLE



S0 Enables



S0 GPU SEQUENCING



Power Sequencing requirements

System:

1. 12V_ADCD -> 3V42G3H -> 12V_S5/12V_S5_SSD -> 3V3_S5 -> 1V0_S5 -> 5V_S4/3V3_S4 -> 1V0_S3

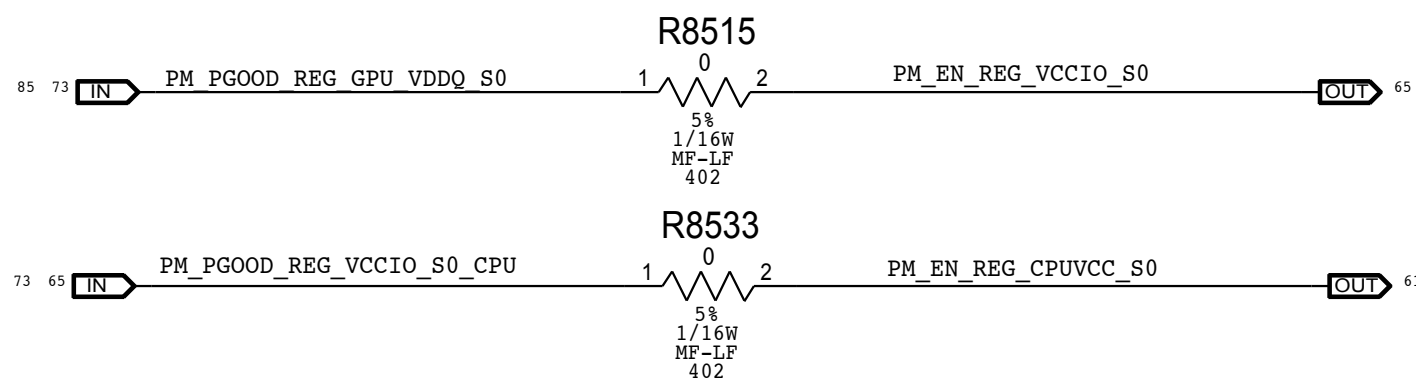
Intel CPU:

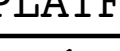
2. 1V0_S3 -> VDDQ_S3 -> 12V_S0 -> 5V_S0 -> 3V3_S0 -> GPU Rails -> VCCIO_S0 -> VCC_CPU_S0 (VCCGT & VCCSA)

AMD GPU:

3. 3V3_S0 -> 0V95 -> 1V8 (VDD_CT) -> GPUCORE (VDDC) -> VDDCI -> FBVDDQ

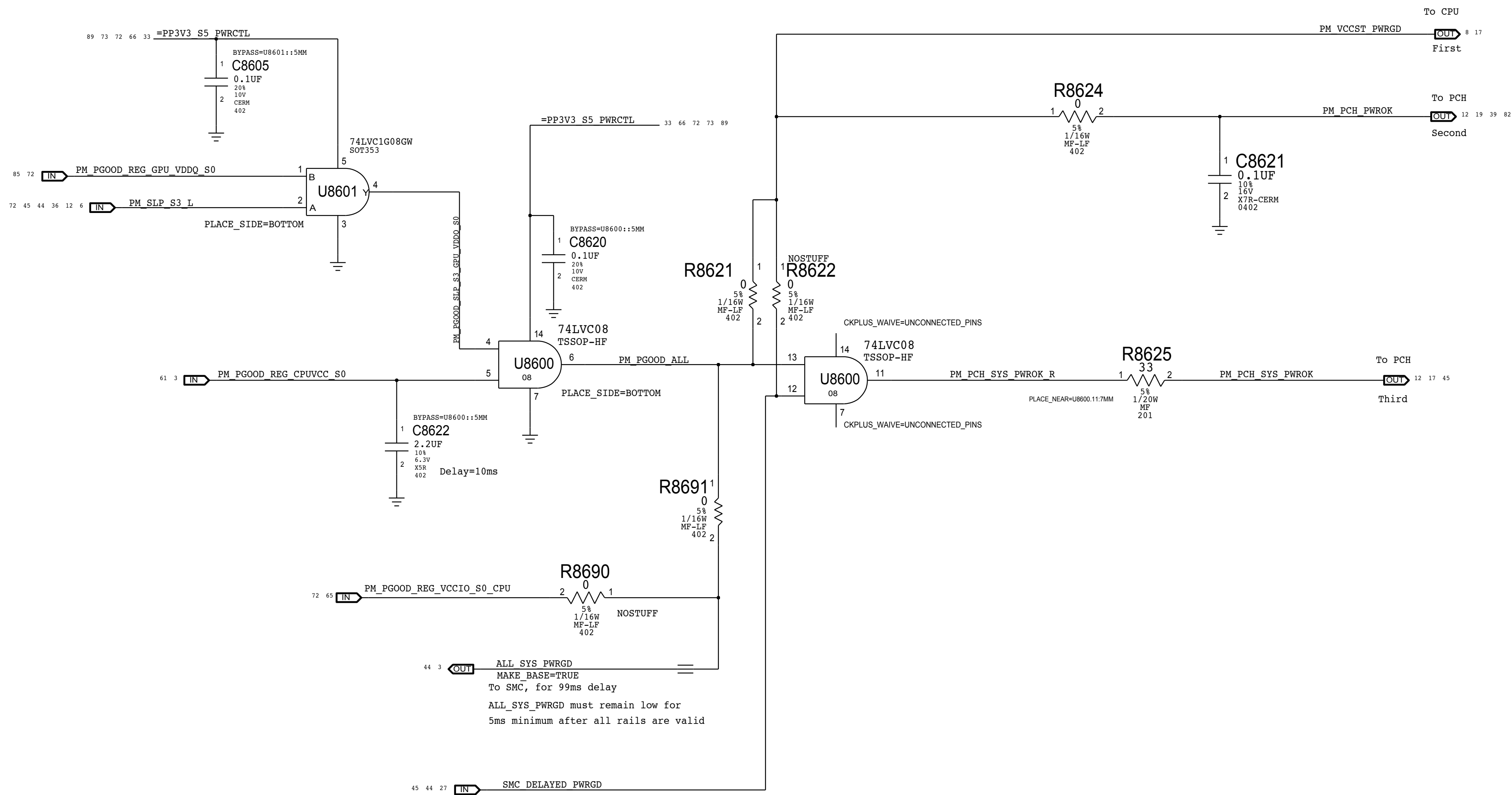
S0 CPU Sequencing



SYNC_MASTER=J78 KENNY		SYNC_DATE=12/18/2013	
PAGE TITLE			
PLATFORM POWER: Regulator Enables			
	DRAWING NUMBER		SIZE
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ALL_SYS_PWRGD,PCH_PWROK & SYS_PWROK Generation

PCH Power Goods



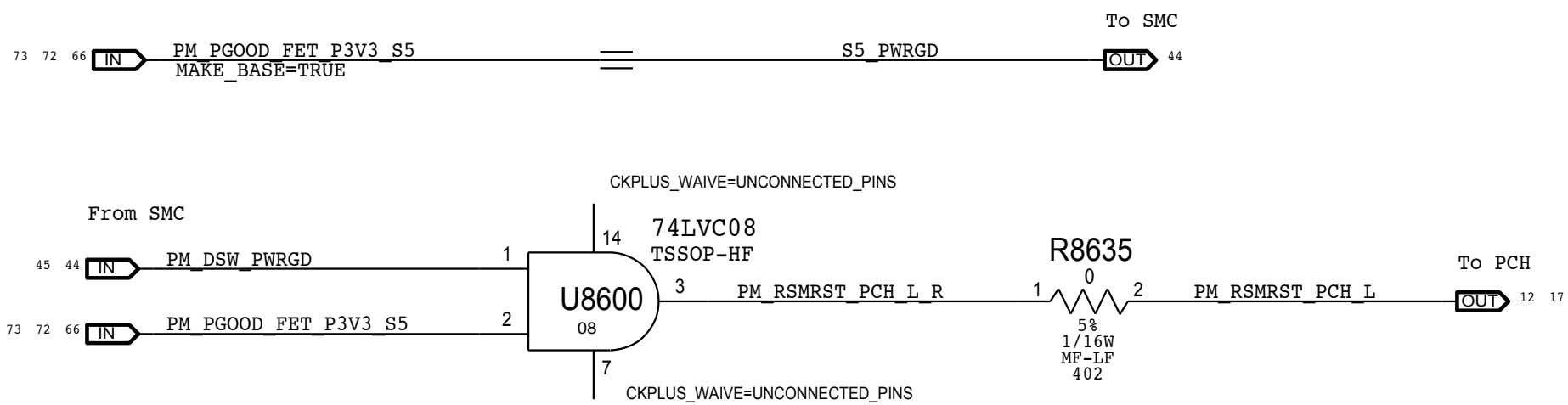
Resume Reset


Intel Doc# 29517 Maho Bay PDG, Section 22.13
Intel Doc# 29562 Panther Point EDS, Section 8.7 and 8.8

Note:
THE IMAC J78 DESIGNS DOES NOT SUPPORT DEEP SX MODES SO BOTH DPWROK AND RSMRST# signals are shorted together

Requirements:
Power on:
Asserted at least 10 ms after all suspend well power is valid
Power off or loss of AC:
Transition to 0.0V or less before VccSUS3_3 drops to 2.90 V
to allow PCH to switch suspend well to battery without excessive loading

Method:
The SMC guarantees proper assertion and de-assertion of RSMRST# for normal operation via PM_DSW_PWRGD.
RSMRST# is asserted when power good from regulator is de-asserted in the event AC is lost. Power good de-assertion should happen quickly enough to meet Intel spec.



SYNC_MASTER=J78 KENNY		SYNC_DATE=10/09/2013	
PAGE TITLE			
PLATFORM POWER: PM Power Good			
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Page Notes

Power aliases required by this page

- *997772_DPU_VCO32

Signal aliases required by this paper:

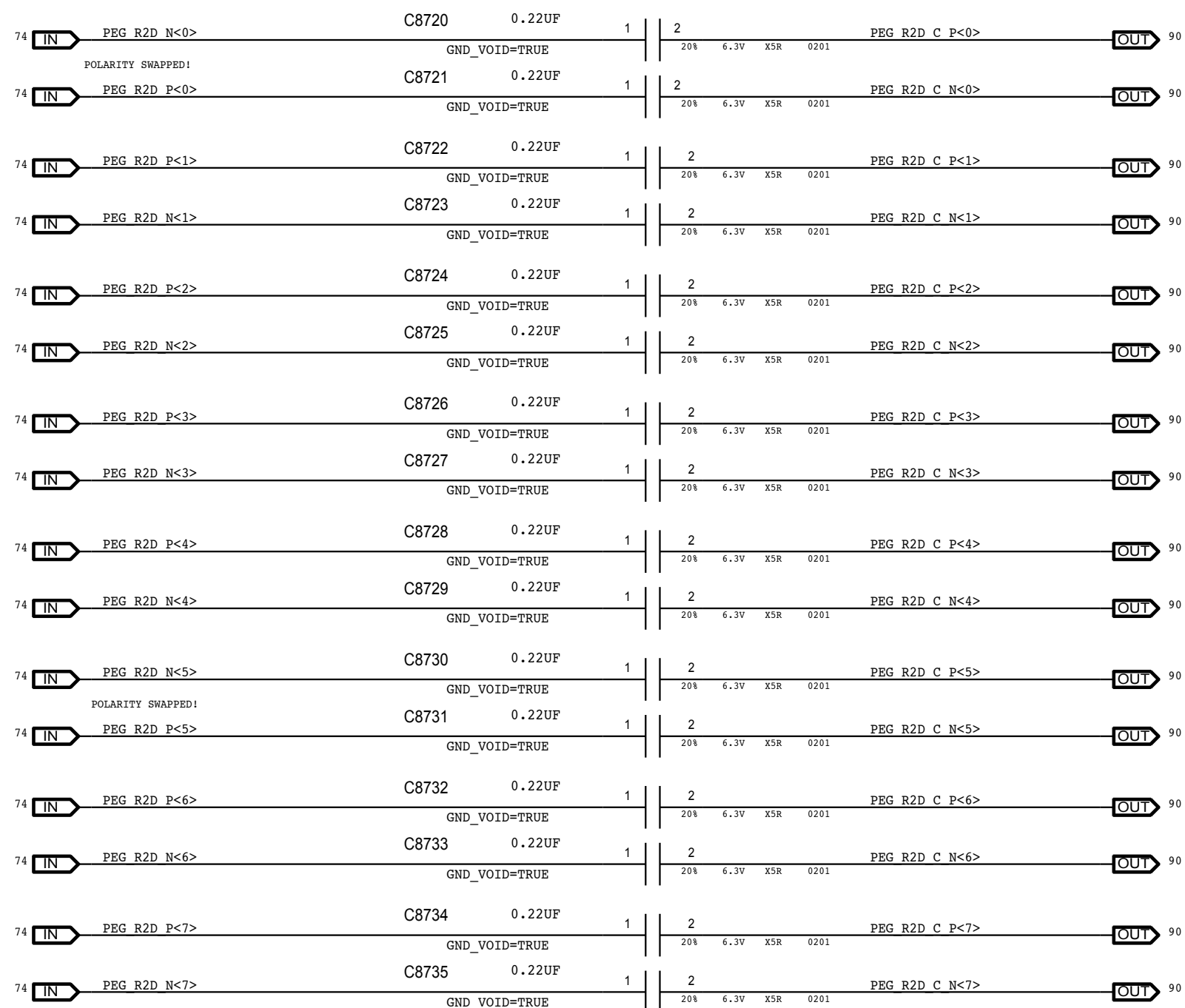
(1992)

DOI options provided by this page

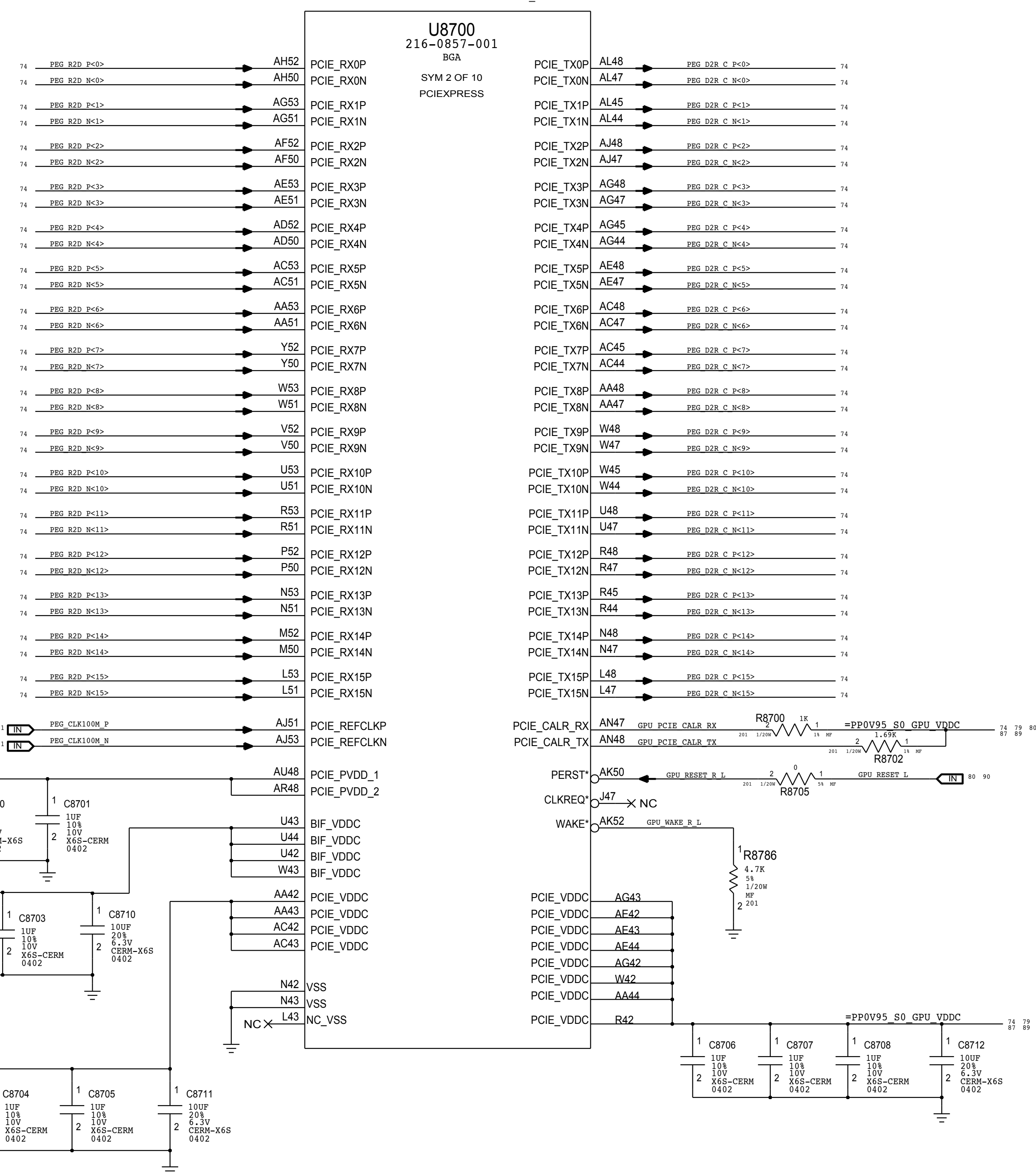
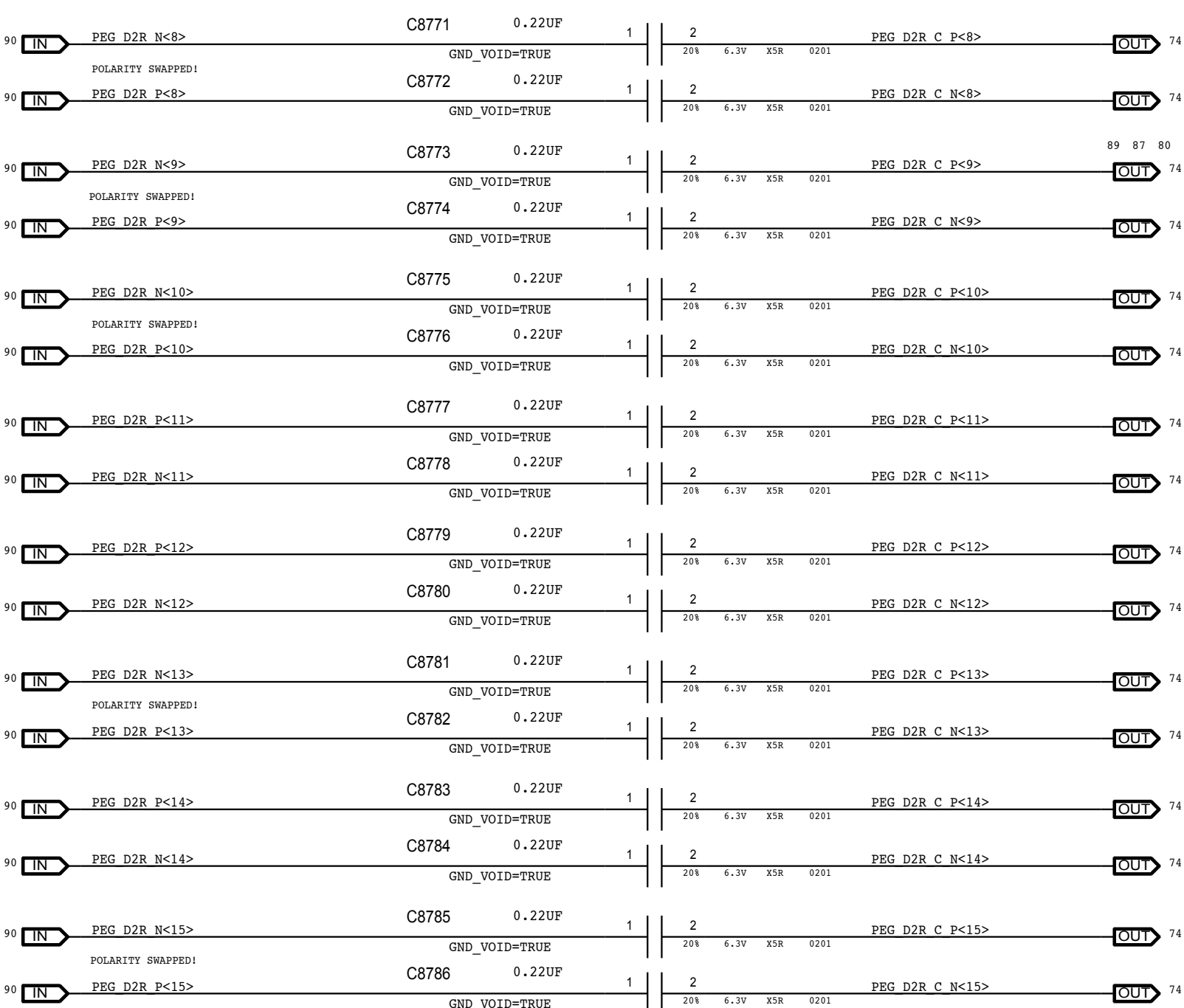
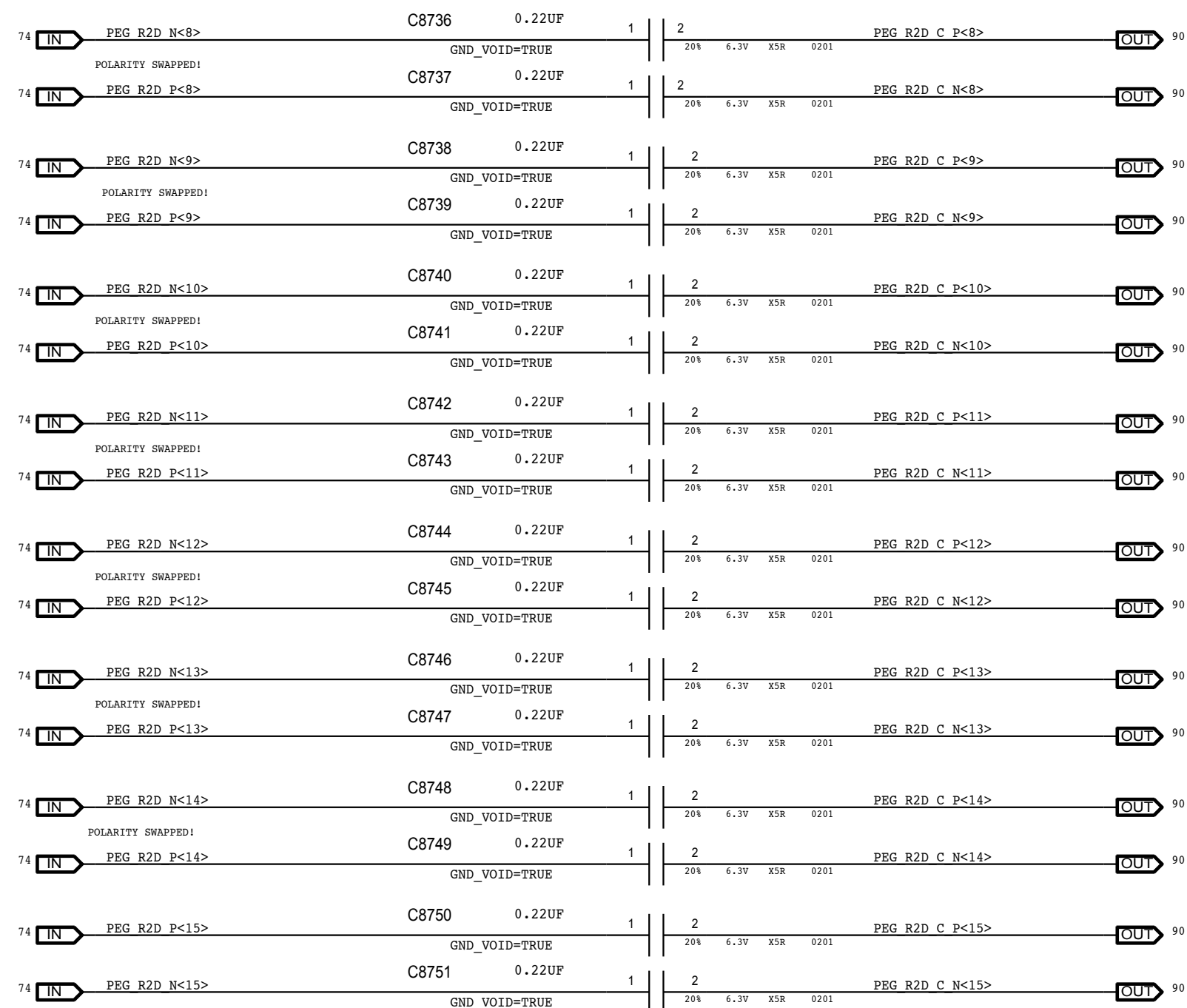
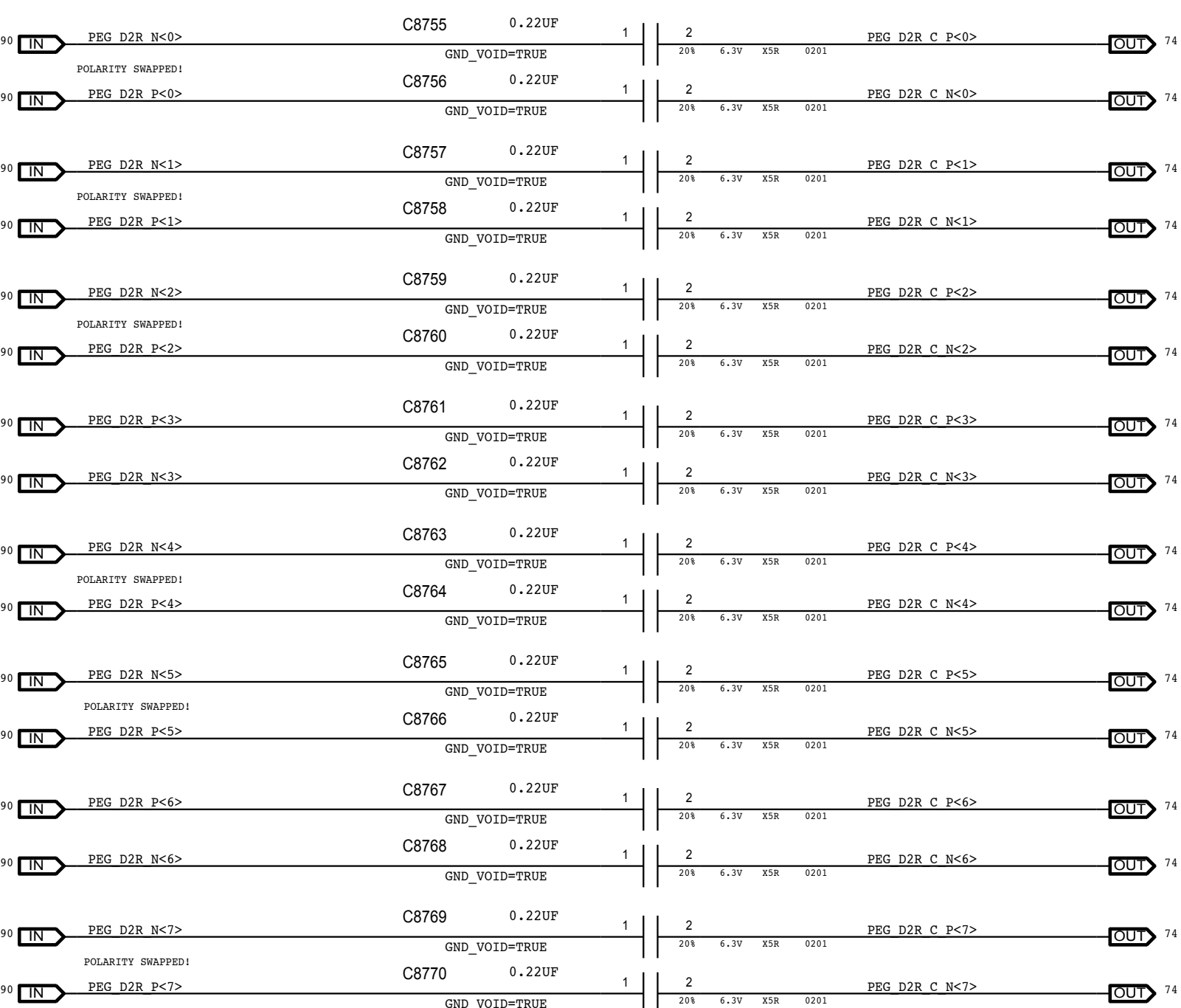
(1908)

POLARITY SWAPS INTENDED ON LANES,SEE NOTES AT DIFF PAIRS.
ALL LANES ARE ALSO REVERSED, SEE ALIASES ON CSA 112

ALL LANES ARE REVERSED (SEE ALIASES ON CSA 112), SEE DIFF PAIRS FOR POLARITY SWAP INFO



ALL LANES ARE REVERSED (SEE ALIASES ON CSA 112), SEE DIFF PAIRS FOR POLARITY SWAP INFO



SYNC MASTER=J95 SYNC DATE=08/26/2013

PAGE TITLE

GFX: Emerald PCIe



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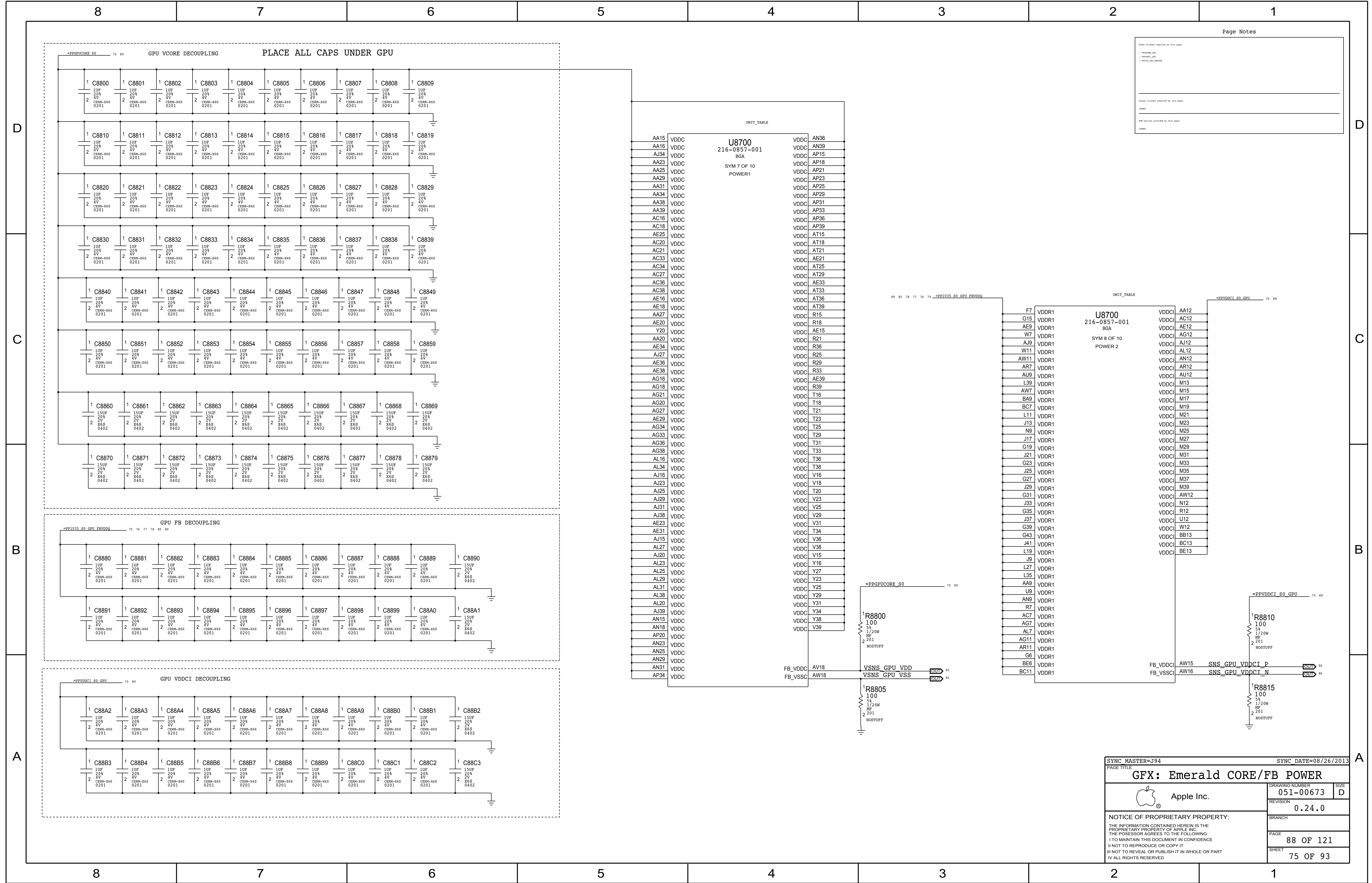
0.24.0

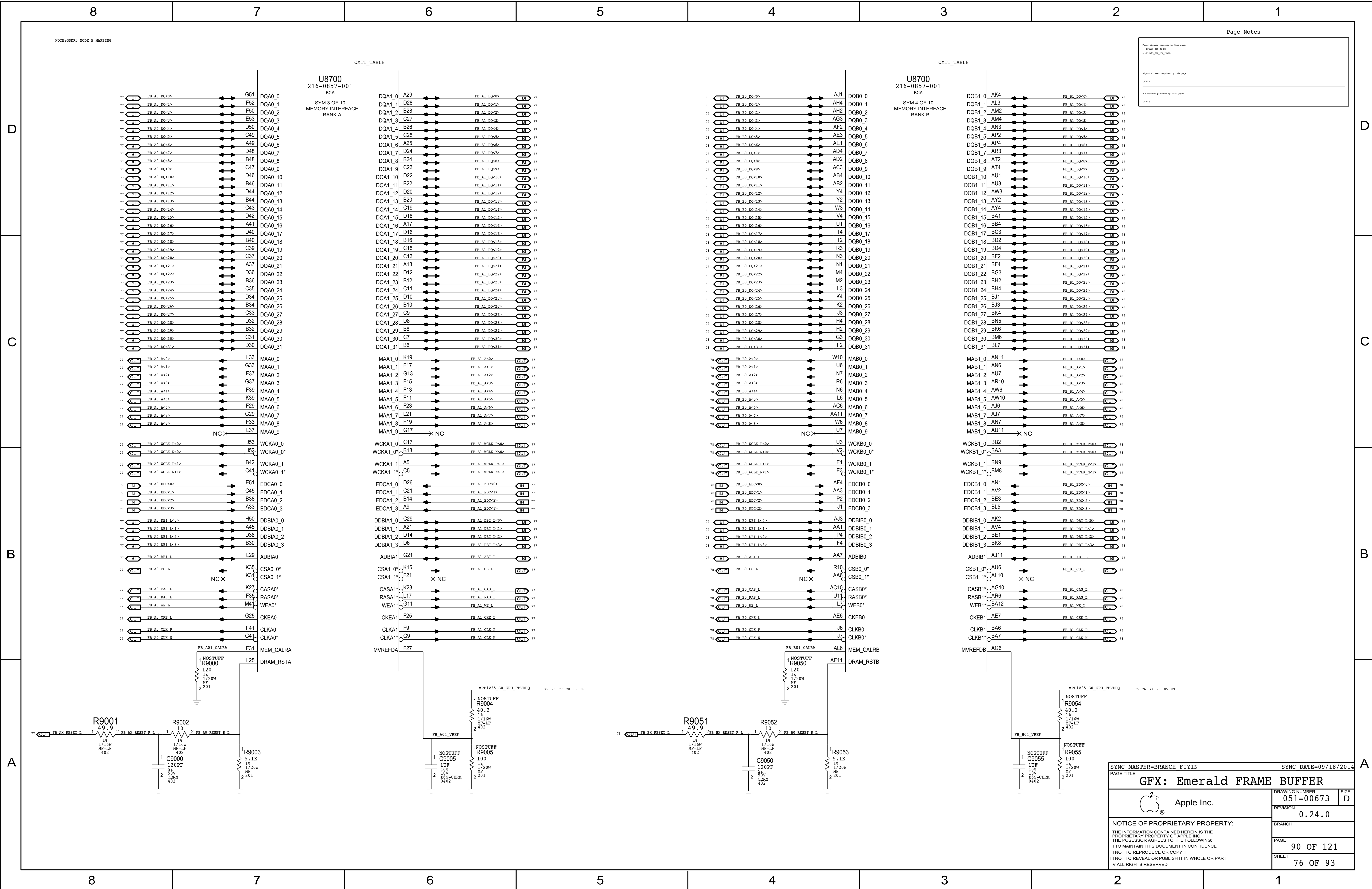
BRANCH

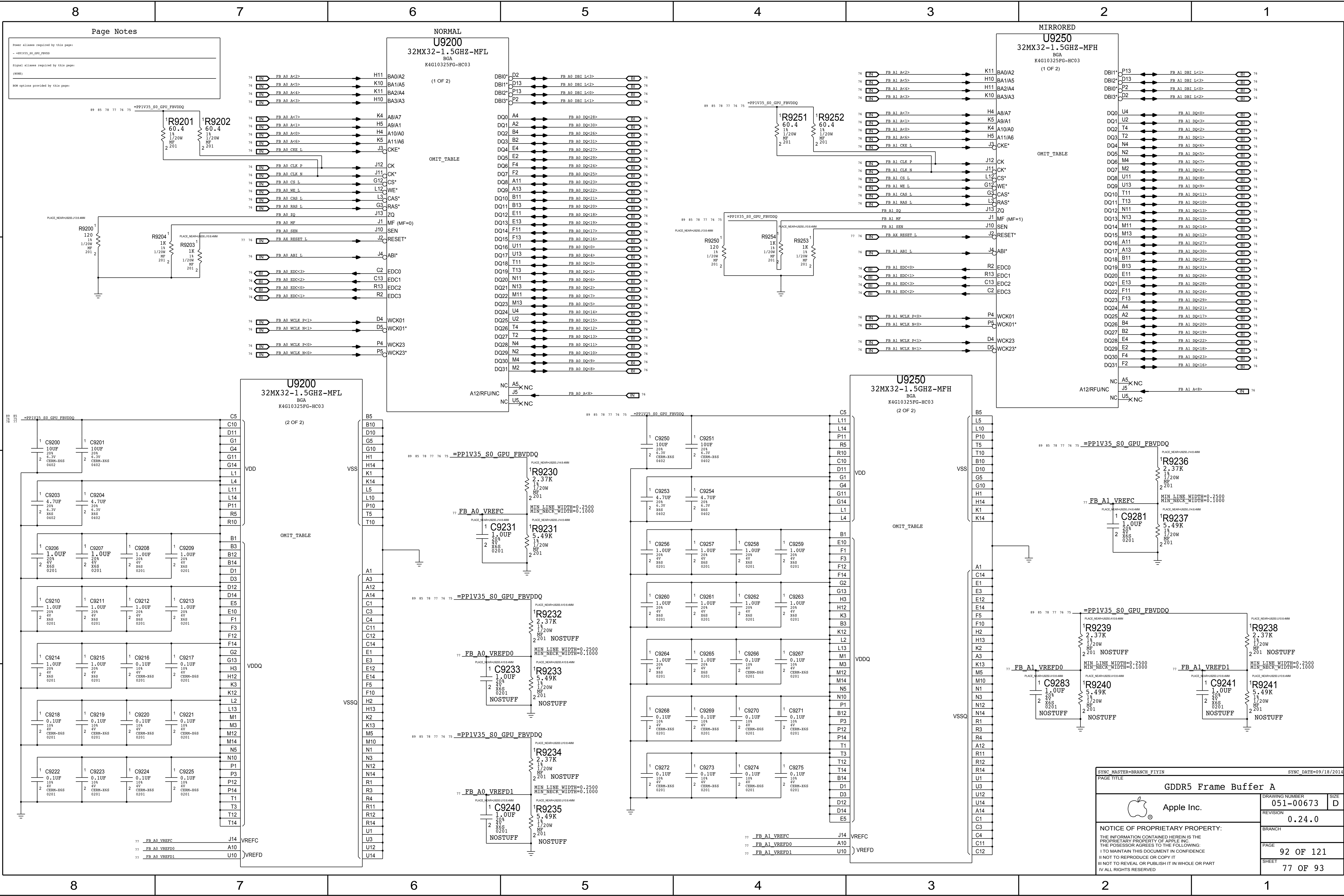
Table 1

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Page Notes

Power aliases required by this page:
- *PP1V35_S0_GPU_FBVDDQ

Signal aliases required by this page:
(NONE)

ROM options provided by this page:

NORMAL

U9200

32MX32-1.5GHZ-MFL

BGA

K4G10325FG-HC03

(1 OF 2)

MIRRORED

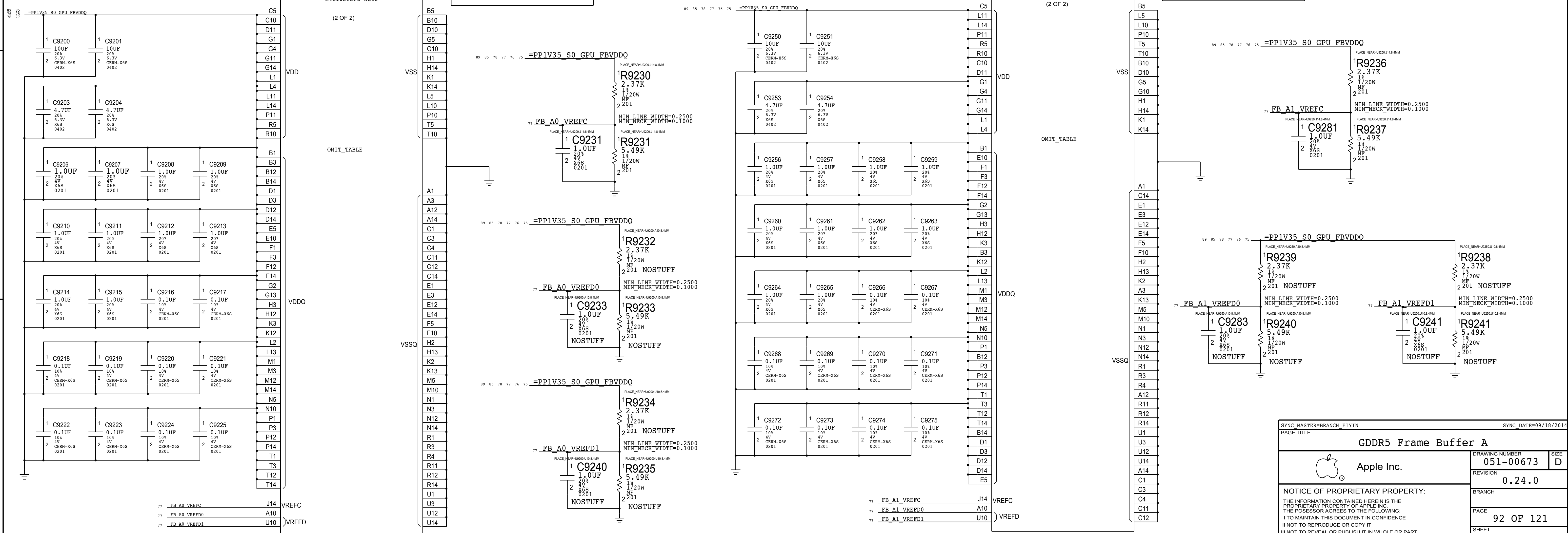
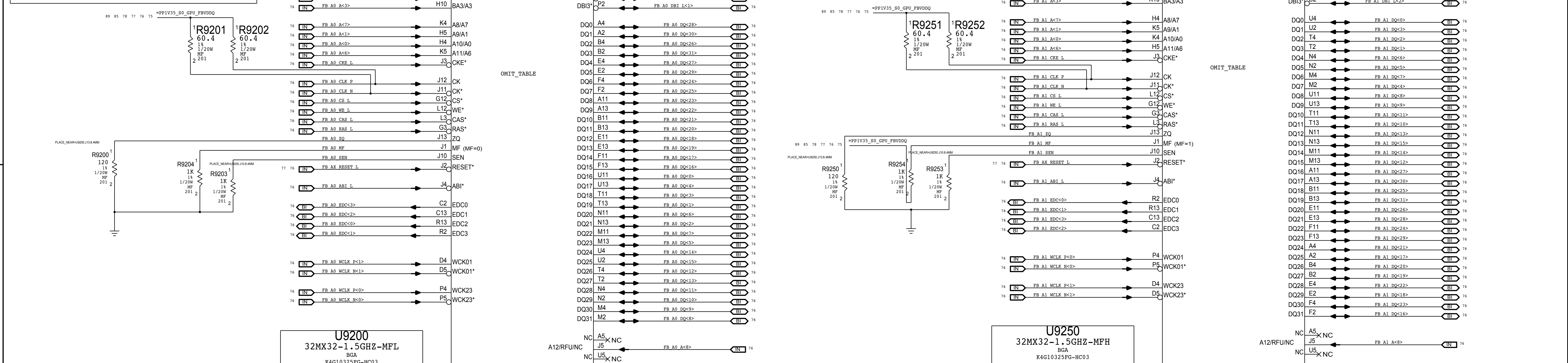
U9250

32MX32-1.5GHZ-MFH

BGA

K4G10325FG-HC03

(1 OF 2)



SYNC_MASTER=BRANCH_FIYIN

SYNC_DATE=09/18/2014

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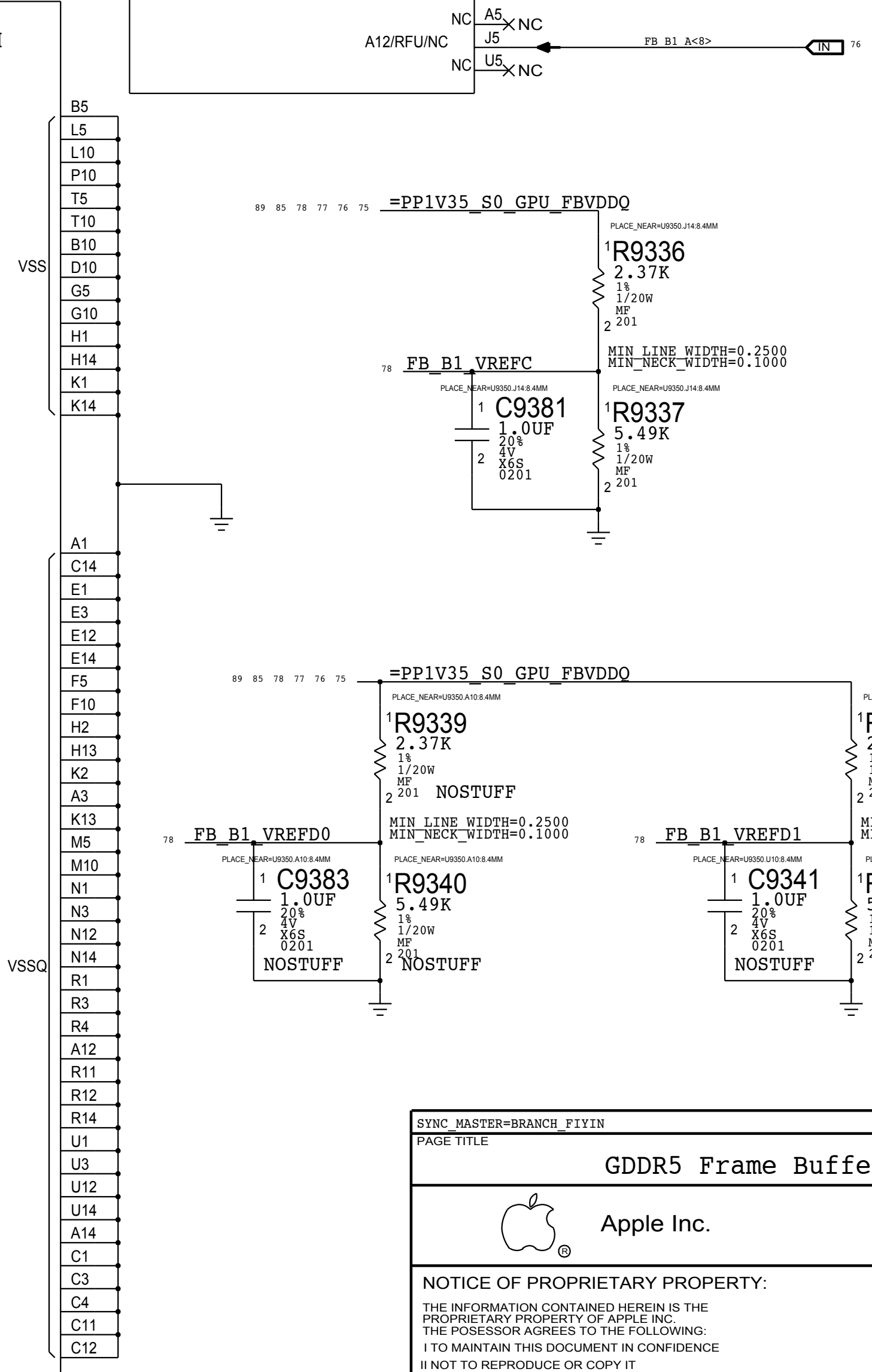
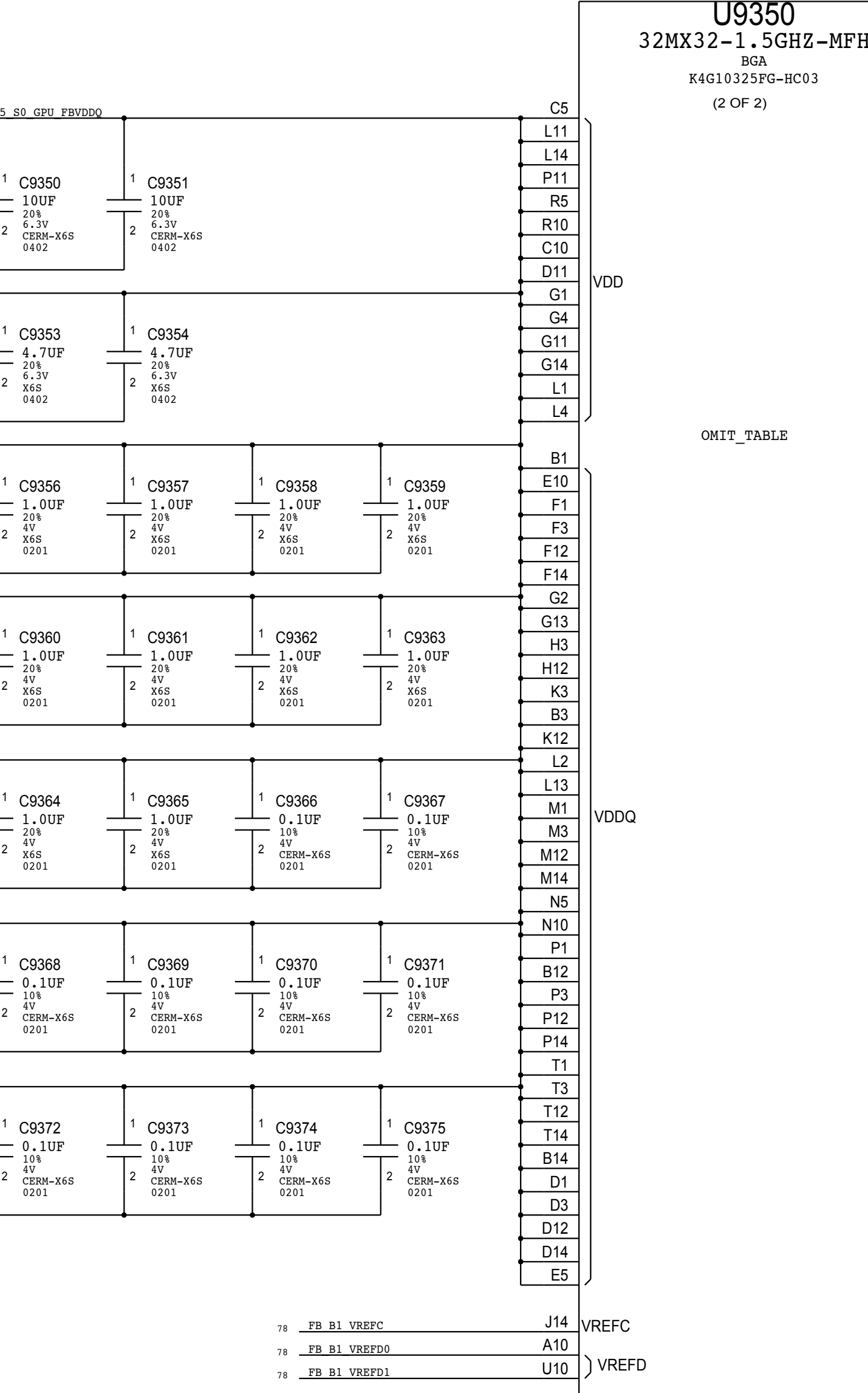
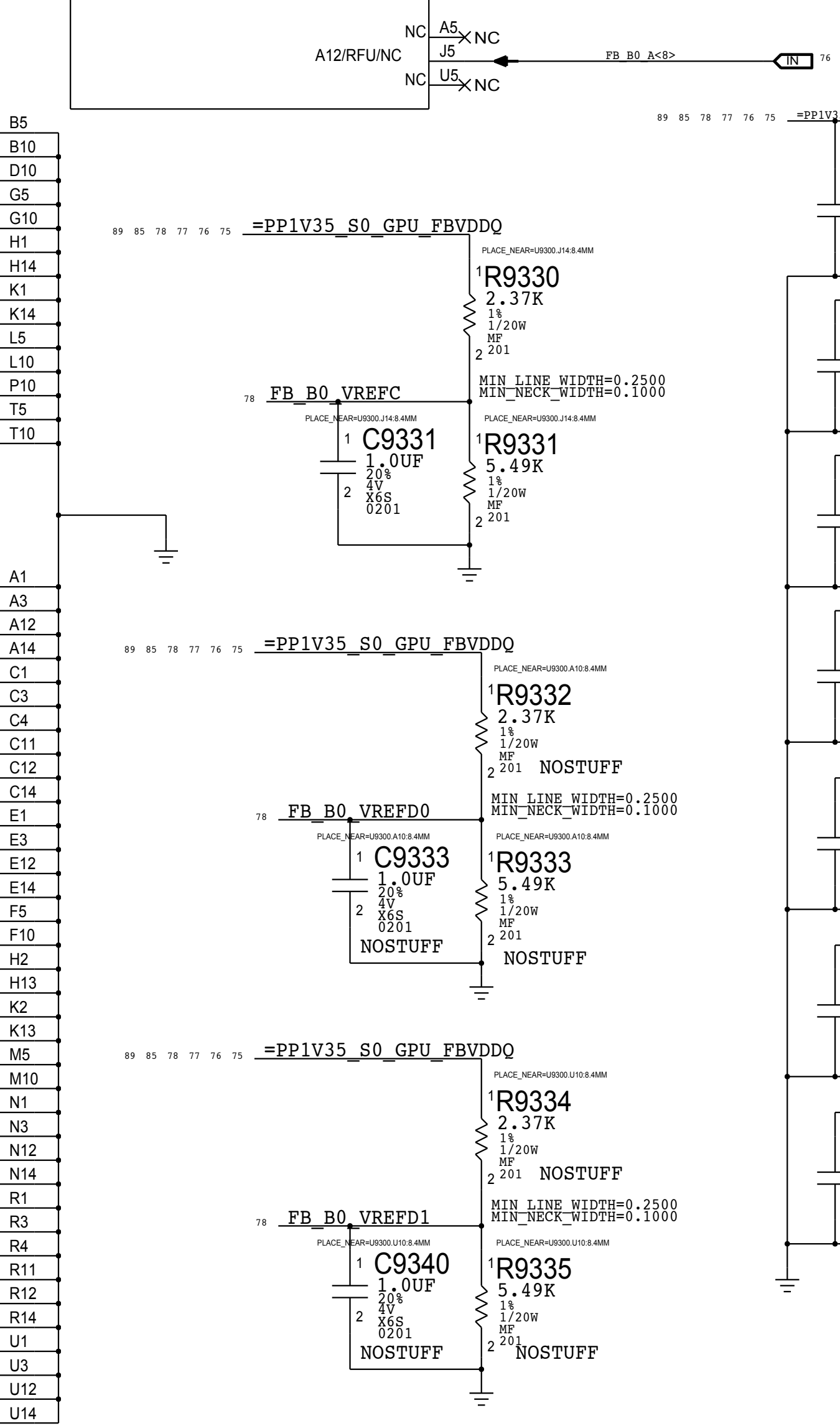
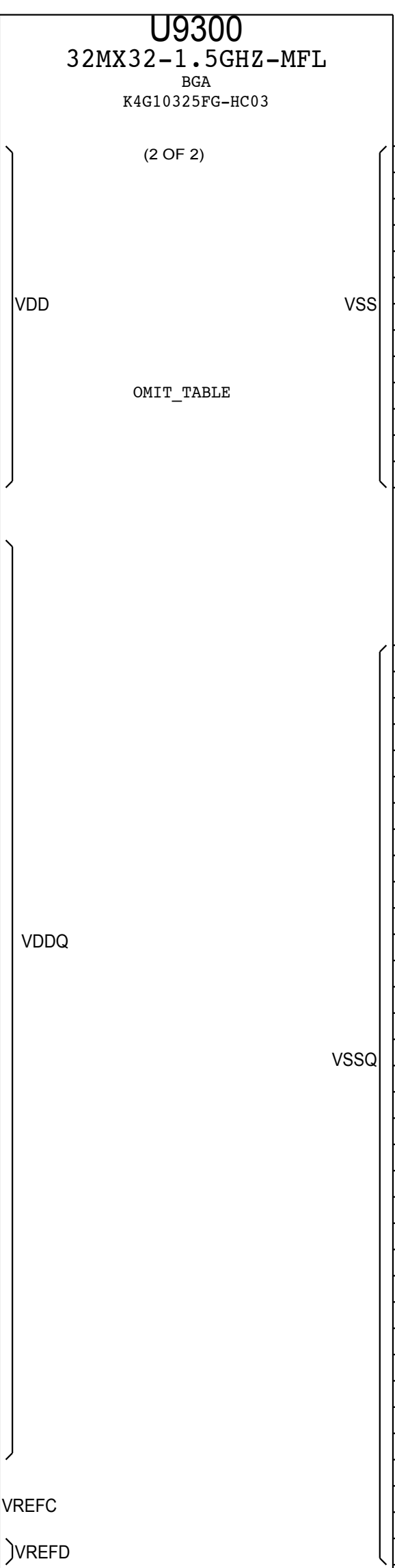
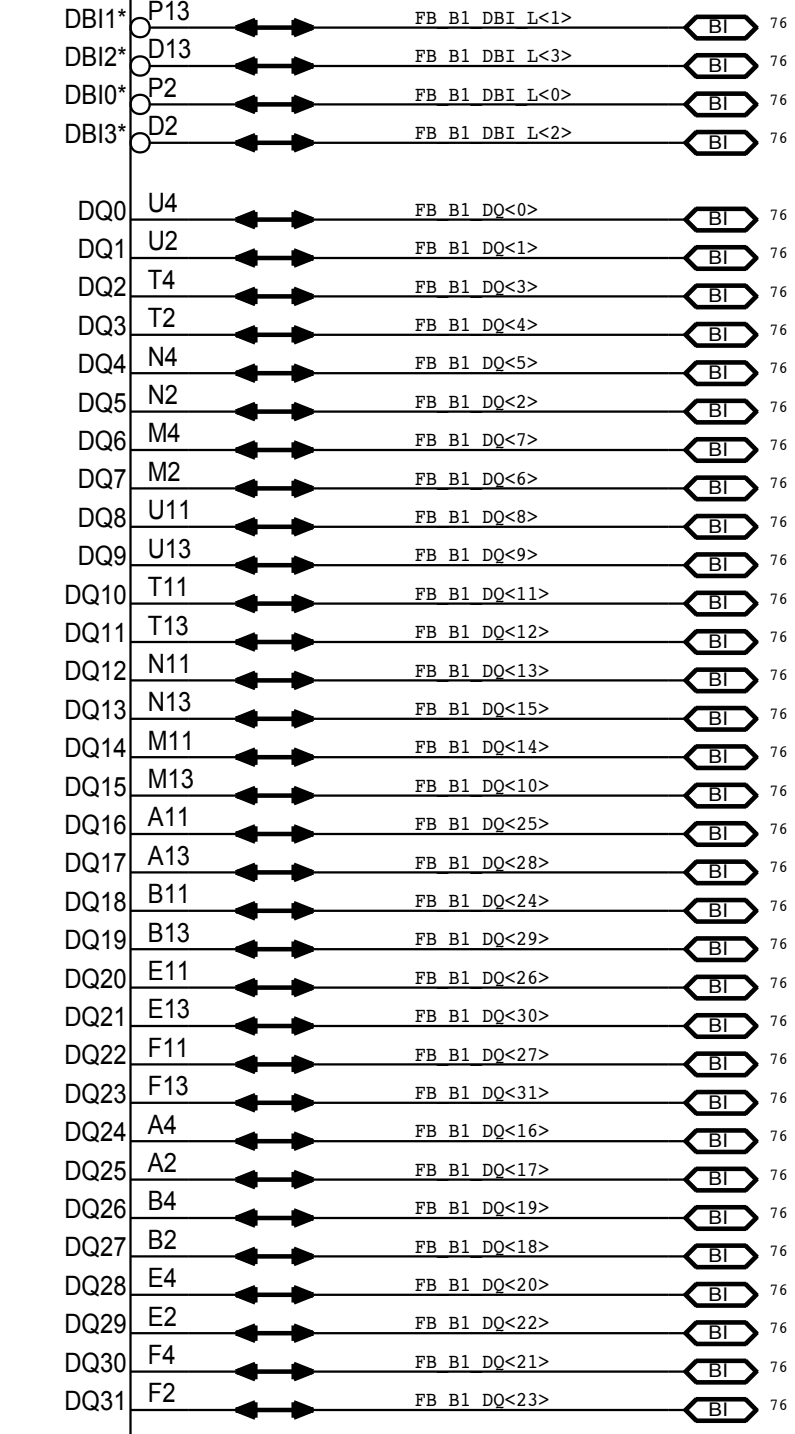
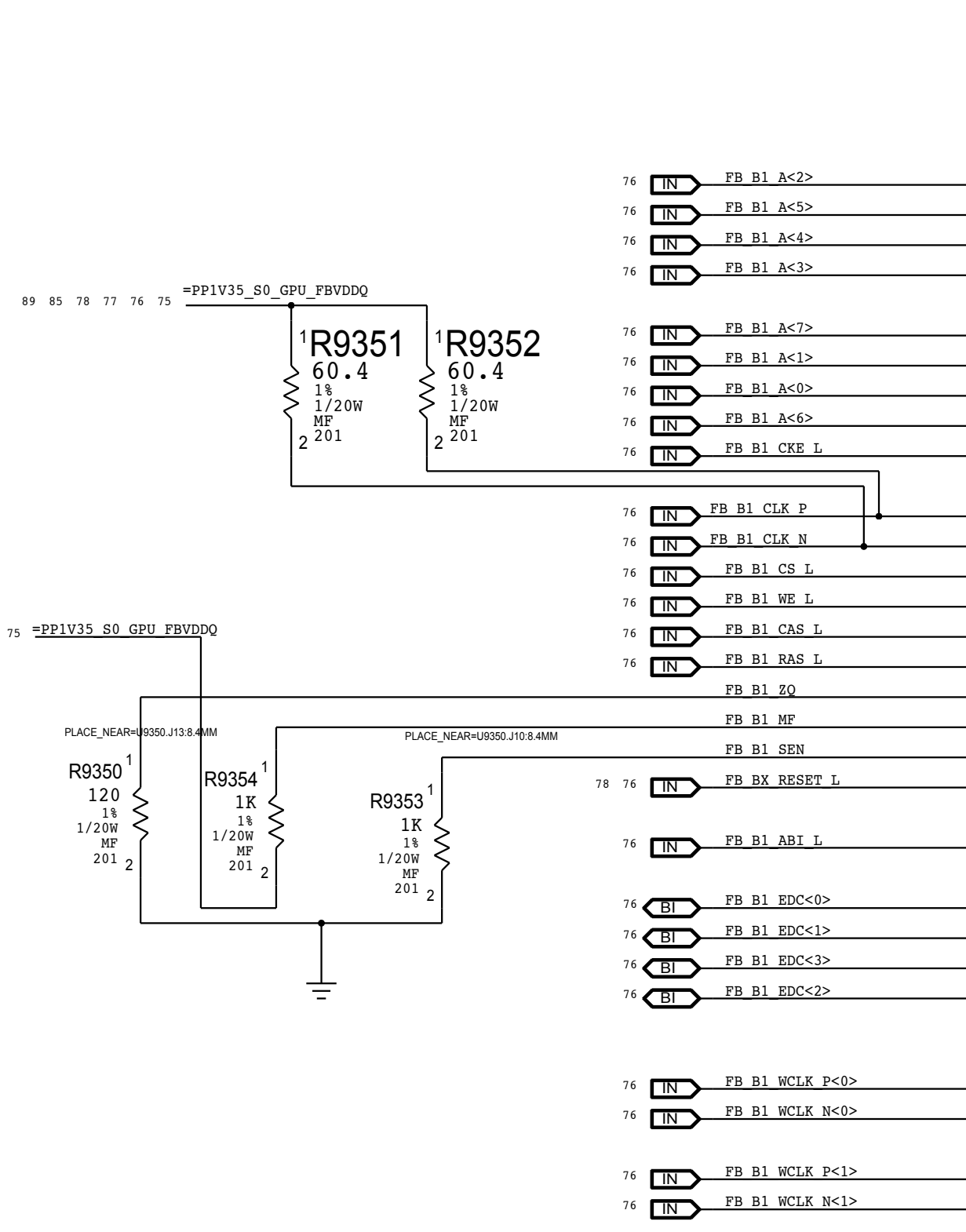
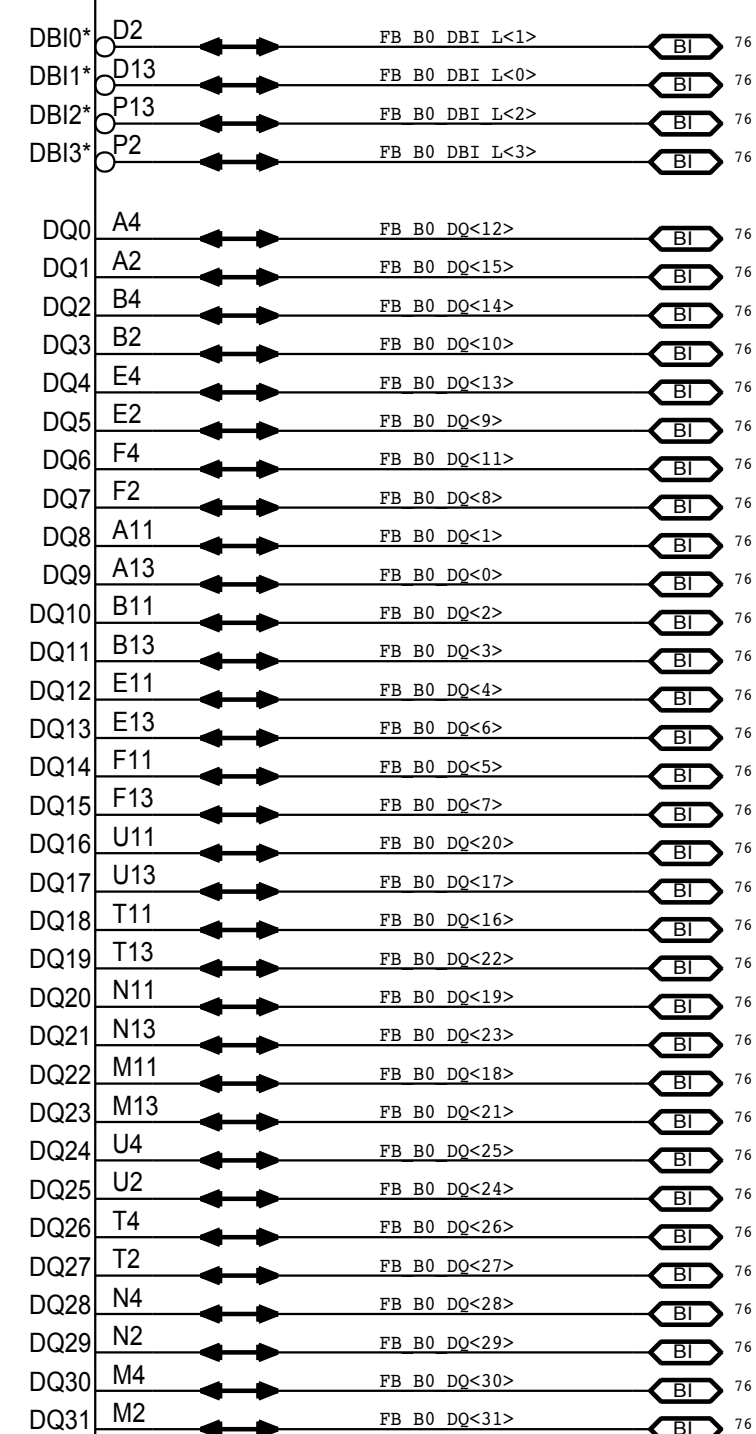
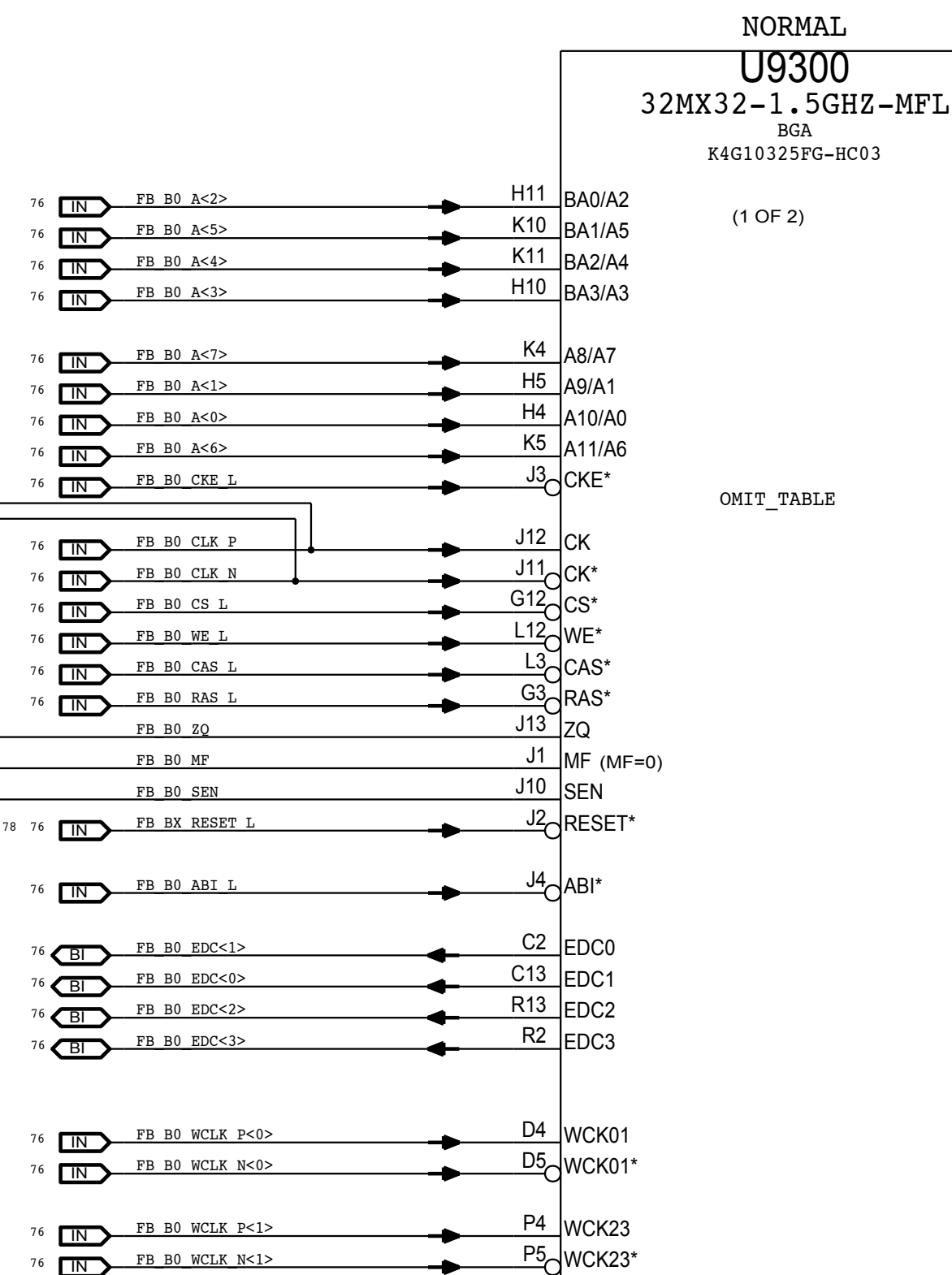
Page Notes


Power aliases required by this page:

- #P91V35 50 GPU FBVIO

Signal aliases required by this page

BOM options provided by this page:



SYNC_MASTER=BRANCH_FYIYN		SYNC_DATE=09/18/2014	
PAGE TITLE			
GDDR5 Frame Buffer B			
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		BRANCH	
		PAGE	93 OF 121
		SHEET	78 OF 93

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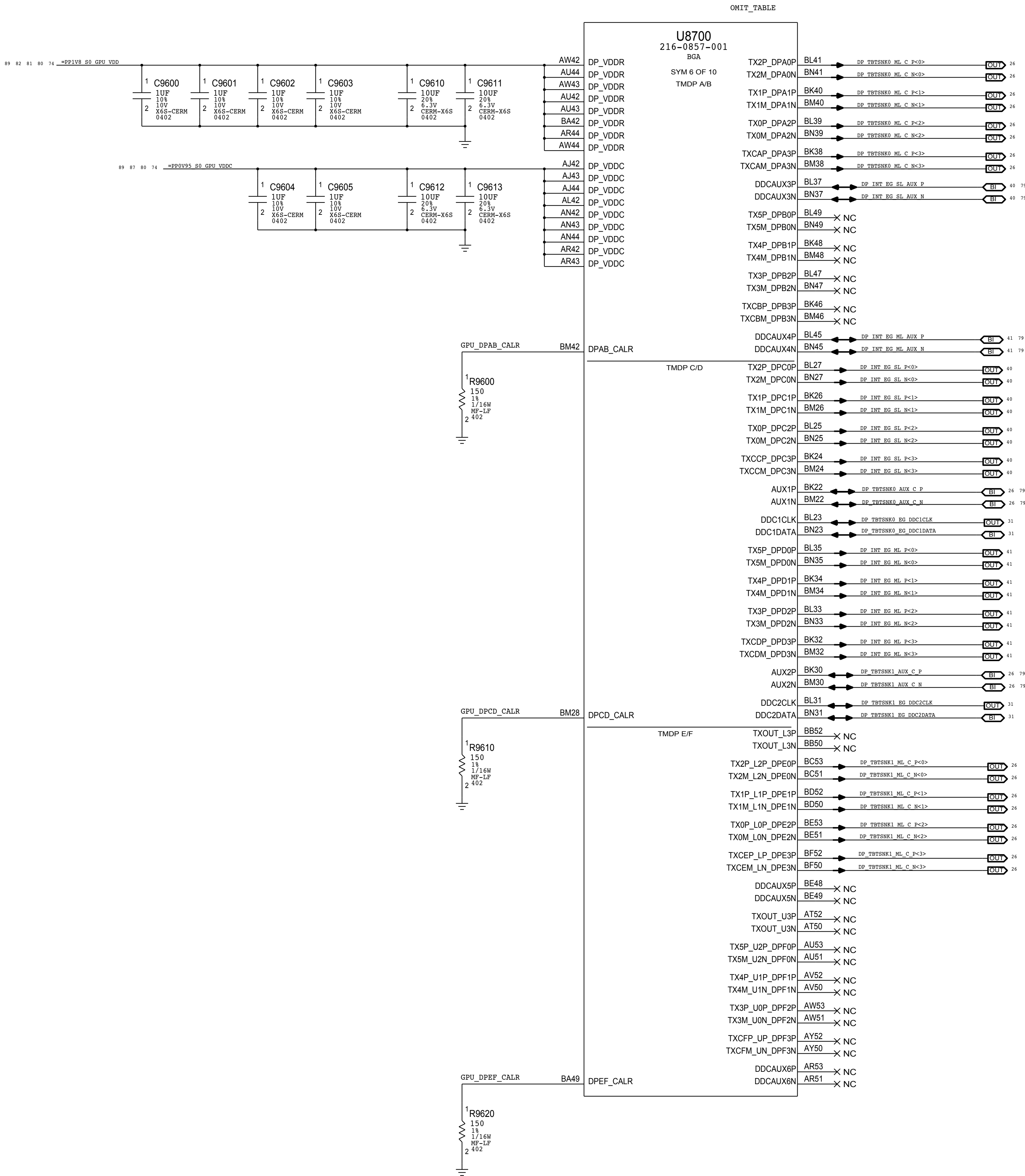
A

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A



Page Notes

Power aliases required by this page:

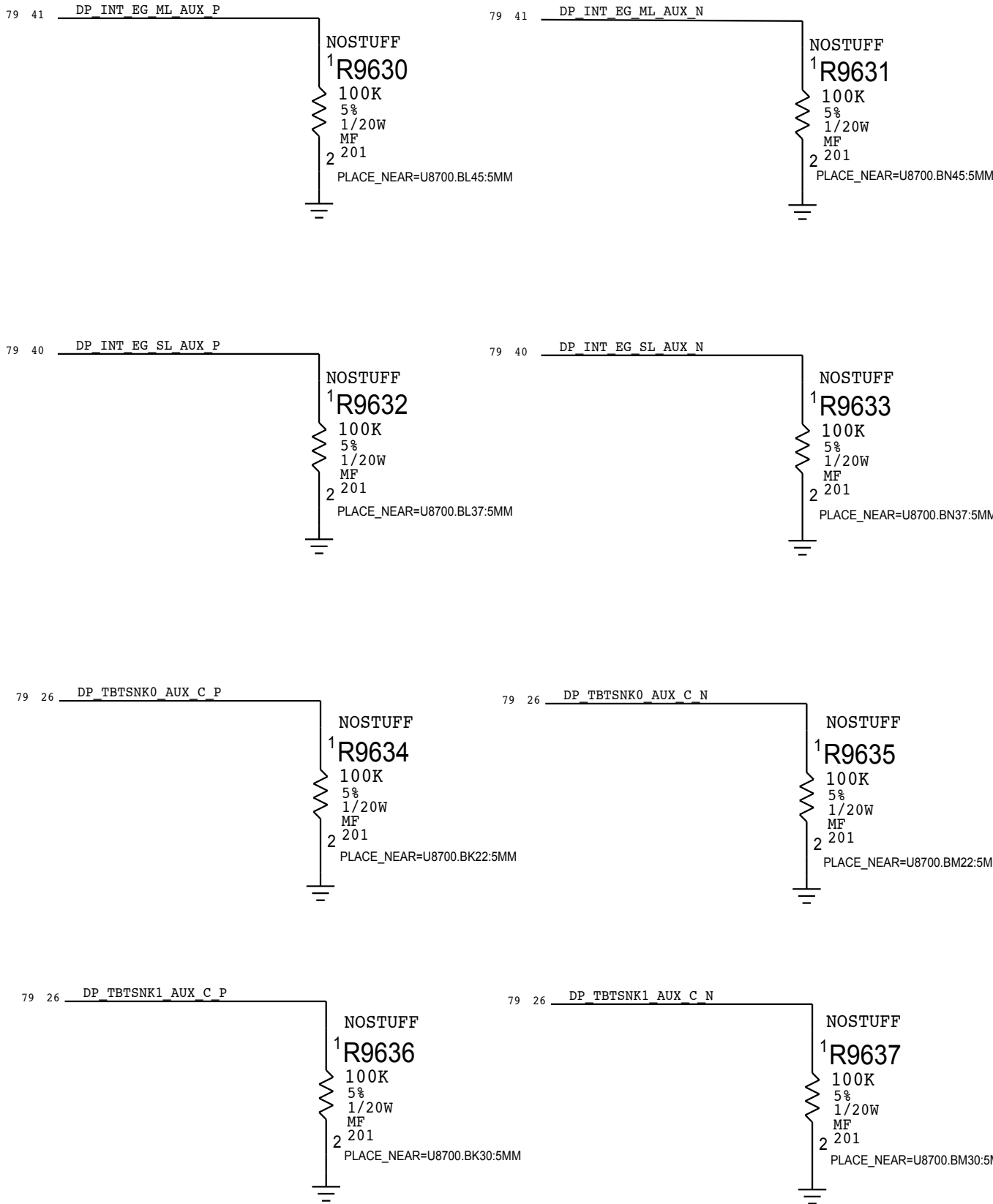
+ +VDD1_DP0_1200 + +VDD1_DP0_1200
+ +VDD1_DP0_1200 + +VDD1_DP0_1200
+ +VDD1_DP0_1200 + +VDD1_DP0_1200
+ +VDD1_DP0_1200 + +VDD1_DP0_1200


Signal aliases required by this page:

(NONE)

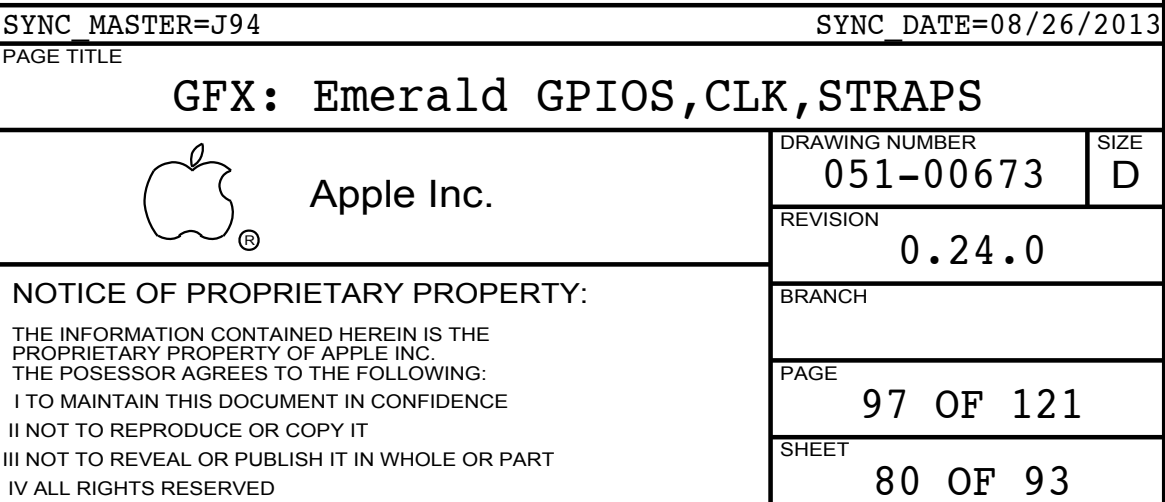
SW options provided by this page:

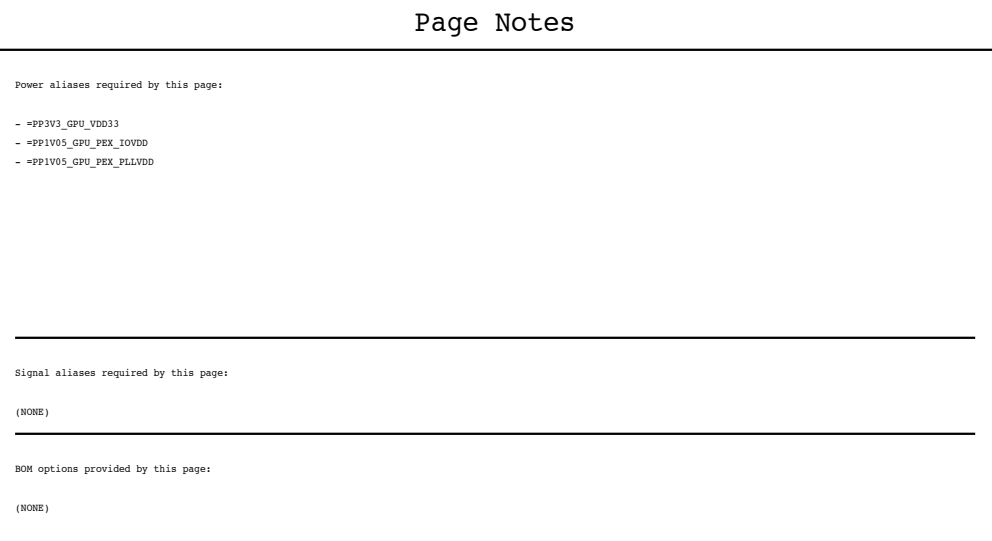
+ -211100
+ -211100



SYNC_MASTER=J94		SYNC_DATE=08/26/2013			
PAGE TITLE					
GFX: Emerald IntDP/TBT DP					
	Apple Inc.	DRAWING NUMBER	051-00673	SIZE	D
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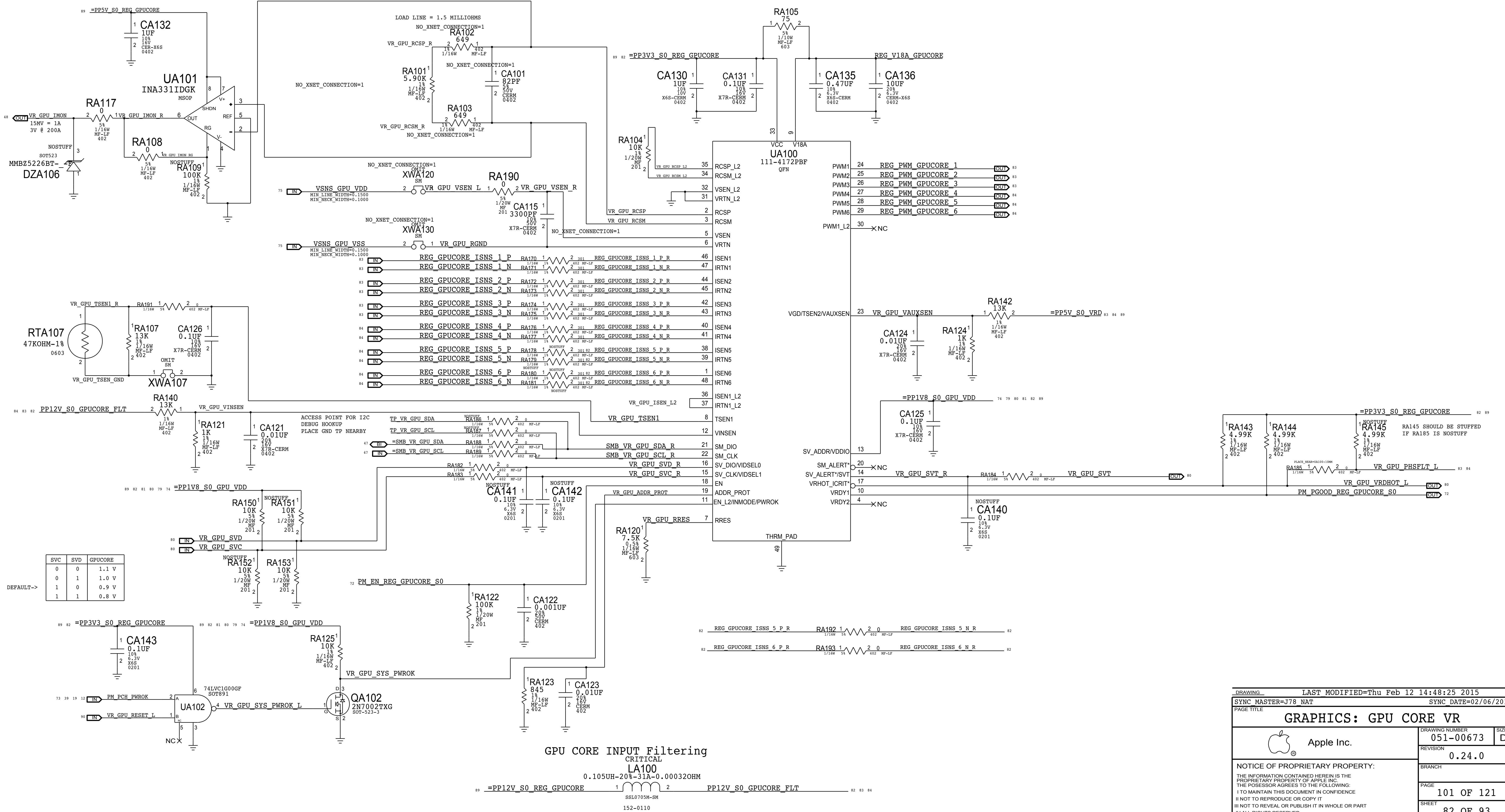
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O/P= PPGPUCORE_S0_REG

GPUCORE
VOUT = VCORE
PEAK = 195A
AVG = 154A



DRAWING		LAST MODIFIED=Thu Feb 12 14:48:25 2015	
SYNC MASTER=J78 NAT		SYNC DATE=02/06/2014	
PAGE TITLE			
GRAPHICS: GPU CORE VR			
 Apple Inc.		DRAWING NUMBER	051-00673
		REVISION	0.24.0
		BRANCH	
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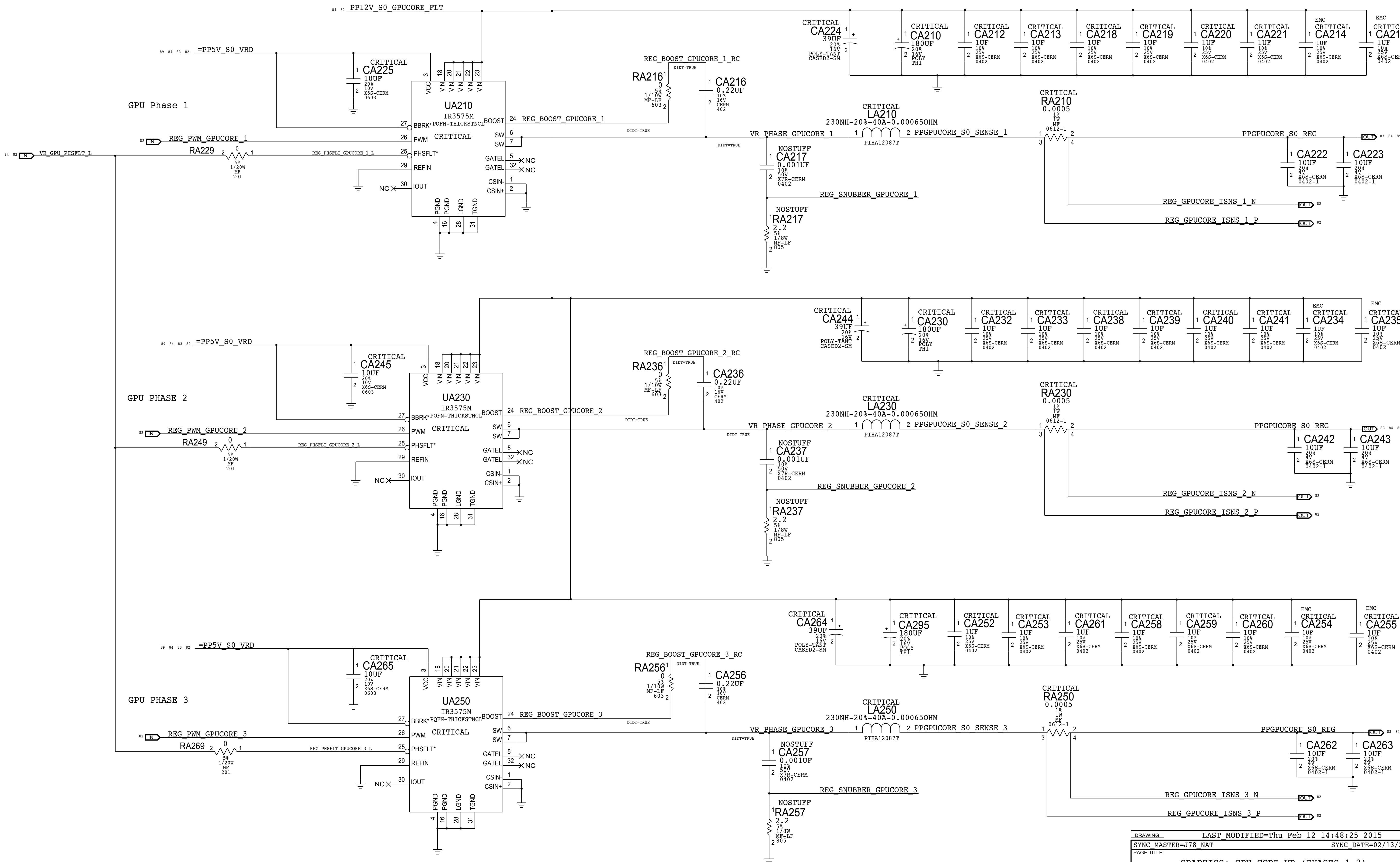
A

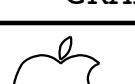
D

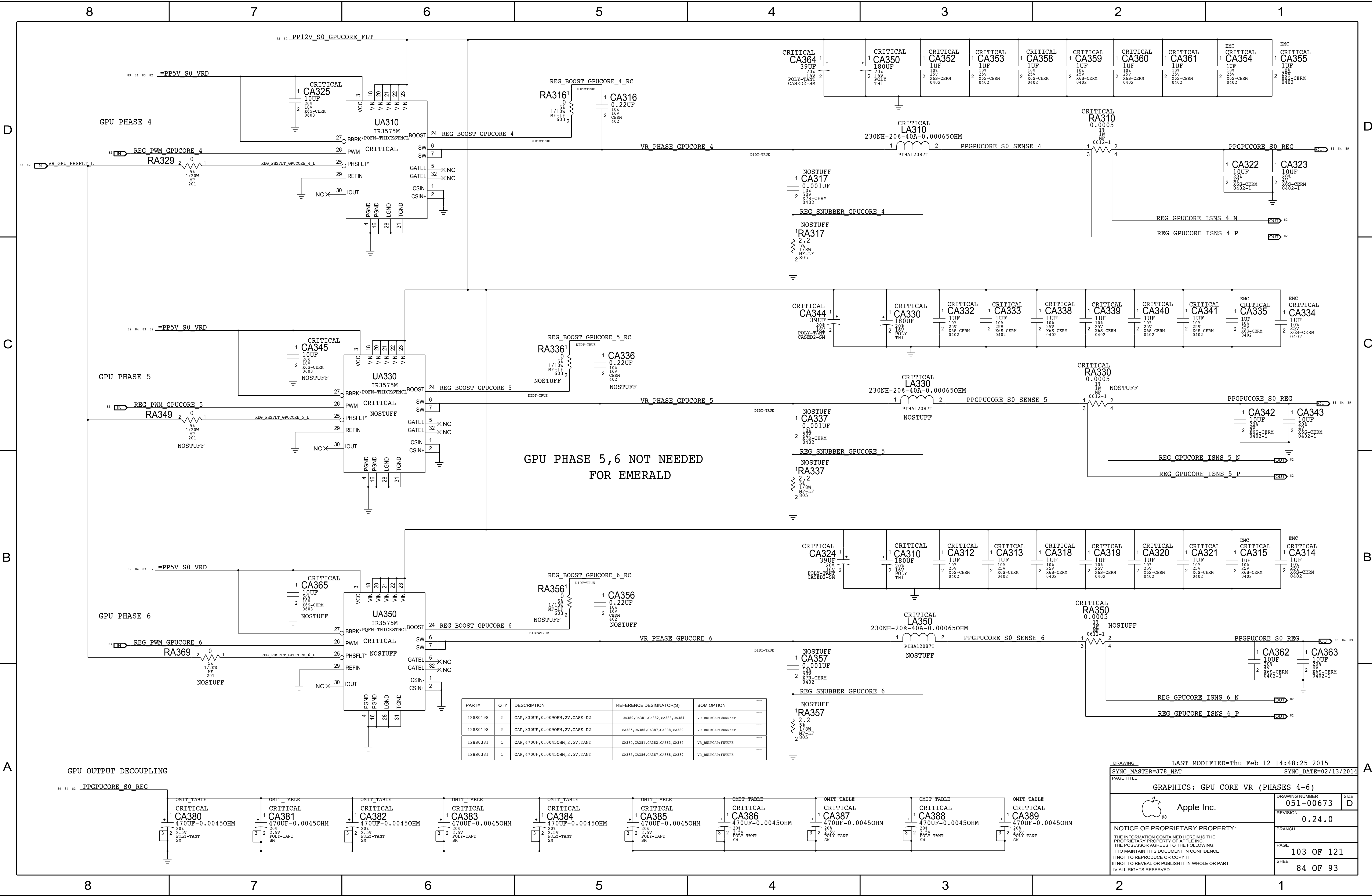
C

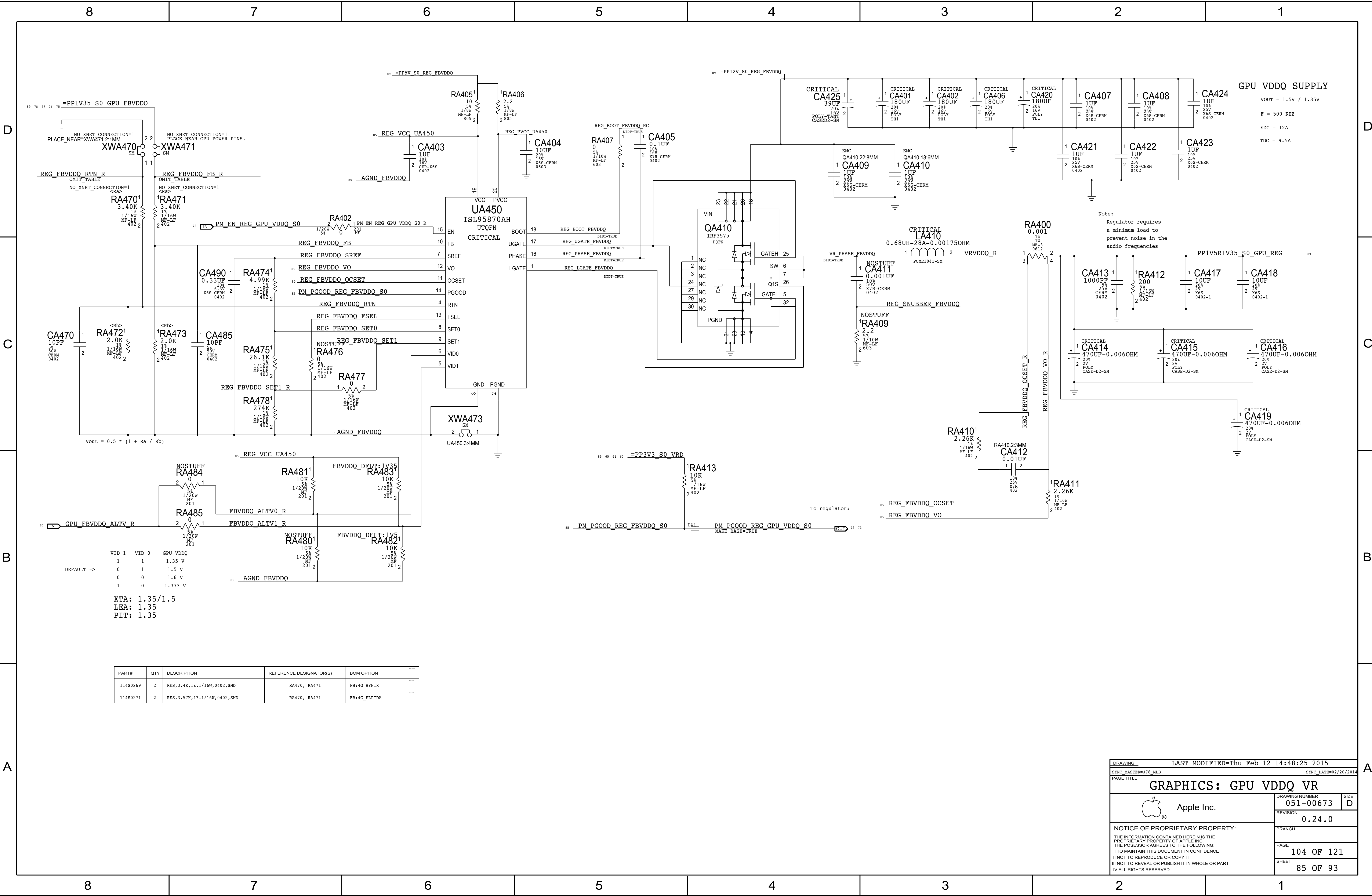
B

A



DRAWING		LAST MODIFIED=Thu Feb 12 14:48:25 2015	
SYNC MASTER=J78 NAT		SYNC DATE=02/13/2014	
PAGE TITLE			
GRAPHICS: GPU CORE VR (PHASES 1-3)			
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	051-00673		D
	REVISION		
	0.24.0		
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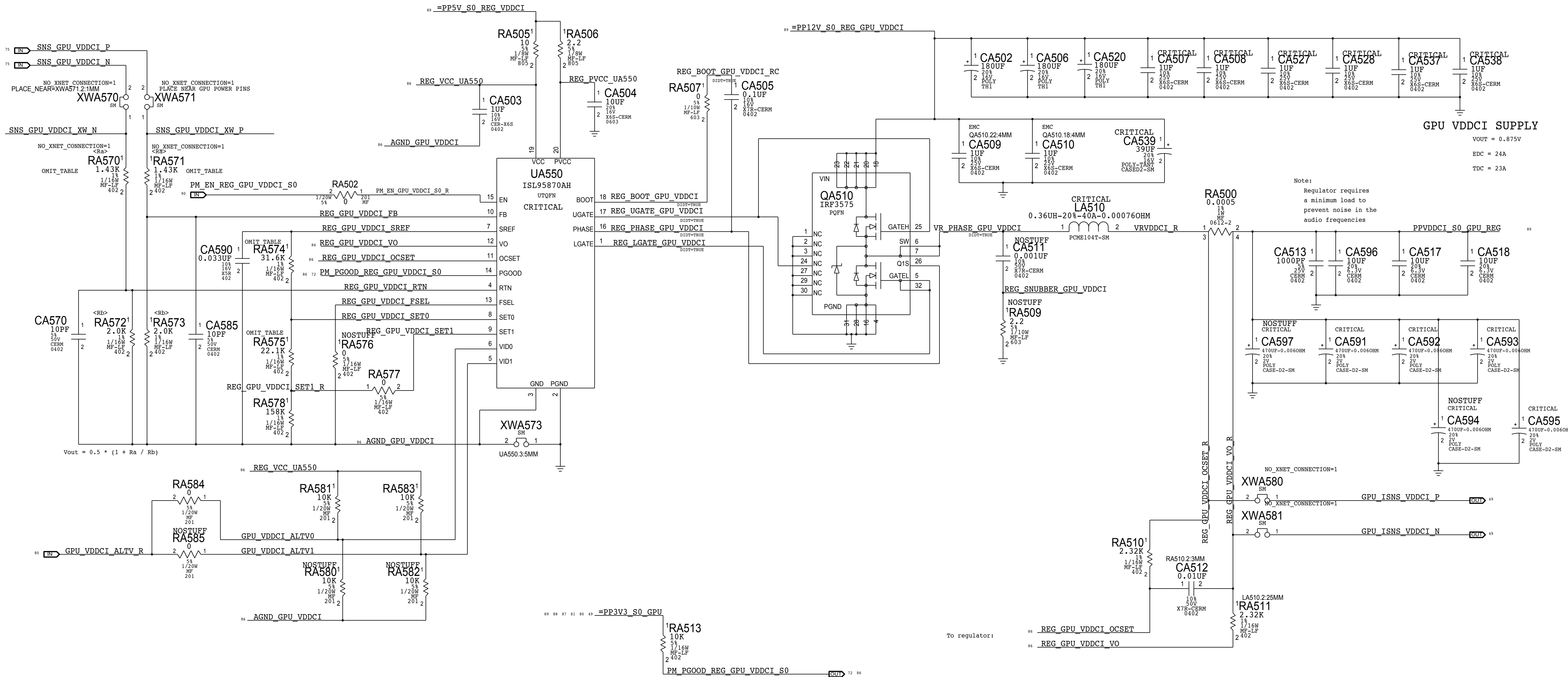
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NEPTUNE			AMETHYST		
VID 1	VID 0	GPU VDDCI	VID 1	VID 0	GPU VDDCI
DEFAULT ->	1	1	0.850 V	DEFAULT ->	1
	1	0	1.000 V		1
					0
					1.000 V


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11480363	1	RES,31.6K,0402	RA574	GPU_Emerald
11680068	2	RES,1.2K,0402	RA570,RA571	GPU_Emerald
11480378	1	RES,45.3K,0402	RA575	GPU_Emerald
11480363	1	RES,31.6K,0402	RA574	GPU_Neptune
11480231	2	RES,1.4K,0402	RA570,RA571	GPU_Neptune
11480347	1	RES,22.1K,0402	RA575	GPU_Neptune
11480373	1	RES,40.2K,0402	RA574	GPU_AmethystP_XTA
11480228	2	RES,1.3K,0402	RA570,RA571	GPU_AmethystP_XTA
11480347	1	RES,22.1K,0402	RA575	GPU_AmethystP_XTA
11480382	1	RES,48.7K,0402	RA574	GPU_AmethystP_PROA
11480228	2	RES,1.3K,0402	RA570,RA571	GPU_AmethystP_PROA
11480347	1	RES,22.1K,0402	RA575	GPU_AmethystP_PROA

SYNC_MASTER=hcheng_j95

SYNC_DATE=02/10/2015

PAGE TITLE

GRAPHICS: GPU VDDCI VR

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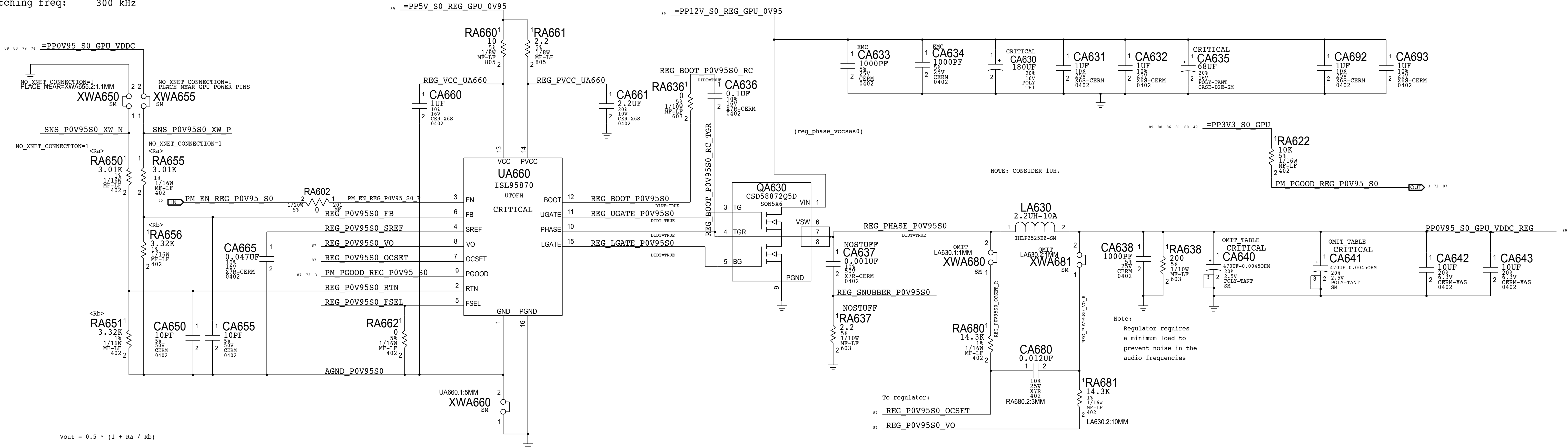
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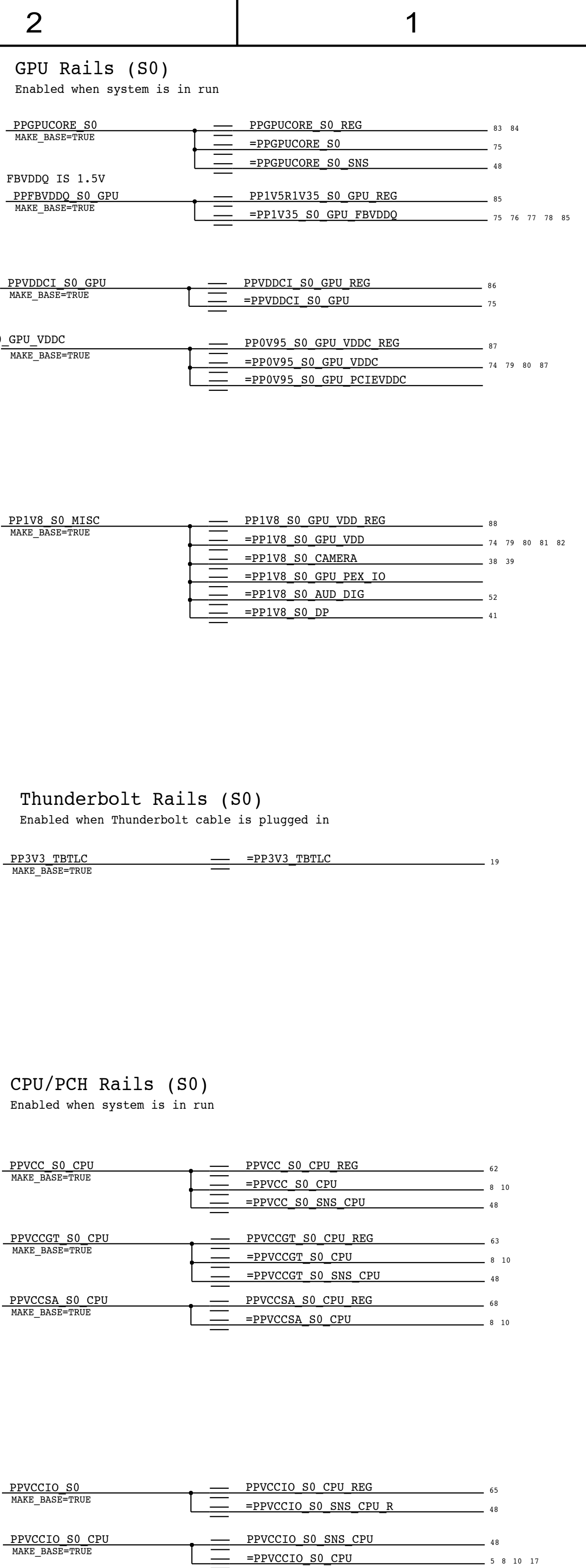
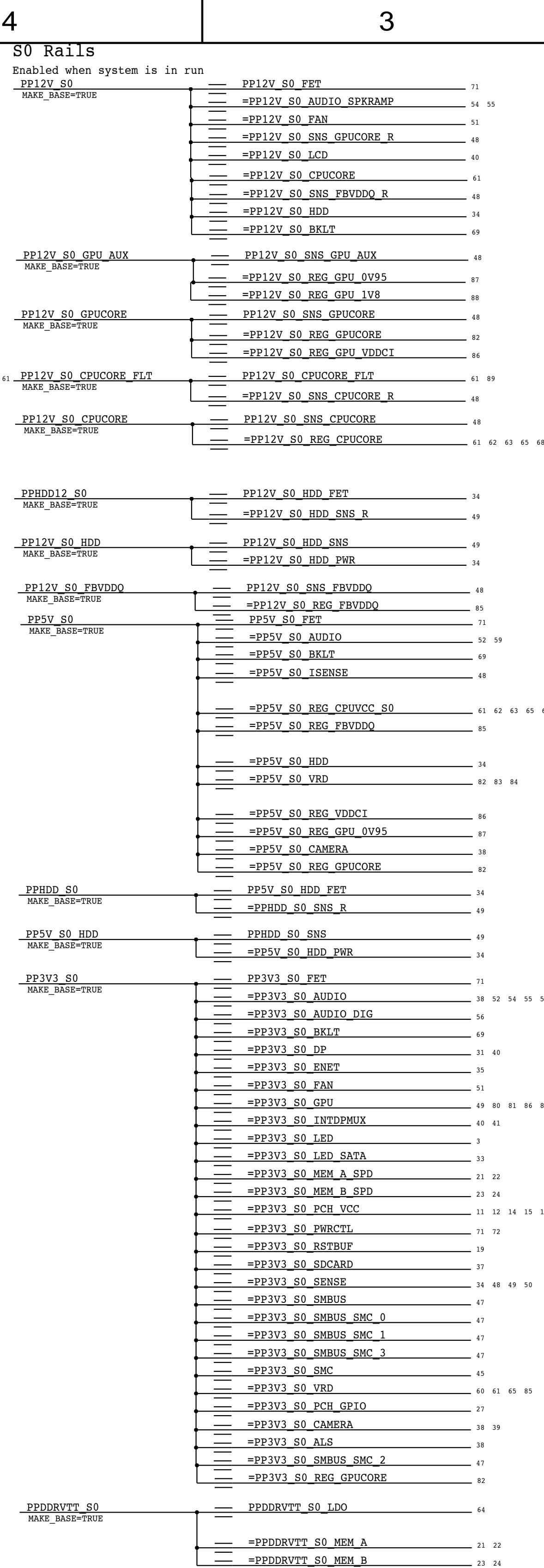
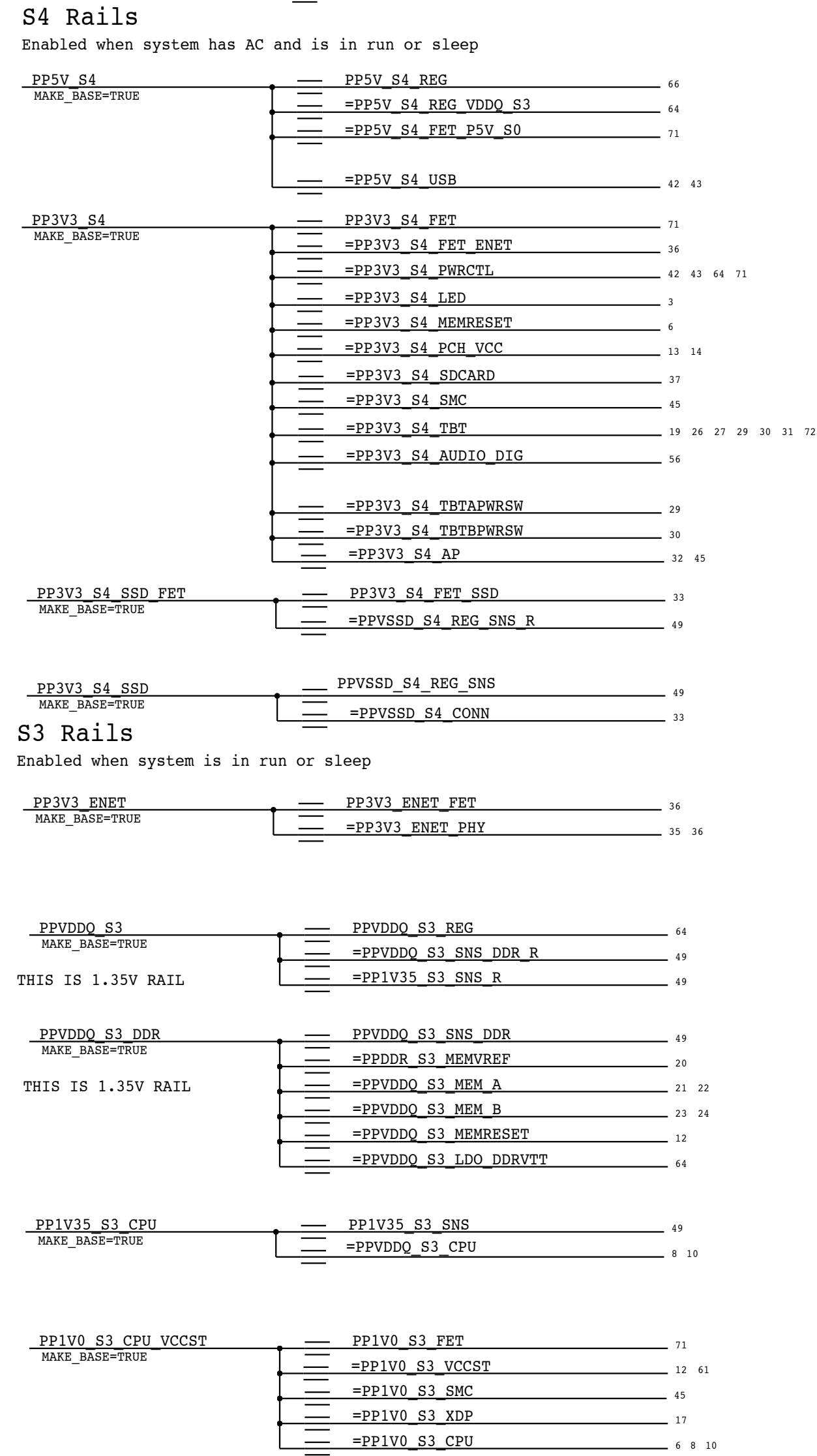
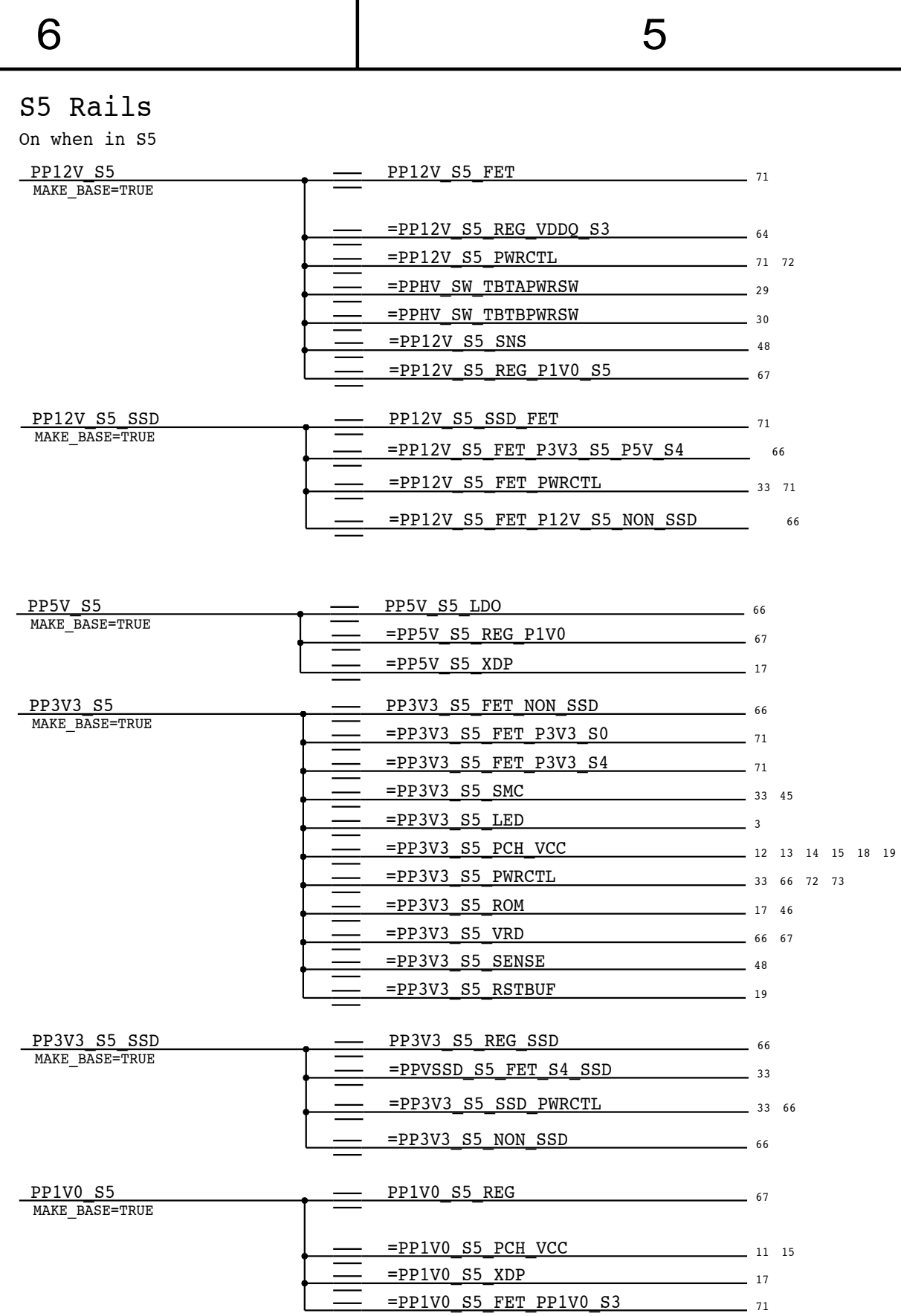
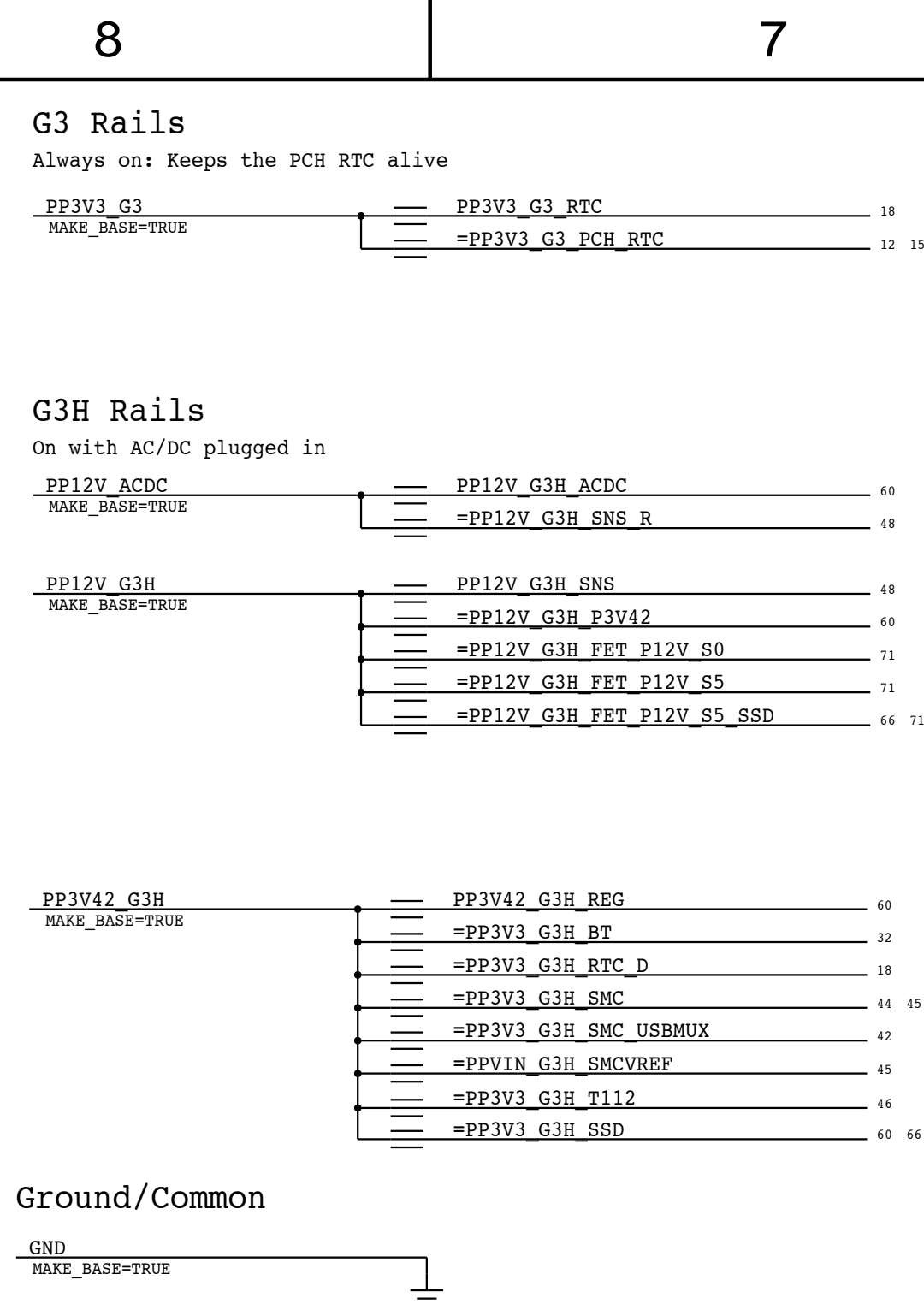
GPU VDDC (0.95V) S0 REGULATOR


Max avg current: 4.3 A
Max peak current: 4.5 A
Switching freq: 300 kHz



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
12880358	2	CAP, 470uF, 0.0060HM, 2V, D2	CA640, CA641	VR_BULKCAP:CURRENT
12880381	2	CAP, 470uF, 0.00450HM, 2.5V, SM	CA640, CA641	VR_BULKCAP:FUTURE

DRAWING		LAST MODIFIED=Thu Feb 12 14:48:26 2015			
SYNC_MASTER=J78_MLB		SYNC_DATE=08/02/2014			
PAGE TITLE					
GRAPHICS: GPU 0V95 VR					
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		051-00673		D	
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		BRANCH			
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PAGE TITLE			
Power Connectors/Aliases			
 Apple Inc.	DRAWING NUMBER		SIZE
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	REVISION		
		0.24.0	
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PEG aliases


74	<u>PEG_D2R N<0..15></u>	MAKE BASE=TRUE	==	=PEG_D2R N<15..0>	5
74	<u>PEG_D2R P<0..15></u>	MAKE BASE=TRUE	==	=PEG_D2R P<15..0>	5
74	<u>PEG_R2D C N<0..15></u>	MAKE BASE=TRUE	==	=PEG_R2D C N<15..0>	5
74	<u>PEG_R2D C P<0..15></u>	MAKE BASE=TRUE	==	=PEG_R2D C P<15..0>	5

GPU ALIASES

80	74	<u>GPU_RESET_L</u>	<u>TP_GPU_RESET_L</u>	19
		MAKE_BASE=TRUE		
82		<u>VR_GPU_RESET_L</u>	<u>TP_VR_GPU_RESET_L</u>	19
		MAKE_BASE=TRUE		

```
GPU VDDCI PGOOD
```

```
72 TP PM EN REG GPU VDDCI S0      — PM EN REG GPU VDDCI S0      86
                                     — MAKE_BASE=TRUE
```

SYNC MASTER=J78 MLB		SYNC DATE=12/05/2013	
PAGE TITLE			
Signal Aliases			
	Apple Inc.		DRAWING NUMBER 051-00673
			SIZE D
		REVISION 0.24.0	
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	8	7	6	5	4	3	2	1	
D	<div>CPU Reserved</div> <div><div><div>176CPU_CFG<15..12>TP_CPU_CFG<15..12>MAKE_BASE=TRUE</div><div>40_DP_INT_PIN_57NC_DP_INT_PIN_57MAKE_BASE=TRUE</div><div>40_DP_INT_PIN_55NC_DP_INT_PIN_55MAKE_BASE=TRUE</div></div><div><div>12_TP_CLINK_DATACLINK_DATAMAKE_BASE=TRUENO_TEST=1</div><div>12_TP_CLINK_CLKCLINK_CLKMAKE_BASE=TRUENO_TEST=1</div><div>12_TP_CLINK_RESET_LCLINK_RESET_LMAKE_BASE=TRUENO_TEST=1</div><div>TP_GPU_CB_REFCKN_OUT1GPU_CB_REFCKN_OUT1MAKE_BASE=TRUE</div><div>TP_GPU_CB_REFCKP_OUT1GPU_CB_REFCKP_OUT1MAKE_BASE=TRUE</div><div>TP_GPU_PLL_ANALOG_INGPU_PLL_ANALOG_INMAKE_BASE=TRUE</div><div>12_TP_PCH_SLP_LAN_LPCH_SLP_LAN_LMAKE_BASE=TRUENO_TEST=1</div><div>11_TP_PCH_2PCH_2MAKE_BASE=TRUENO_TEST=1</div><div>12_TP_PM_SLP_A_LPMSLP_A_LMAKE_BASE=TRUENO_TEST=1</div><div>26_TP_TBT_MONDC1TBT_MONDC1MAKE_BASE=TRUE</div><div>26_TP_TBT_PCIE_RESET0_LTBT_PCIE_RESET0_LMAKE_BASE=TRUENO_TEST=1</div></div></div> <td>D</td>								D
C	<div>PCH Clocks</div> <div><div>TP_ITPXDP_CLK100MPTITXDP_CLK100M_PMAKE_BASE=TRUENO_TEST=11117</div><div>TP_ITPXDP_CLK100MNTITXDP_CLK100M_NMAKE_BASE=TRUENO_TEST=11117</div></div>								C
	<div>PCH Miscellaneous</div> <div><div>11_TP_HDA_SDIN1NC_HDA_SDIN1MAKE_BASE=TRUENO_TEST=1</div></div>								
	<div><div>11_PEG_CLKREQ_LNC_PEG_CLKREQ_LMAKE_BASE=TRUE</div><div>8014_GPU_NEPTUNE_EMERALD_IDNC_GPU_IS_AMETHYSTMAKE_BASE=TRUENO_TEST=1</div></div>								
B									B
A									A
	8	7	6	5	4	3	2	1	

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SYNC DATE=12/05/2013

PAGE TITLE

Unused Signal Aliases



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J17 BOARD SPECIFIC PHYSICAL AND SPACING CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM	NO_TYPE, BGA, BGA_TBT, BGA_VRAM	MM	16.2

General Physical Rule Definitions

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.1 MM	0.070 MM	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
34_OHM_SE	*	Y	0.185 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
34_OHM_SE	ISL5, ISL8	Y	0.205 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
34_OHM_SE	TOP, BOTTOM	Y	0.220 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
39_OHM_SE	*	Y	0.150 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
39_OHM_SE	ISL5, ISL8	Y	0.165 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
39_OHM_SE	TOP, BOTTOM	Y	0.175 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
42_OHM_SE	*	Y	0.130 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
42_OHM_SE	ISL5, ISL8	Y	0.145 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
42_OHM_SE	TOP, BOTTOM	Y	0.155 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	*	Y	0.115 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	ISL5, ISL8	Y	0.126 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	TOP, BOTTOM	Y	0.135 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	0.090 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	ISL5, ISL8	Y	0.100 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP, BOTTOM	Y	0.105 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	0.075 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	ISL5, ISL8	Y	0.080 MM	0.080 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP, BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
68_OHM_DIFF	*	Y	0.171 MM	0.085 MM	=STANDARD	0.130 MM	0.1 MM
68_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.085 MM	=STANDARD	0.150 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.136 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.141 MM	0.085 MM	=STANDARD	0.185 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.121 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.109 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.111 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.086 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.090 MM	0.085 MM	=STANDARD	0.230 MM	0.1 MM

General Spacing Definitions

Default

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

Fixed and Dielectric

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1X_DIELECTRIC	TOP,BOTTOM	0.071 MM	?
1X_DIELECTRIC	ISL3,ISL10	0.101 MM	?
1X_DIELECTRIC	*	0.076 MM	?

Board Stack-up

FINISHED BOARD THICKNESS: 1.94 MM

-----	Top	Signal	0.5 oz (Cu plated)
-----		Prepreg	0.071 MM
-----	2	Plane	1 oz
-----		Core	0.101 MM
-----	3	Signal	0.5 oz
-----		Prepreg	0.115 MM
-----	4	Plane	1 oz
-----		Core	0.076 MM
-----	5	Signal	0.5 oz
-----		Prepreg	0.380 MM
-----	6	Plane	1 oz
-----		Core	0.076 MM
-----	7	Plane	1 oz
-----		Prepreg	0.380 MM
-----	8	Signal	0.5 oz
-----		Core	0.076 MM
-----	9	Plane	1 oz
-----		Prepreg	0.115 MM
-----	10	Signal	0.5 oz
-----		Core	0.101 MM
-----	11	Plane	1 oz
-----		Prepreg	0.071 MM
-----	Btm	Signal	0.5 oz (Cu plated)

BGA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=STANDARD	?

Power and Common


SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_ISO	*	=STANDARD	8000
GND_P2MM	*	=2:1_SPACING	1000
PWR_P2MM	*	=2:1_SPACING	1100

GENERIC

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GENERIC_ISO	*	=1:1 SPACING	?

BGA Area Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM

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