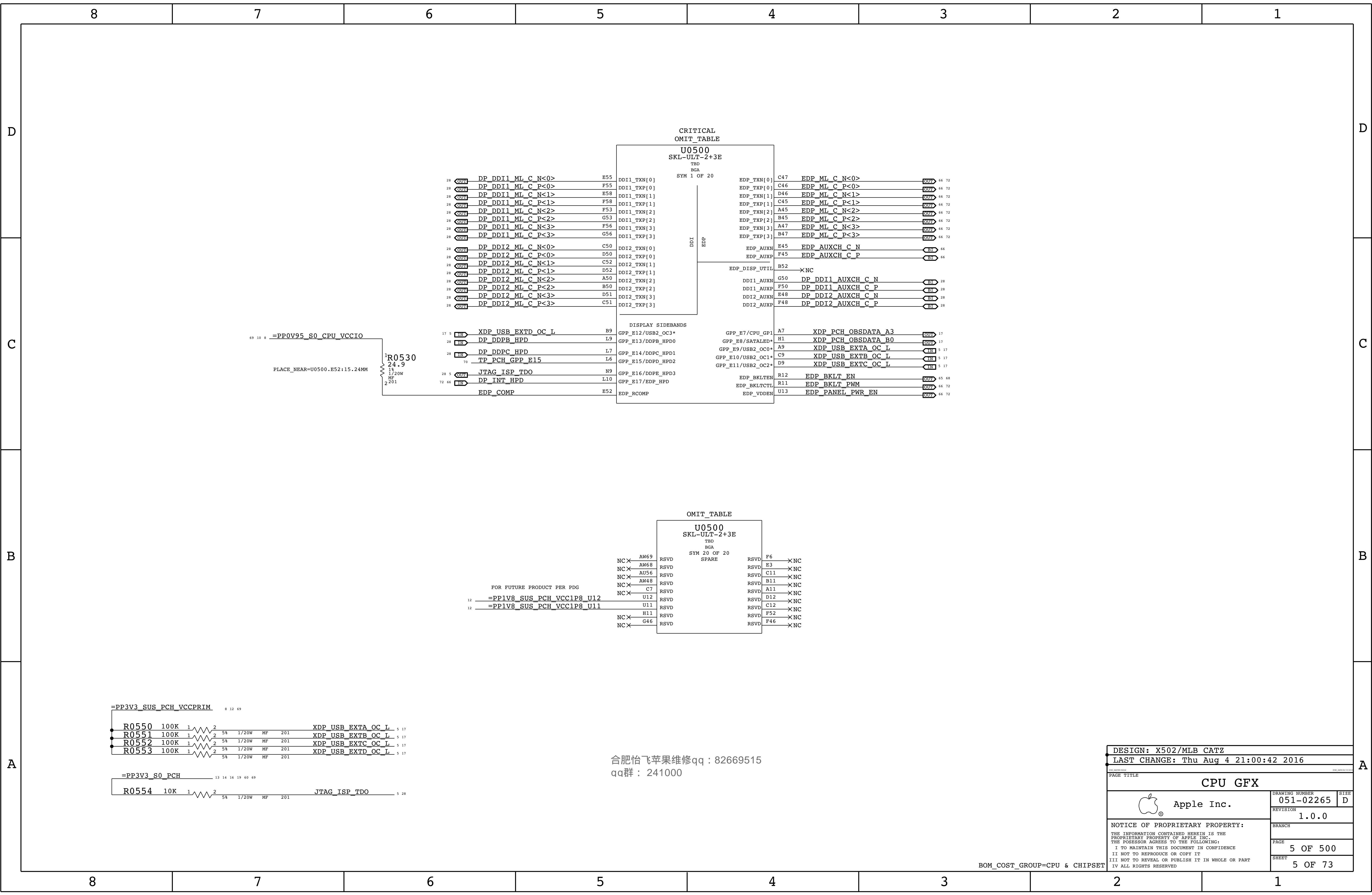
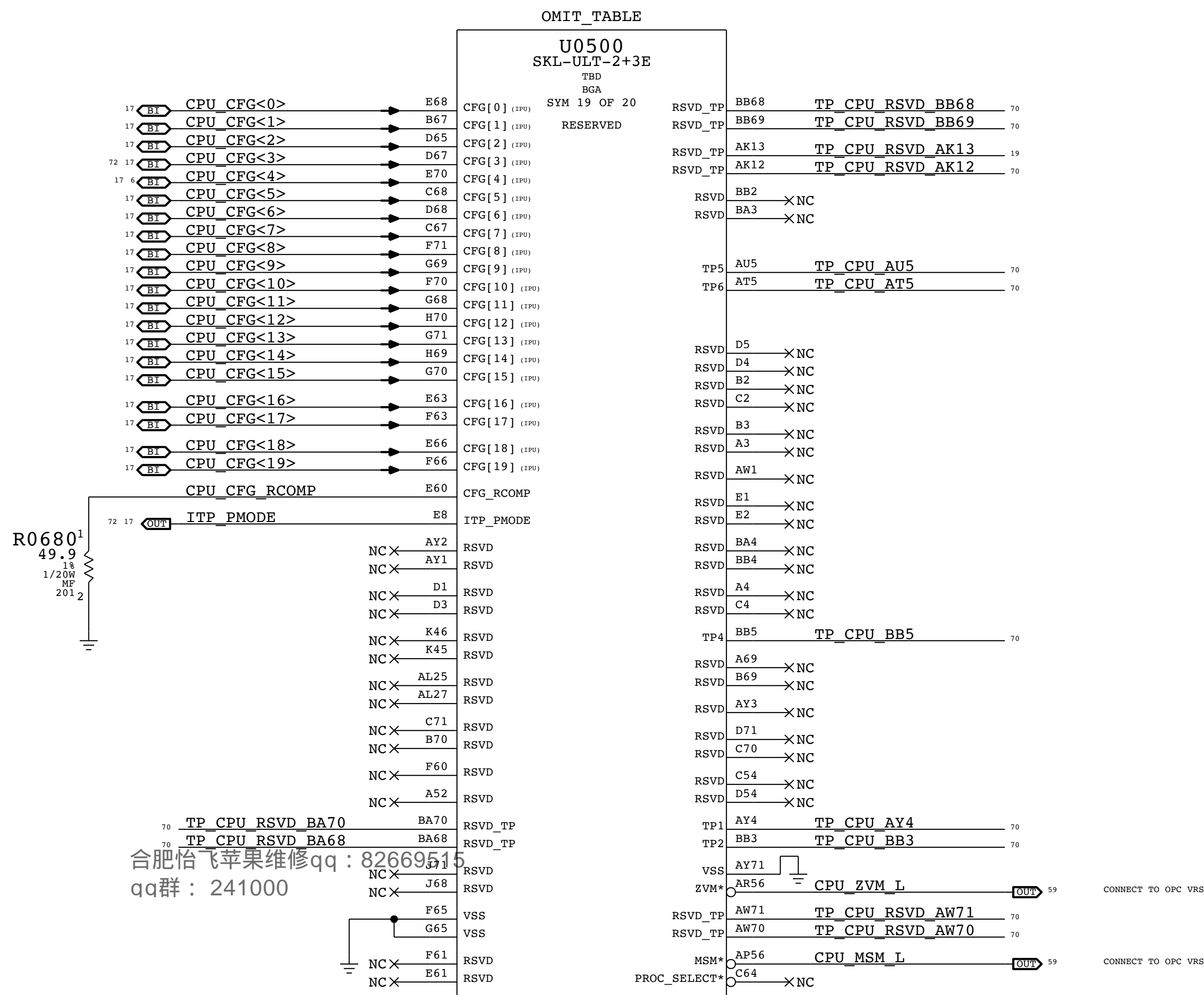
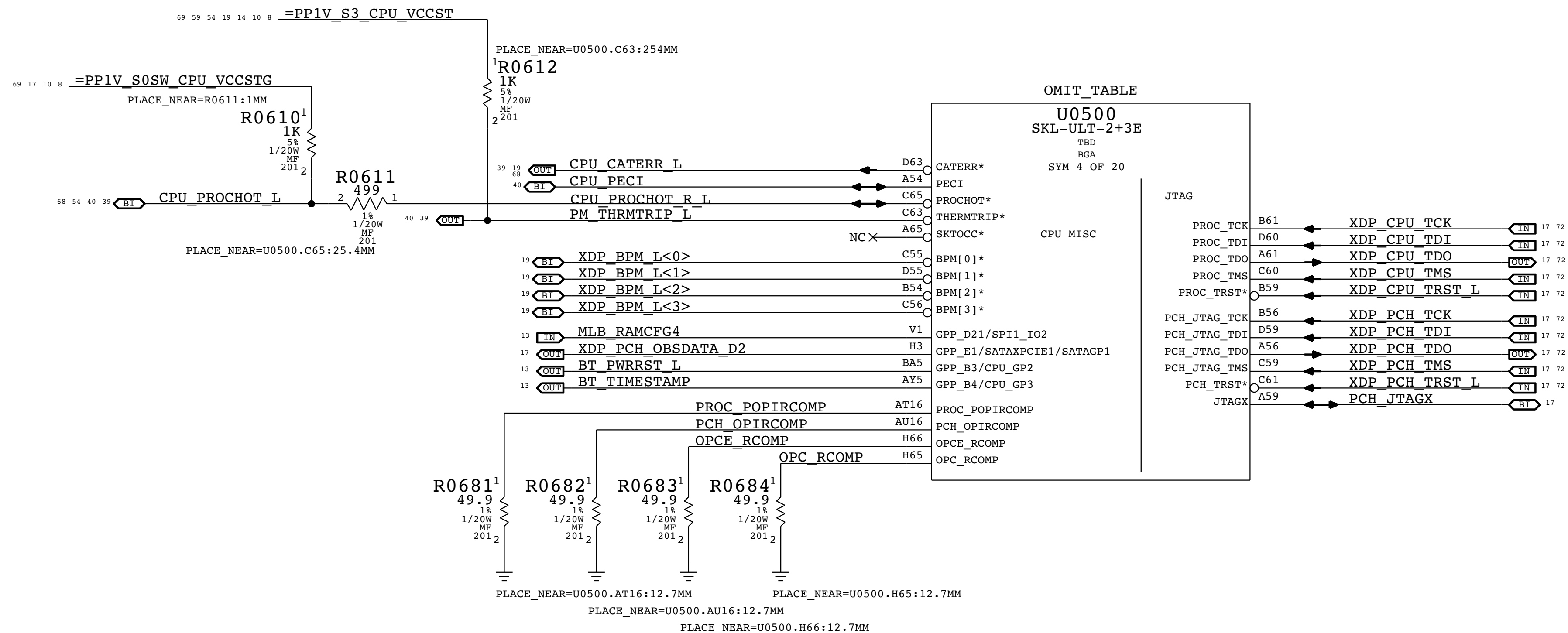
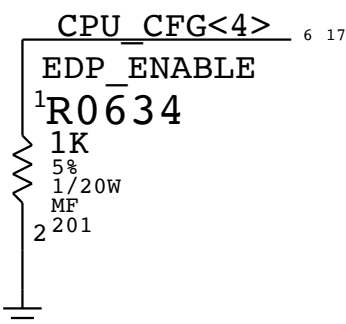



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LAST CHANGE: Tue Aug 9 17:02:57 2016															
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LAST_MODIFICATION=Tue Aug 9 17:03:06 2016															
PAGE CSA CONTENTS SYNC DATE															
1 1 Table of Contents															
2 2 BOM Configuration PAULM 06/15/2015															
3 3 BOM Configuration PAULM 06/15/2015															
4 4 PD Parts PAULM 06/15/2015															
5 5 CPU GFX PAULM 06/15/2015															
6 6 CPU MISC/JTAG/CFG/RSVD PAULM 06/15/2015															
7 7 CPU LPDDR3 Interface PAULM 06/15/2015															
8 8 CPU & PCH Power PAULM 06/15/2015															
9 9 CPU & PCH Grounds PAULM 06/15/2015															
10 10 CPU Core Decoupling PAULM 06/15/2015															
11 11 CPU GT Decoupling															
12 12 PCH Decoupling															
13 13 PCH Audio/LPC/SPI/SMBus															
14 14 PCH Power Management															
15 15 PCH PCIE/USB/CLKS															
16 16 PCH SPI/UART/GPIO															
17 18 CPU/PCH Merged XDP															
18 19 Chipset Support 1															
19 20 Chipset Support 2															
20 22 LPDDR3 VREF Margining															
21 23 LPDDR3 DRAM Channel A (00-31)															
22 24 LPDDR3 DRAM Channel A (32-63)															
23 25 LPDDR3 DRAM Channel B (00-31)															
24 26 LPDDR3 DRAM Channel B (32-63)															
25 27 LPDDR3 DRAM Termination															
26 28 USB-C HIGH SPEED 1															
27 29 USB-C HIGH SPEED 2															
28 30 USB-C SUPPORT															
29 31 USB-C PORT CONTROLLER A															
30 32 USB-C PORT CONTROLLER B															
31 33 USB-C CONNECTOR A															
32 34 USB-C CONNECTOR B															
33 35 USB-C SUPPORT 2															
34 37 WIFI/BT MODULE															
35 38 WIFI/BT Module Support															
36 39 CAMERA 1 OF 2															
37 40 CAMERA 2 OF 2															
38 48 P1:KEYBOARD & TRACKPAD CONN															
39 50 SMC															
40 51 SMC Shared Support															
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41 52 SMC Project Support PAULM 06/15/2015															
42 53 SMBus Connections PAULM 06/15/2015															
43 54 Power Sensors High Side PAULM 06/15/2015															
44 55 Power Sensors Load Side PAULM 06/15/2015															
45 56 Power Sensors Extended PAULM 06/15/2015															
46 58 Thermal Sensors PAULM 06/15/2015															
47 61 SPI ROM & SWD Debug PAULM 06/15/2015															
48 62 HDA BRIDGE AHAAGE 03/23/2016															
49 63 JACK CODEC AHAAGE 09/22/2015															
50 64 SPEAKER AMP AHAAGE 03/23/2016															
51 66 JACK TRANSLATORS															
52 69 DC-IN & BATTERY CONNECTORS															
53 70 PBUS Supply & Battery Charger															
54 71 VReg CPU VCC Cntl															
55 72 CPU IMVP VCC & VCCSA															
56 73 IMVP VCCSA															
57 74 GT IMVP VCCGT															
58 76 VR - 5V S4, 3.3V S5															
59 77 VR - OPC (EDRAM)															
60 78 PMIC IC & Power Control															
61 79 PMIC VCCPCH VCCIO 1.8V															
62 80 PMIC 1.2V 1.0V 0.6V															
63 81 RAIL DESENSE CAPS															
64 82 Power FETs															
65 84 LCD Backlight Driver															
66 85 eDP Display Connector X362 06/23/2015															
67 86 SSD MODULE PAULM 06/15/2015															
68 99 DEVELOPMENT ONLY PAULM 06/15/2015															
69 100 Power Aliases X502-EXP 12/03/2015															
70 102 NC_ AND NO_TEST SIGNALS PAULM 06/15/2015															
71 103 Memory Signal Swaps X502-EXP 12/03/2015															
72 104 FCT, ICT PROPERTIES PAULM 06/15/2015															
73 500 =LAST SCHEMATIC PAGE= MICKLEE 06/23/2015															
DOCUMENTS / BOARDS / ASSEMBLIES															
PART NUMBER QTY DESCRIPTION REFERENCE DES CRITICAL BOM OPTION															
051-02265 1 SCHEM,MLB_CATZ,X502 SCH															
820-00875 1 PCBF,MLB_CATZ,X502 MLB CRITICAL															
639-03266 PCBA,MLB_CATZ,XXXXX,X502															
685-00125 1 COMMON PARTS,MLB_CATZ,X502 CBOM CMN_PARTS_BOM															
985-00239 1 DEV PARTS,MLB_CATZ,X502 DEV1 DEVELOPMENT_LIST															
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Table of Contents															
DRAWING TITLE SCHEM,MLB-CATZ,X502															
DRAWING NUMBER 051-02265 SIZE D															
REVISION 1.0.0															
BRANCH															
PAGE 1 OF 500															
SHEET 1 OF 73															
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8 7 6 5 4 3 2 1															



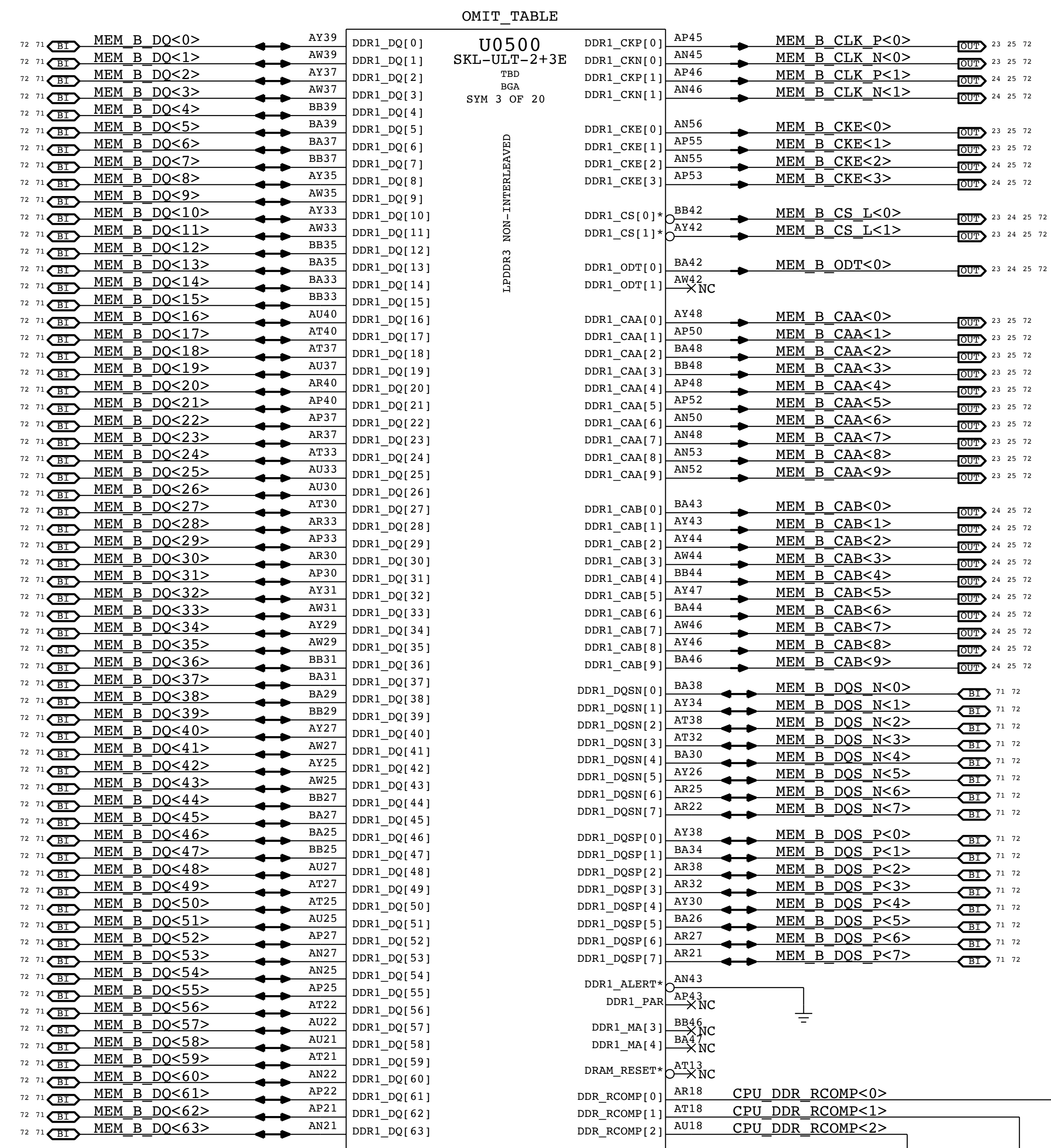
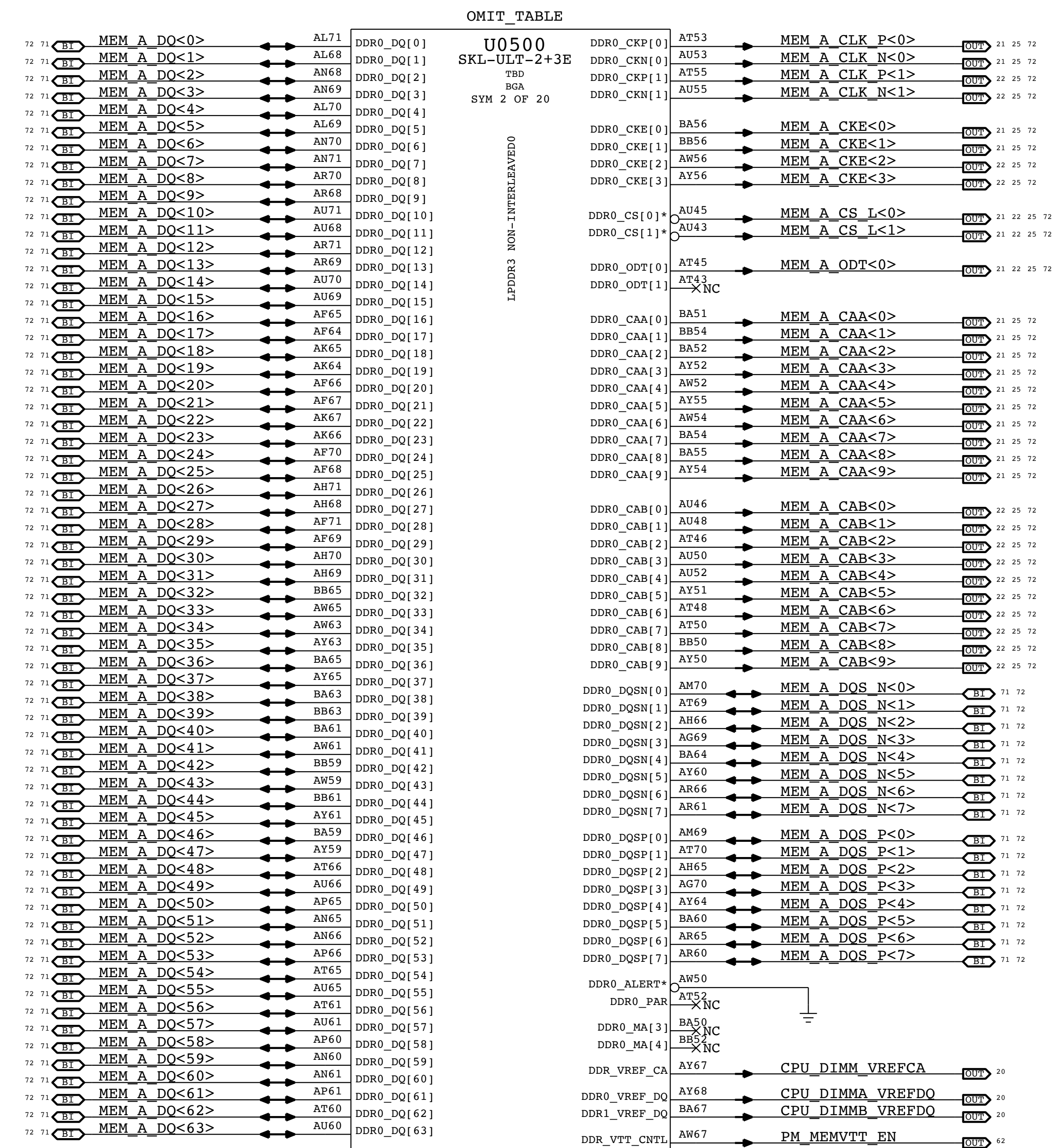


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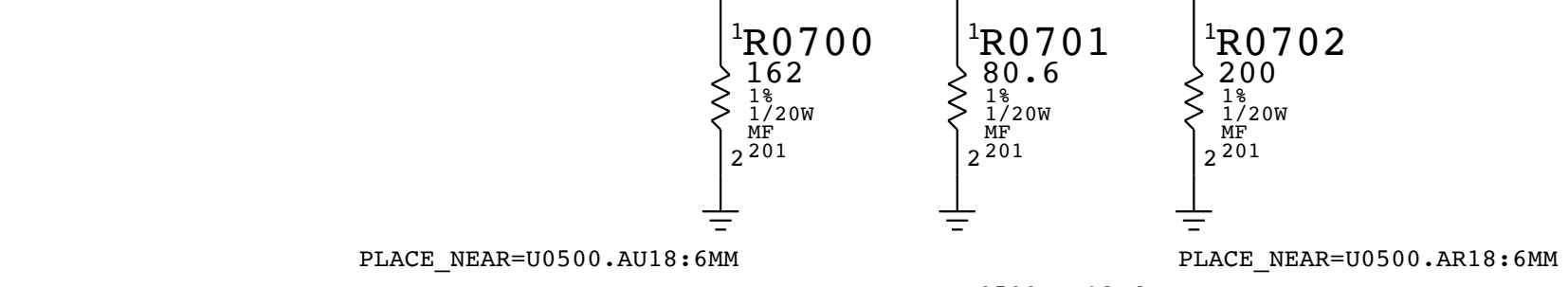



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LAST CHANGE: Thu Aug 4 21:00:42 2016			
PAGE TITLE			
CPU MISC/JTAG/CFG/RSVD			
 Apple Inc.	DRAWING NUMBER		SIZE
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		1.0.0	
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		PAGE	
		6 OF 500	
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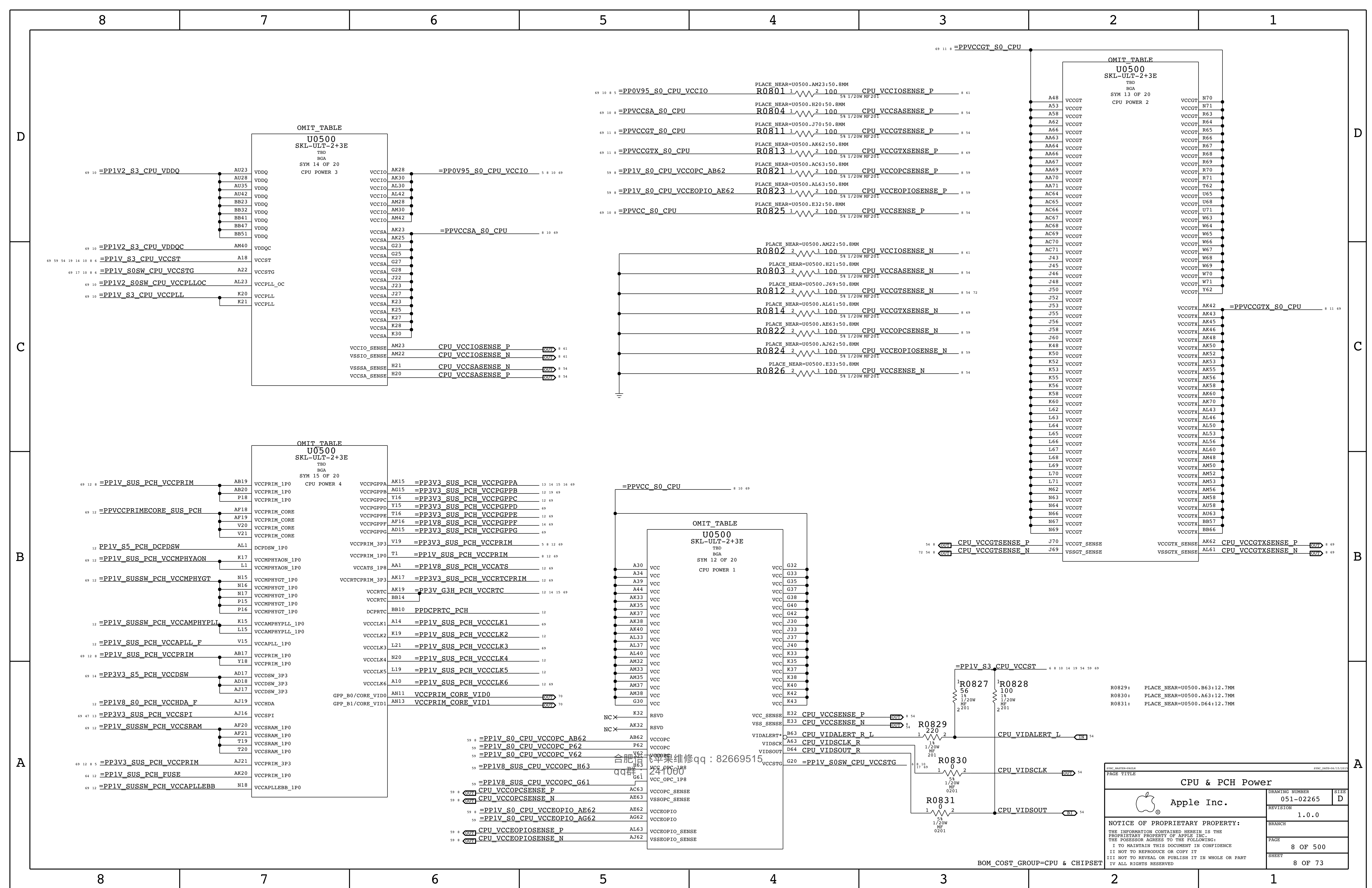


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CPU LPDDR3 Interface			
 Apple Inc.	DRAWING NUMBER		SIZE
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	REVISION		
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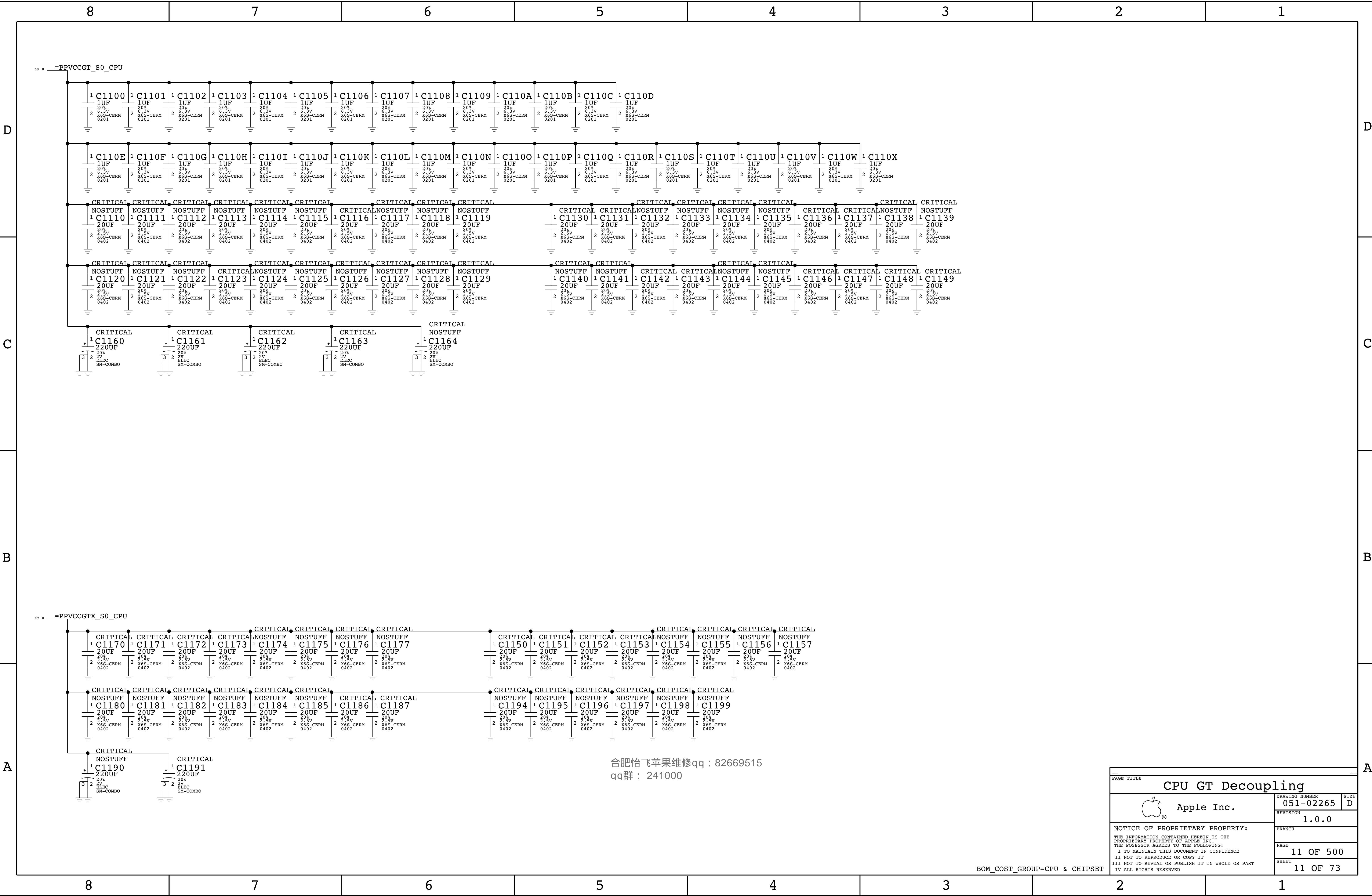
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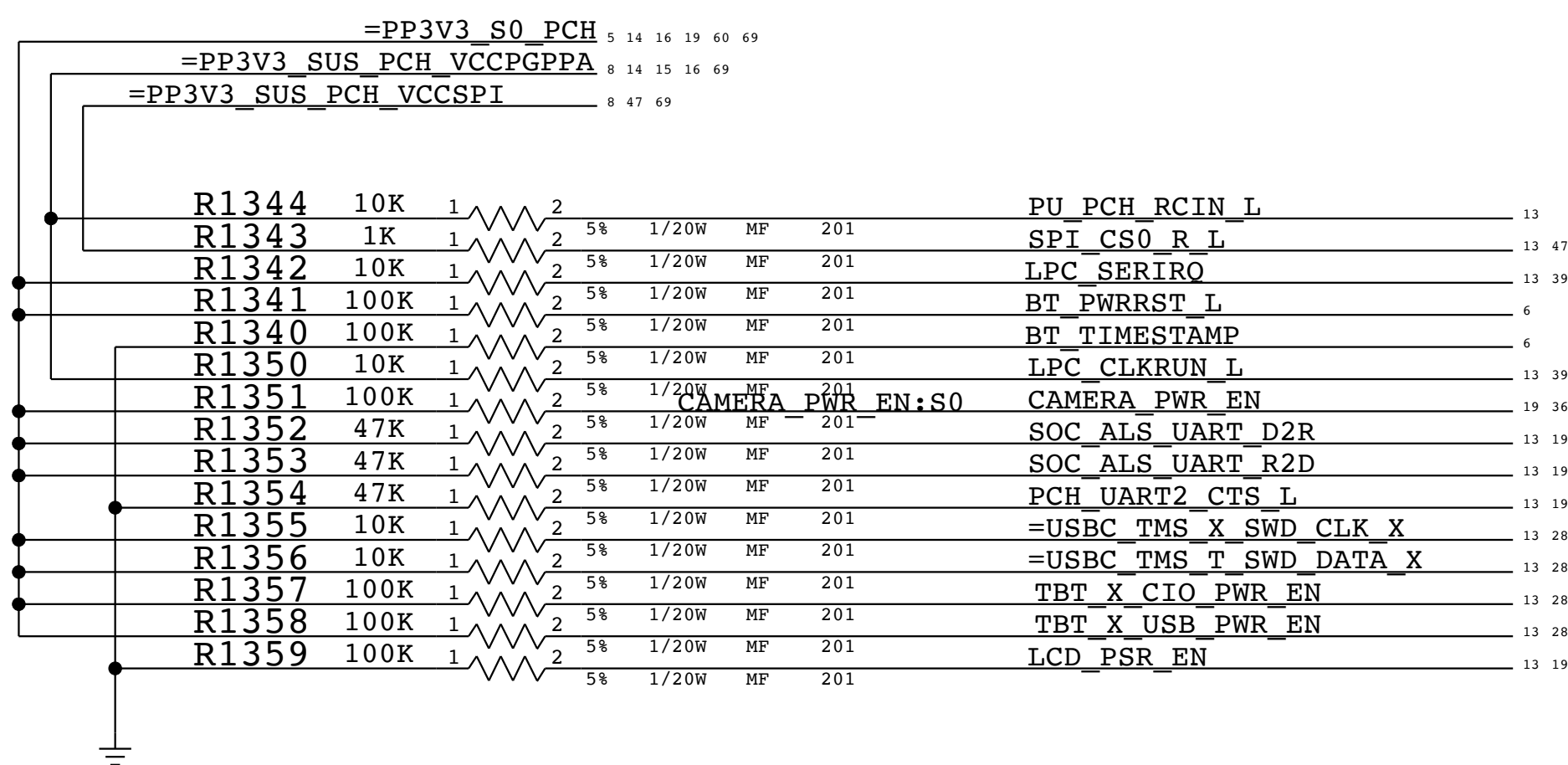
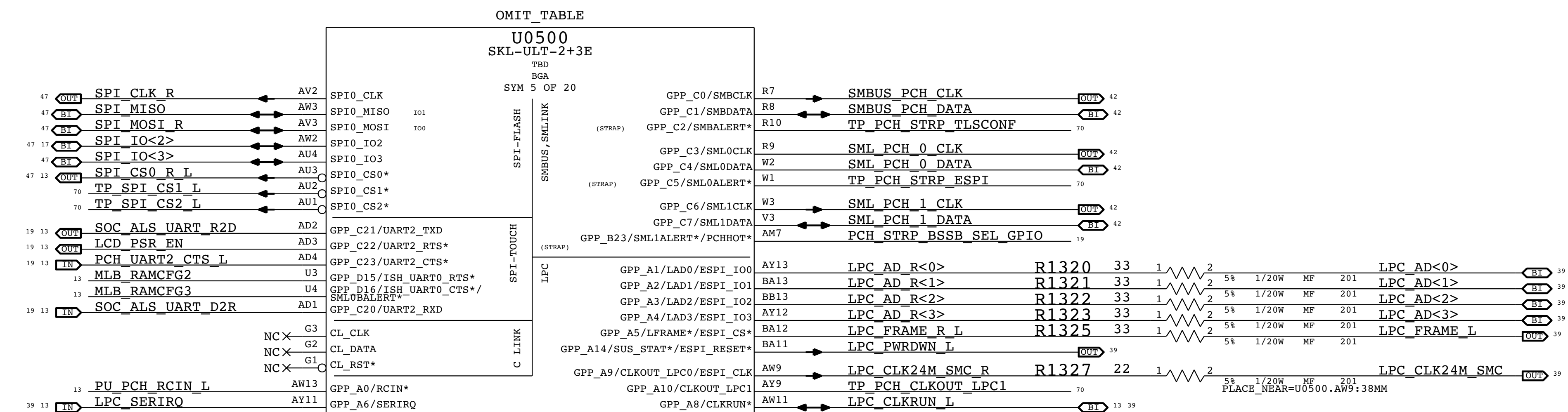
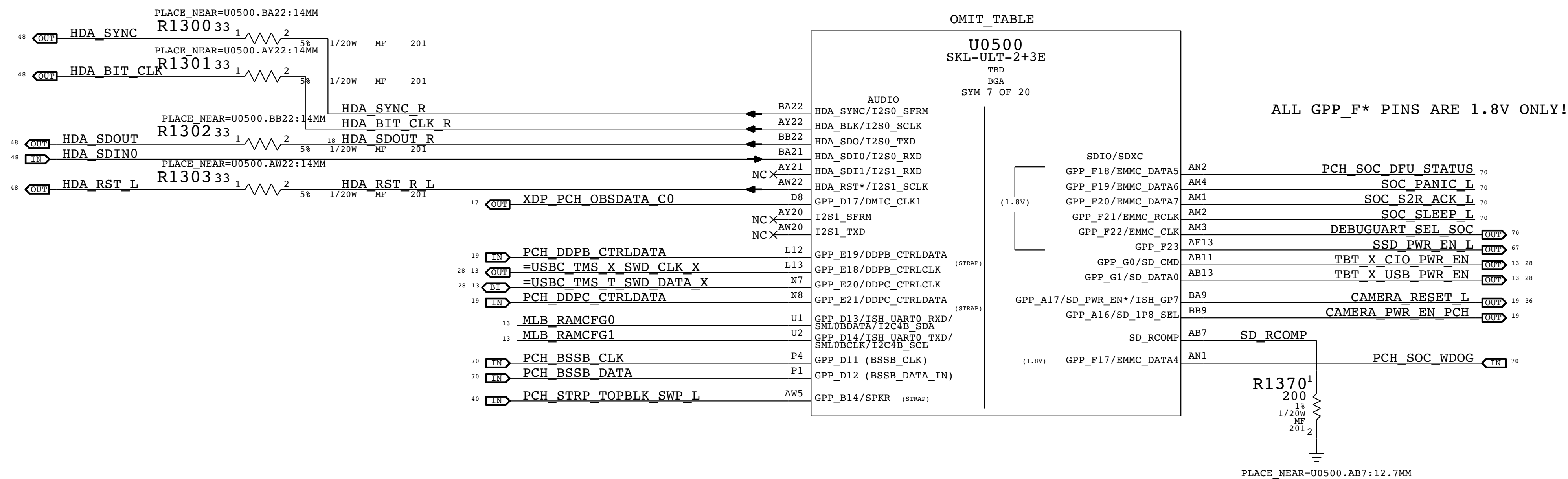
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		REVISION	1.0.0
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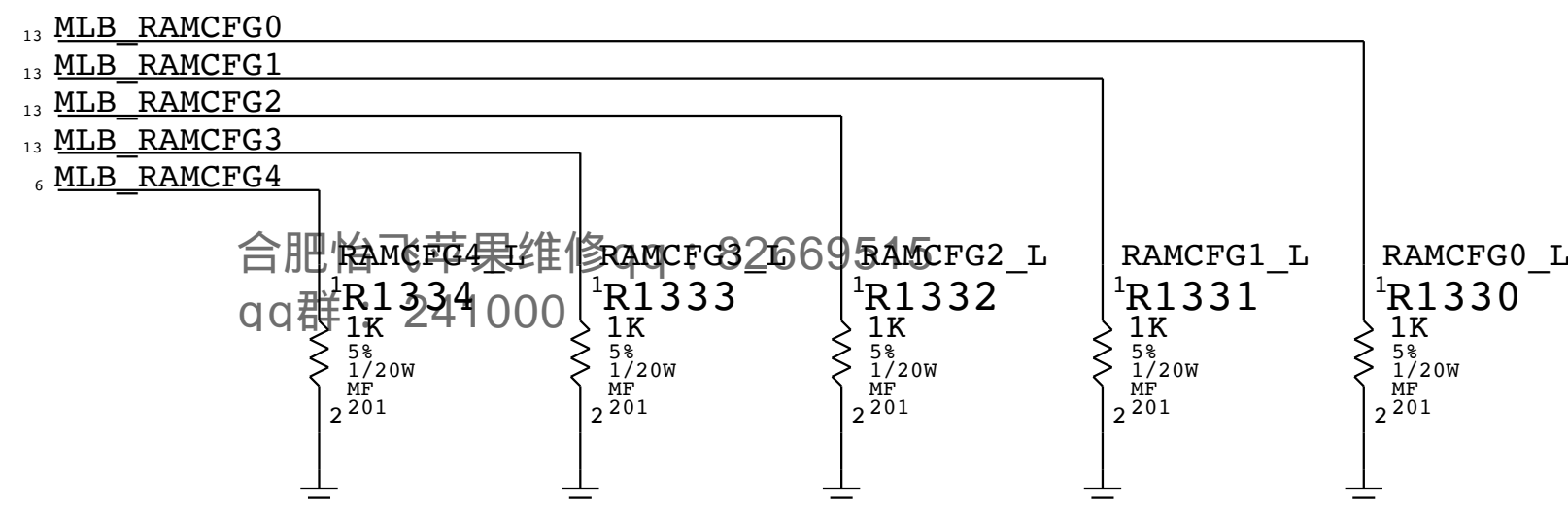
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	REVISION	1.0.0
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BOM_COST_GROUP=CPU & CHIPSET




MEMORY CONFIGURATION STRAPS.

PCH INTERNAL PULL-UPS ARE TO 3.3V.



BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG4_L, RAMCFG3_L, RAMCFG2_L, RAMCFG1_L, RAMCFG0_L

BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB CATZ		
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PAGE TITLE		
PCH Audio/LPC/SPI/SMBus		
 Apple Inc.	DRAWING NUMBER	SIZE
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	REVISION	
	1.0.0	
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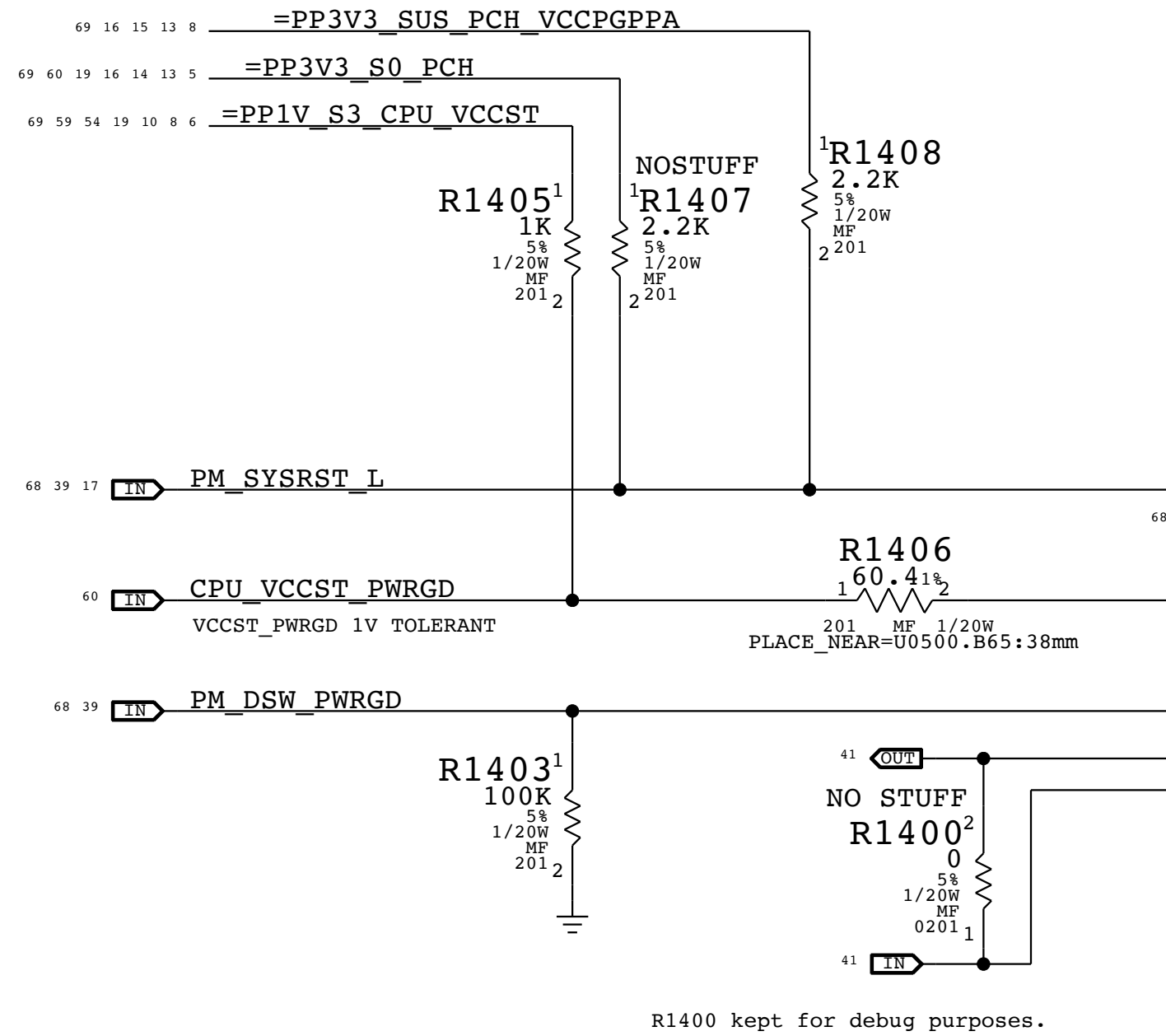
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PCH Reset Button

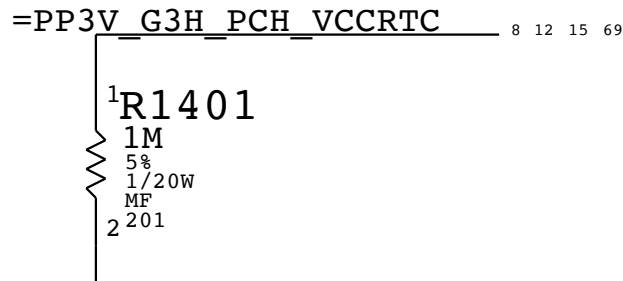


R1400 kept for debug purposes.

OMIT TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 11 OF 20
SYSTEM POWER MANAGEMENT

GPP_B12/SLP_S0*	AT11	PM_SLP_S0_L	OUT	14 39 60 72
GPD4/SLP_S3*	AP15	PM_SLP_S3_L	OUT	14 26 39 59 60 66 72
GPD5/SLP_S4*	BA16	PM_SLP_S4_L	OUT	14 39 60 68 72
GPD10/SLP_S5*	AY16	PM_SLP_S5_L	OUT	14 39 60 72
SLP_SUS*	AN15	PM_SLP_SUS_L	OUT	14 60 72
SLP_LAN*	AW15			
GPD9/SLP_WLAN*	BB17	TP_PCH_SLP_WLAN_L		70
GPD6/SLP_A*	AN16	TP_PCH_SLP_A_L		72
GPD3/PWRBTN*	BA15	PCH_PWRBTN_L	IN	14 41
GPD1/ACPRESENT*	AY15	SSD_SR_EN_L	OUT	14 67
GPD0/BATLOW*	AU13	PM_BATLOW_L	IN	14 28 39
GPP_A11/PME*	AU11	TP_PCH_PME_L		70
INTRUDER*	AP16	PCH_INTRUDER_L		
GPP_B11/EXT_PWR_GATE*	AM10	PCH_HSIO_PWR_EN	OUT	60
GPP_B2/VRALER*	AM11	BT_LOW_PWR_L	OUT	14 34 35



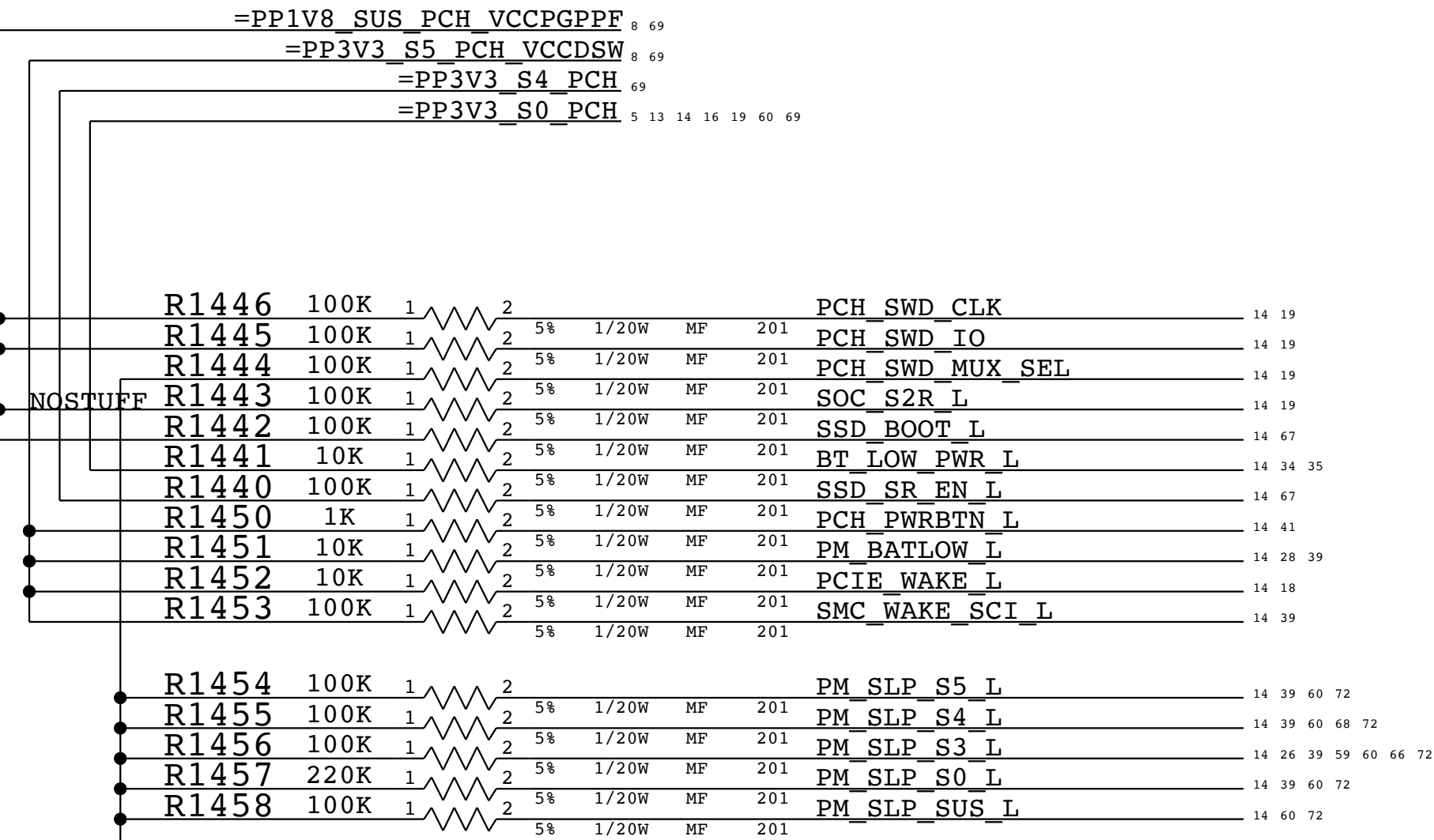
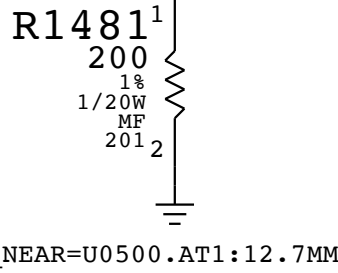
OMIT TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 9 OF 20

CSI2_DN0	C37	XNC	
CSI2_DP0	D37	XNC	
CSI2_DN1	C32	XNC	
CSI2_DP1	D32	XNC	
CSI2_DN2	C29	XNC	
CSI2_DP2	D29	XNC	
CSI2_DN3	B26	XNC	
CSI2_DP3	A26	XNC	
CSI2_DN4	E13	CSI2_COMP	
CSI2_DP4	M1	TP_PCH_GPP_D0	70
CSI2_DN5			
CSI2_DP5			
CSI2_DN6			
CSI2_DP6			
CSI2_DN7			
CSI2_DP7			
CSI2_DN8			
CSI2_DP8			
CSI2_DN9			
CSI2_DP9			
CSI2_DN10			
CSI2_DP10			
CSI2_DN11			
CSI2_DP11			

GPP_F7/I2C3_SCL	AH12	SSD_BOOT_L	OUT	14 67
GPP_F8/I2C4_SDA	AF11	TP_PCH_GPP_F8		70
GPP_F9/I2C4_SCL	AF12	TP_PCH_GPP_F9		70
GPP_F10/I2C5_SDA/ISH_I2C2_SDA	AD11	TP_PCH_GPP_F10		70
GPP_F11/I2C5_SCL/ISH_I2C2_SCL	AD12	PCH_BT_ROM_BOOT		70
GPP_F12/EMMC_CMD	AP4	PCH_SWD_CLK	OUT	14 19
GPP_F13/EMMC_DATA0	AP2	PCH_SWD_IO	BI	14 19
GPP_F14/EMMC_DATA1	AP1	PCH_SWD_MUX_SEL	OUT	14 19
GPP_F15/EMMC_DATA2	AP3	SOC_S2R_L		14 19
GPP_F16/EMMC_DATA3	AN3	PCH_SOC_FORCE_DFU	OUT	70
GPP_F6/I2C3_SDA	AH11	UPC_I2C_INT_L	IN	70

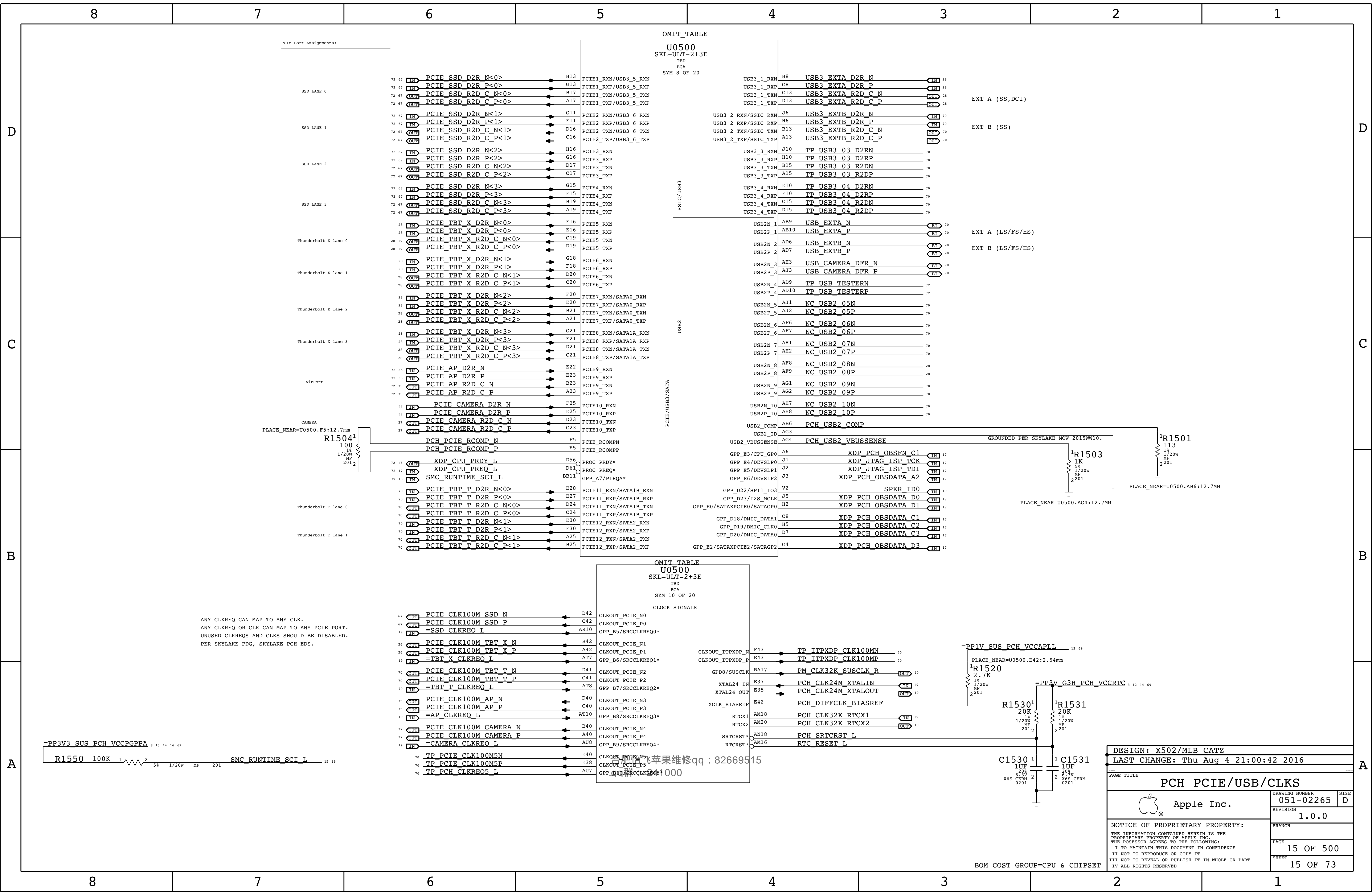
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NOTE: PM_SLP_S0_L HAS INTERNAL PULL-UP BEFORE RSMRST_L IS RELEASED.
THIS CAUSES A VOLTAGE DIVIDER WITH THE PULL-DOWN HERE.
THE SIGNAL IS DRIVEN HI AFTER RSMRST_L IS RELEASED.

BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB CATZ		
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PCH Power Management		
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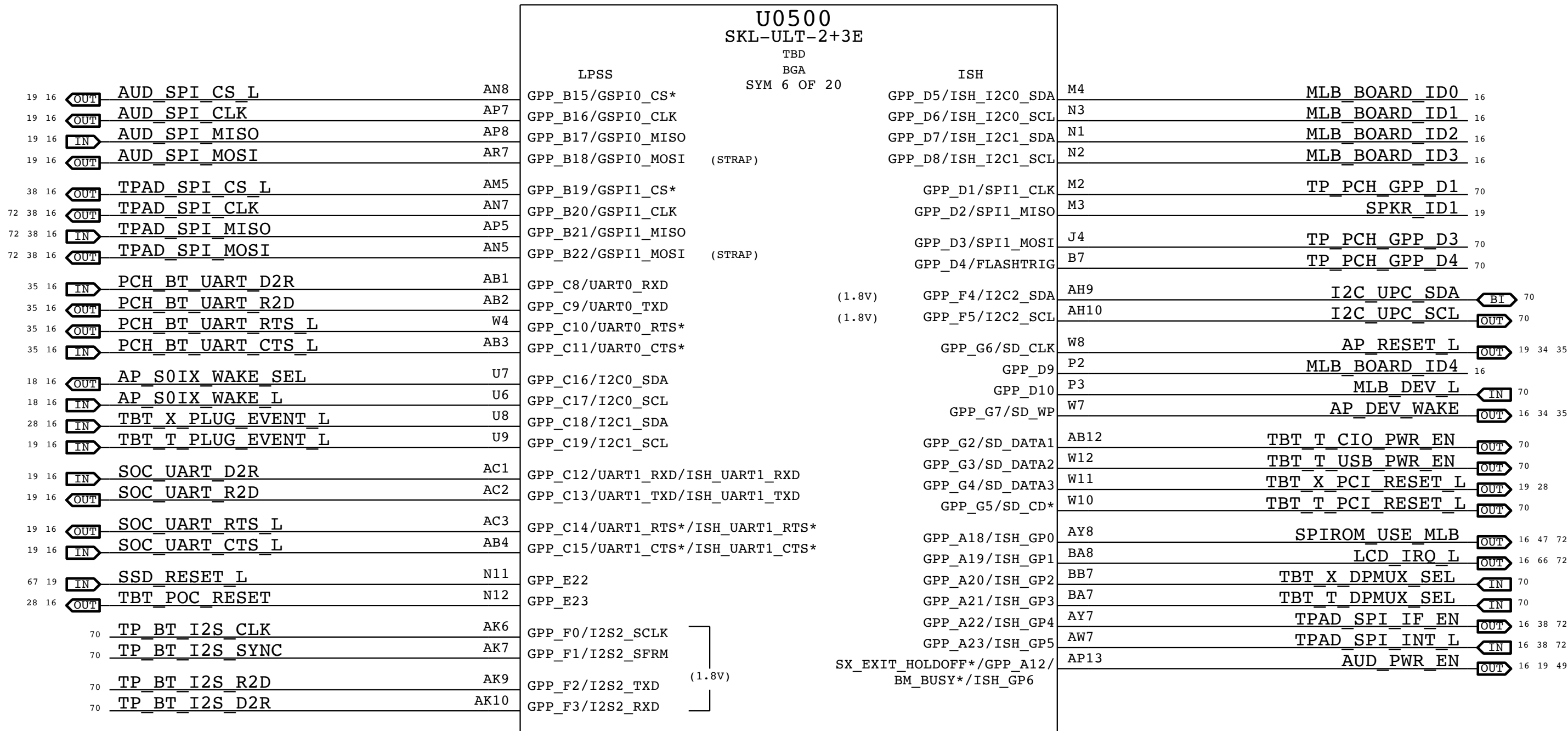
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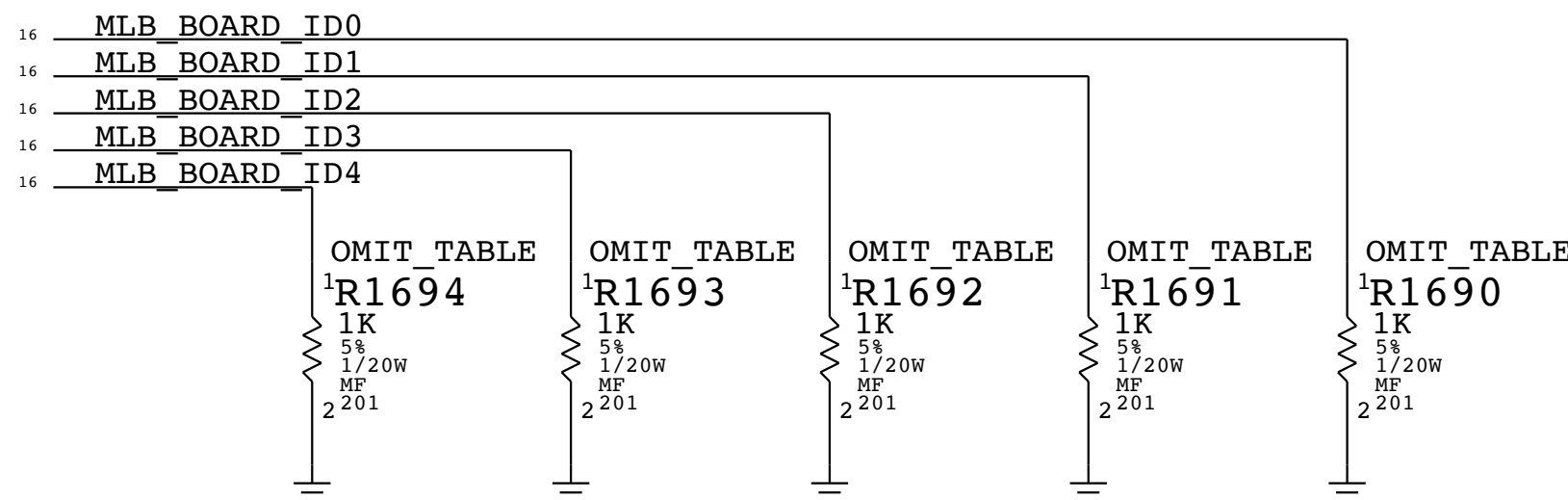
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ALL GPP_F* PINS ARE 1.8V ONLY!
OMIT TABLE

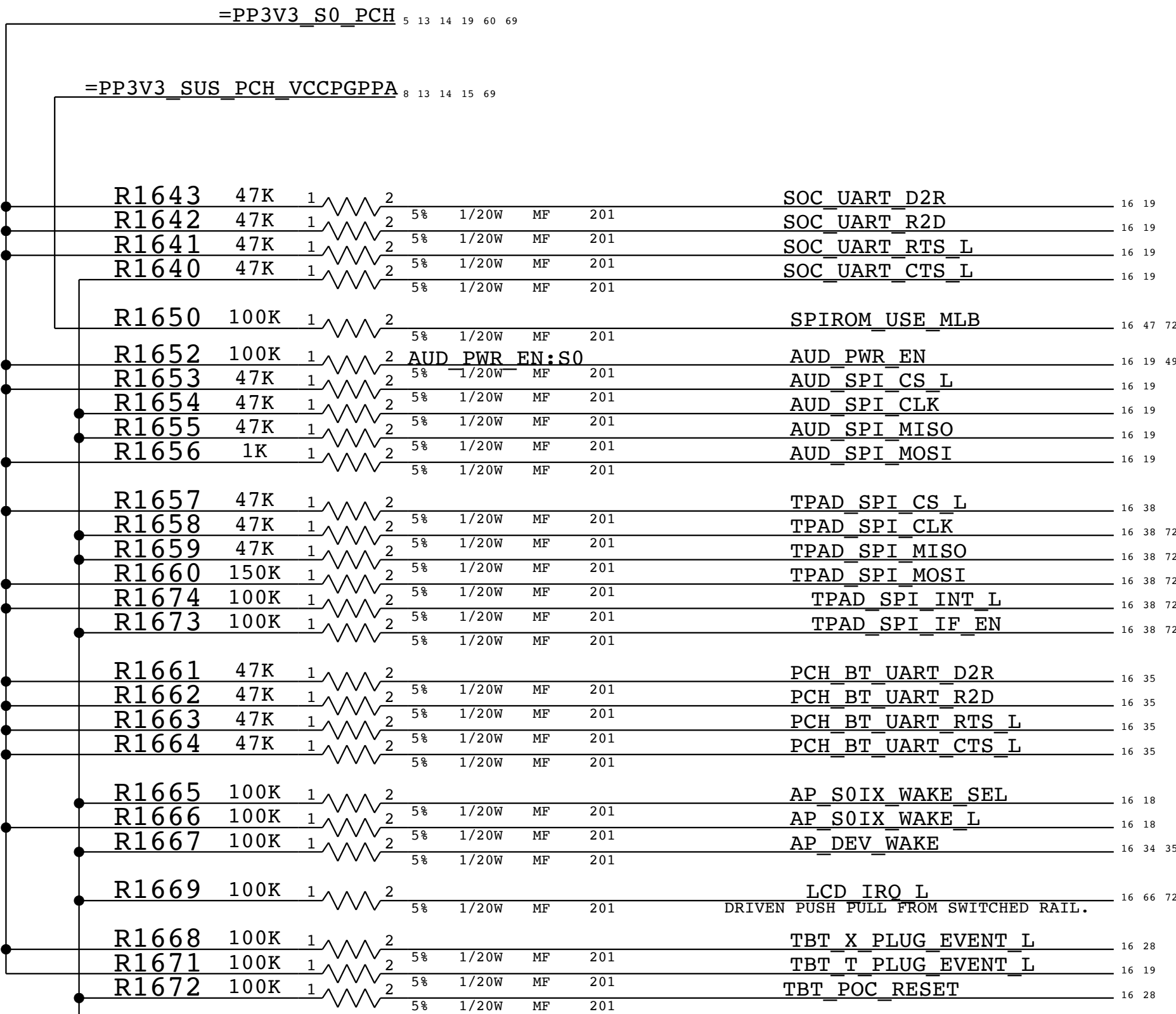


MLB ID STRAPS.


PCH INTERNAL PULL-UPS ARE TO VCCGPPD = 3.3V.

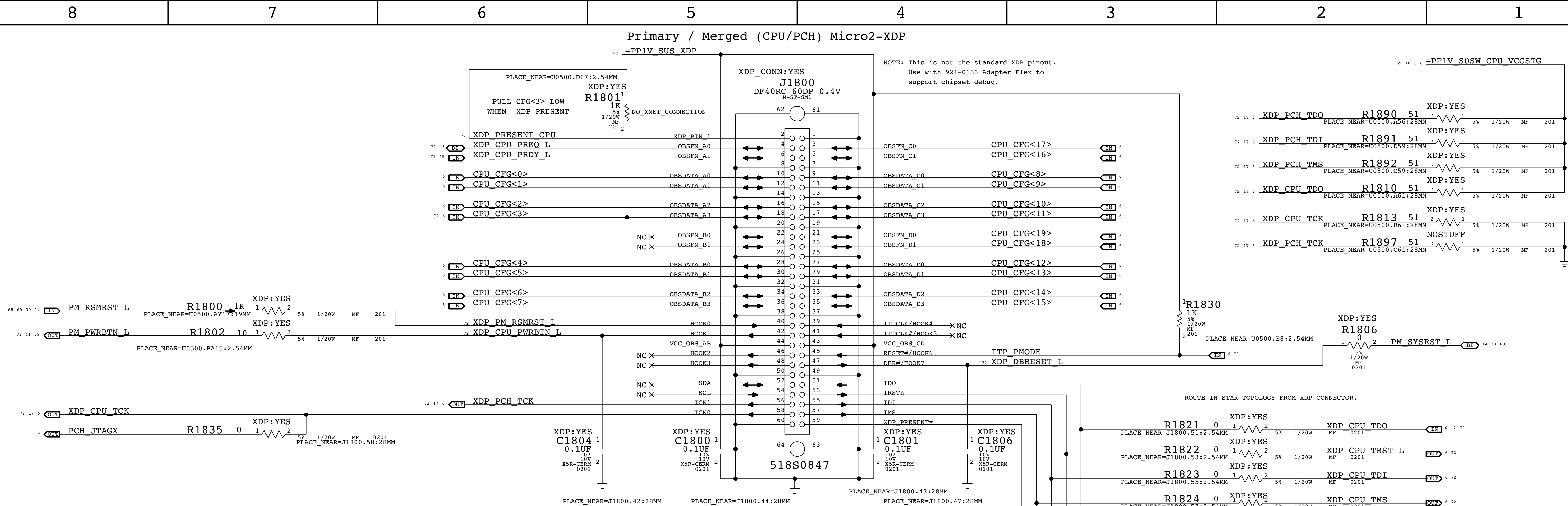


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117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1691	BOARD_ID:2	<11101>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1691,R1690	BOARD_ID:3	<11100>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692	BOARD_ID:4	<11011>
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117S0006	3	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692,R1691,R1690	BOARD_ID:7	<11000>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693	BOARD_ID:8	<10111>
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BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB CATZ		
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PAGE TITLE		
PCH SPI/UART/GPIO		
 Apple Inc.	DRAWING NUMBER	051-02265
	REVISION	1.0.0
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PCH XDP Signals

These signals do not connect to the Primary (Merged) XDP connector in this architecture. The PDG puts them on a secondary XDP connector that is only needed in some PCH debugging situation. They are listed here to show their secondary XDP functions and to provide test points for signals that are not used elsewhere.

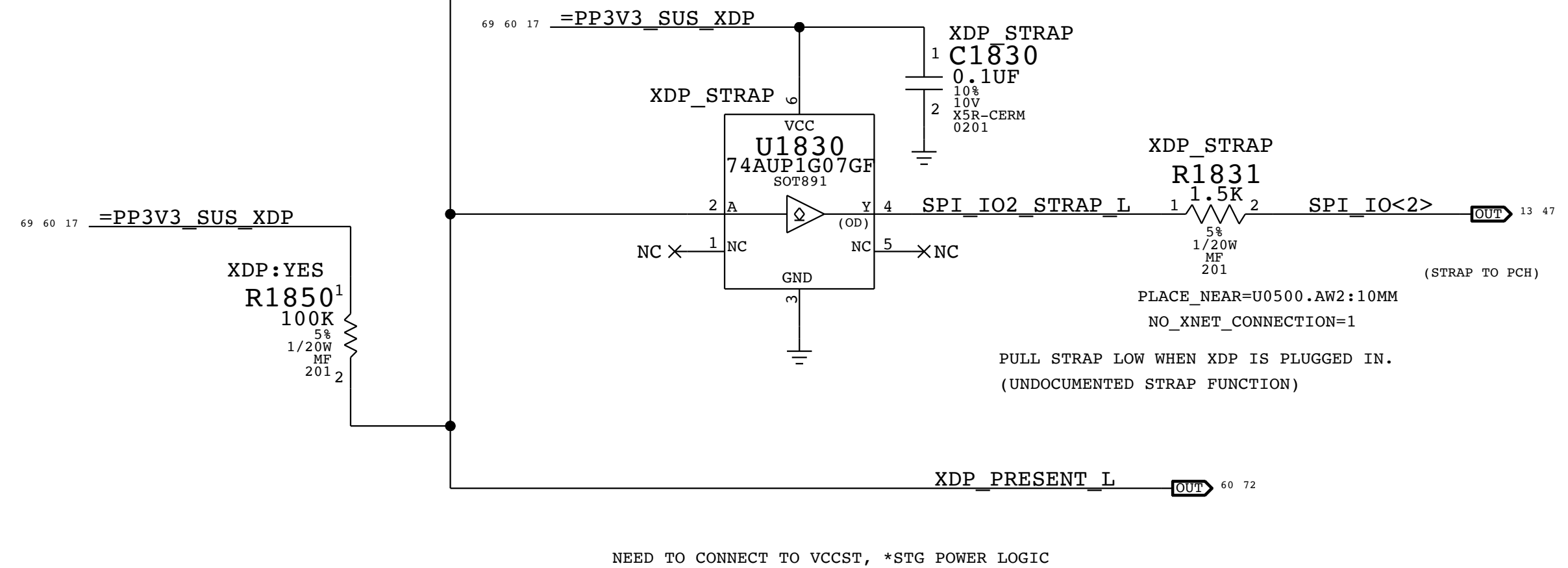
PCH/XDP Signals					Non-XDP Signals				
15	TP	XDP_JTAG_ISP_TCK	MAKE_BASE=TRUE	==		JTAG_ISP_TCK		OUT	28
15	TP	XDP_JTAG_ISP_TDI	MAKE_BASE=TRUE	==		JTAG_ISP_TDI		OUT	28
15	BT	XDP_PCH_OBSDATA_A2			TP-P6	TP1870			
15	BT	XDP_PCH_OBSDATA_A3			TP-P6	TP1871			
15	BT	XDP_PCH_OBSDATA_B0			TP-P6	TP1872			
15	BT	XDP_PCH_OBSDATA_C0			TP-P6	TP1873			
15	BT	XDP_PCH_OBSDATA_C1			TP-P6	TP1874			
15	BT	XDP_PCH_OBSDATA_C2			TP-P6	TP1875			
15	BT	XDP_PCH_OBSDATA_C3			TP-P6	TP1876			
15	BT	XDP_PCH_OBSDATA_D0			TP-P6	TP1877			
15	BT	XDP_PCH_OBSDATA_D1			TP-P6	TP1878			
15	BT	XDP_PCH_OBSDATA_D2			TP-P6	TP1879			
15	BT	XDP_PCH_OBSDATA_D3			TP-P6	TP1880			
15	BT	XDP_PCH_OBSFN_C1			TP-P6	TP1881			
5	OUT	XDP_USB_EXT_A_OC_L	MAKE_BASE=TRUE	==		USB_EXT_A_OC_L		IN	28
5	OUT	XDP_USB_EXTB_OC_L	MAKE_BASE=TRUE	==		USB_EXTB_OC_L		IN	28
5	OUT	XDP_USB_EXTC_OC_L	MAKE_BASE=TRUE	==		USB_EXTC_OC_L		IN	28
5	OUT	XDP_USB_EXTD_OC_L	MAKE_BASE=TRUE	==		USB_EXTD_OC_L		IN	28

Unused GPIOs have TPs.


USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.

JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.

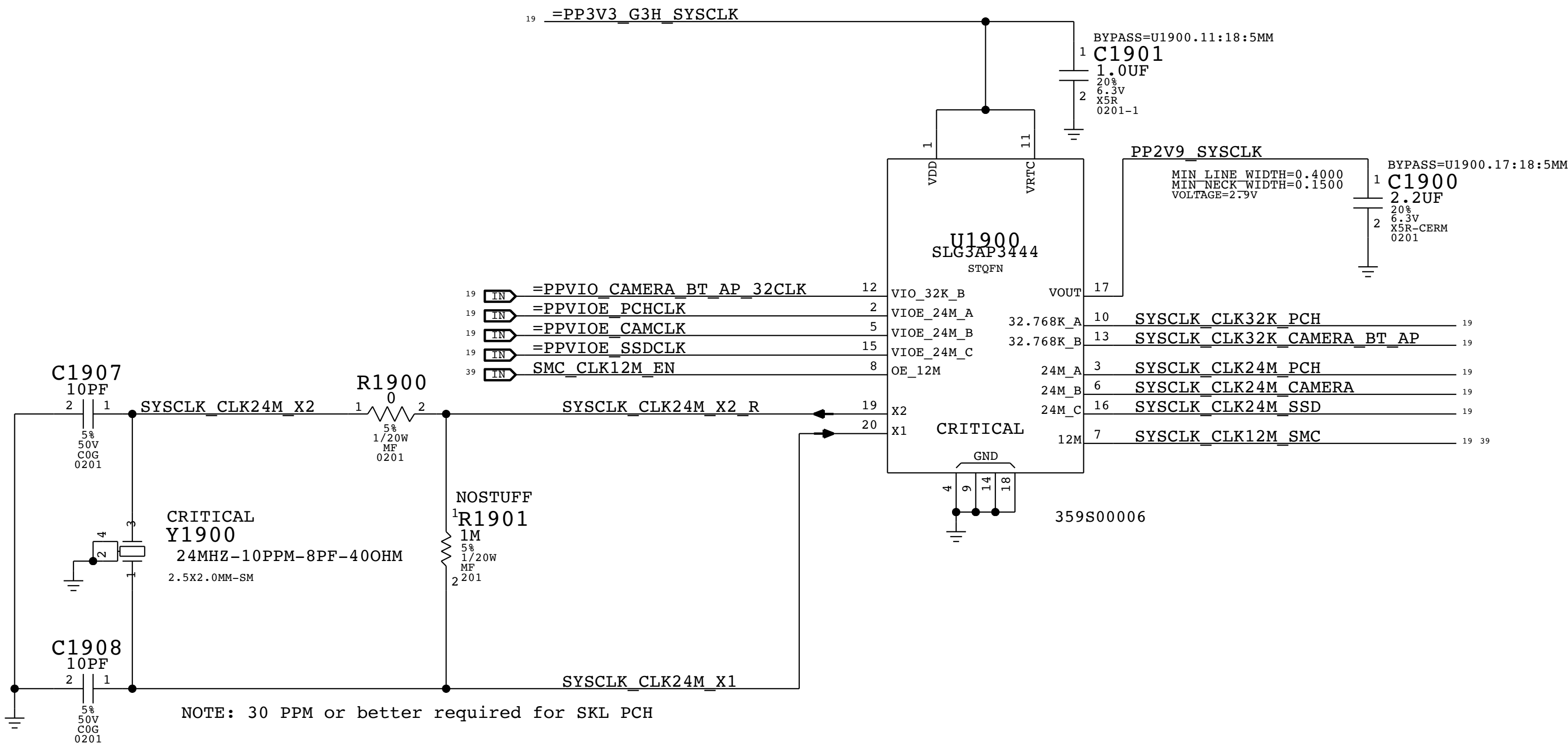
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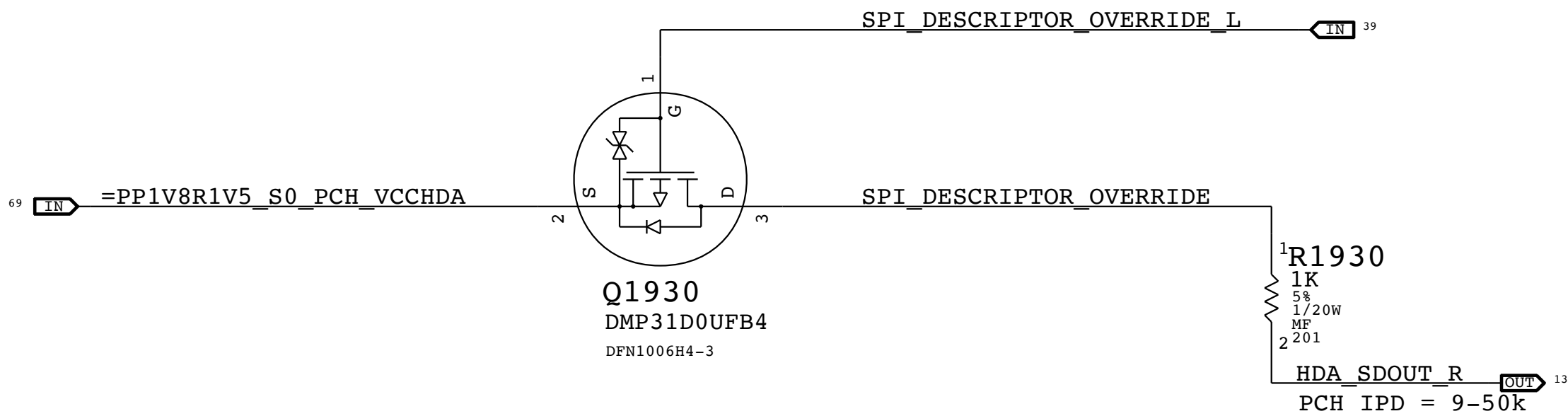
NEED TO CONNECT TO VCCST, *STG POWER LOGIC

DESIGN: X502/MLB CATZ		
LAST CHANGE: Thu Aug 4 21:00:42 2016		
PAGE TITLE		
CPU/PCH Merged XDP		
 Apple Inc.	DRAWING NUMBER	SIZE
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	BRANCH	
	PAGE	18 OF 500
	SHEET	17 OF 73

System 32kHz / 12MHz / 24MHz Clock Generator

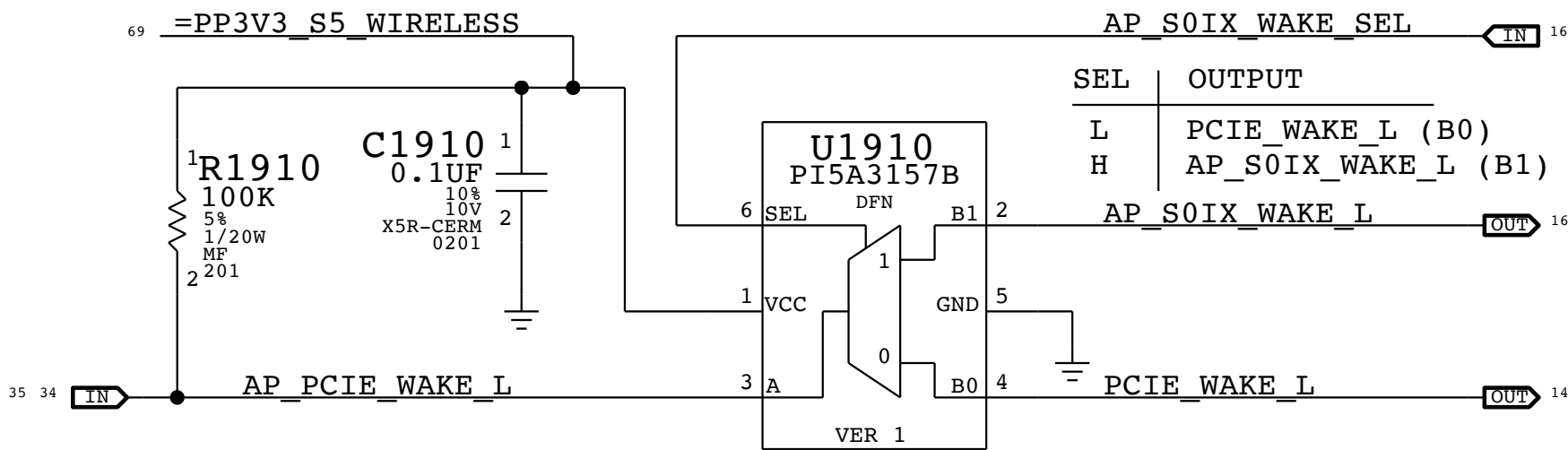


PCH ME Disable Strap



PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. ***** Circuit does not support HDA voltage >3.3V.

PCIe Wake Muxing



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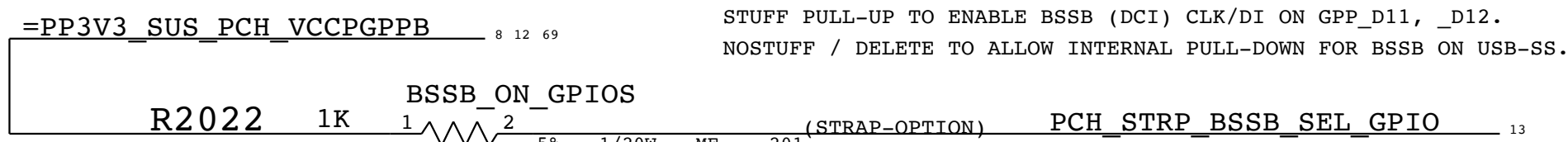
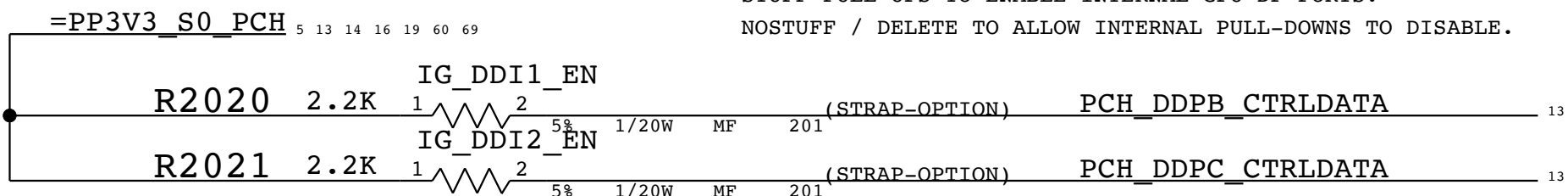
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		PAGE		19 OF 500	
		SHEET		18 OF 73	

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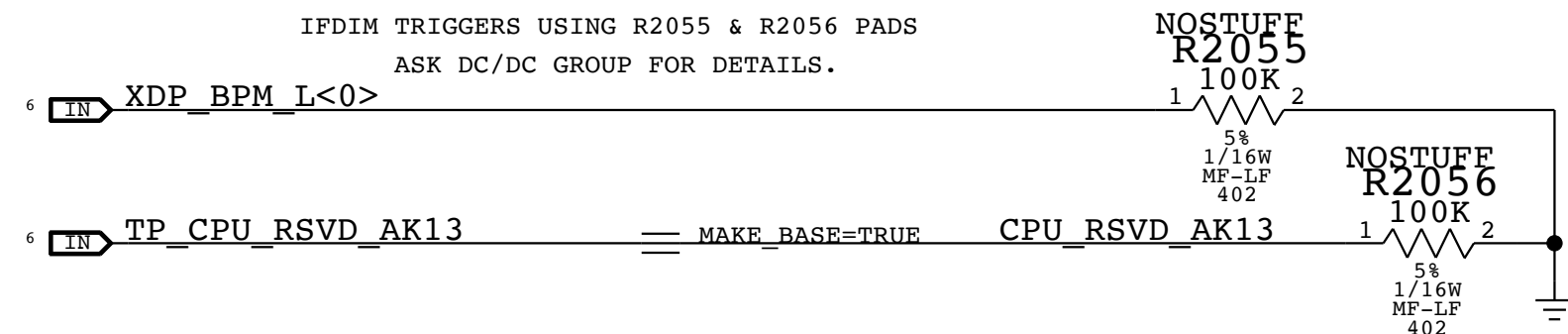
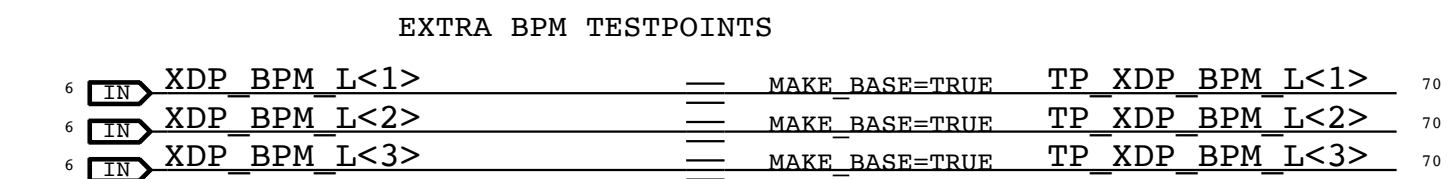
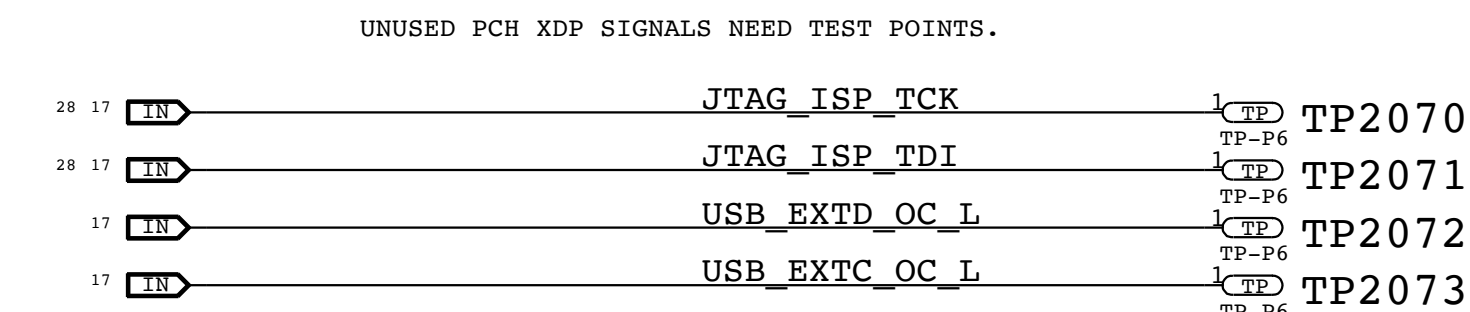
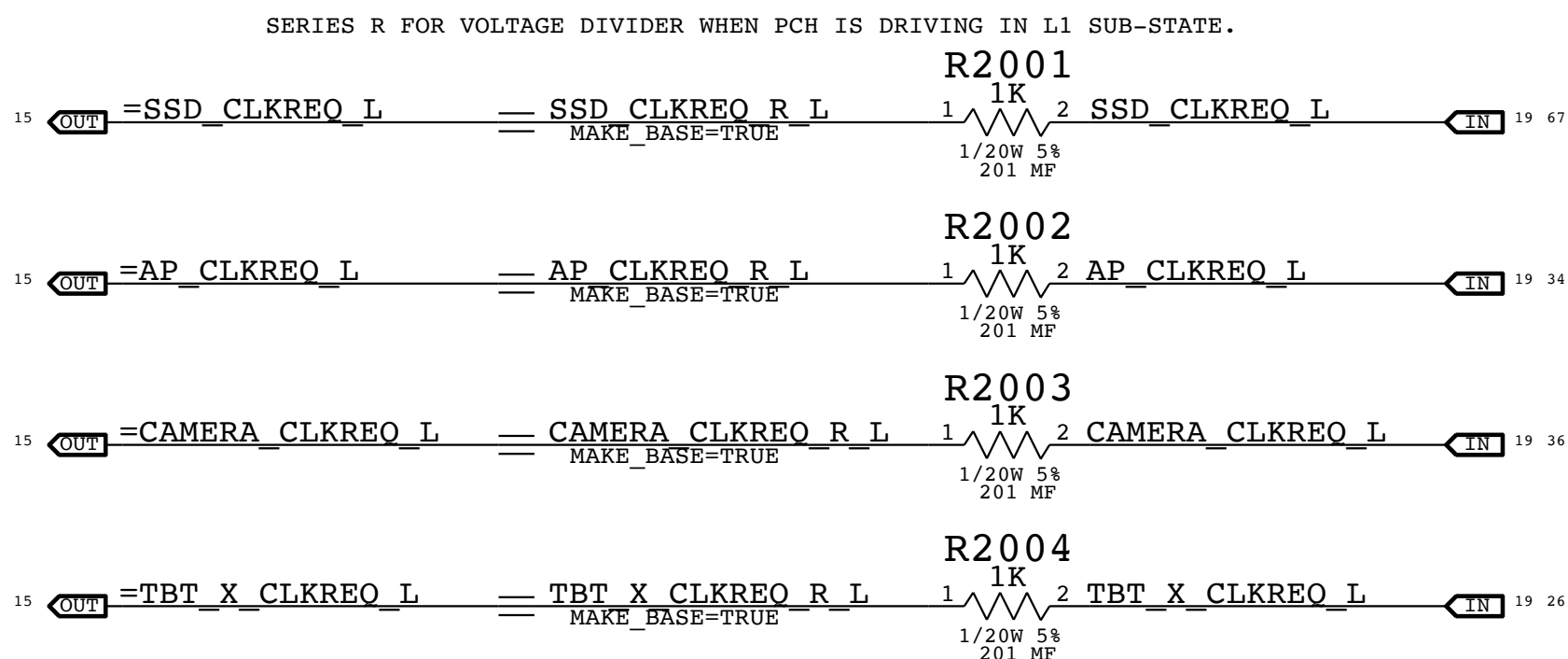
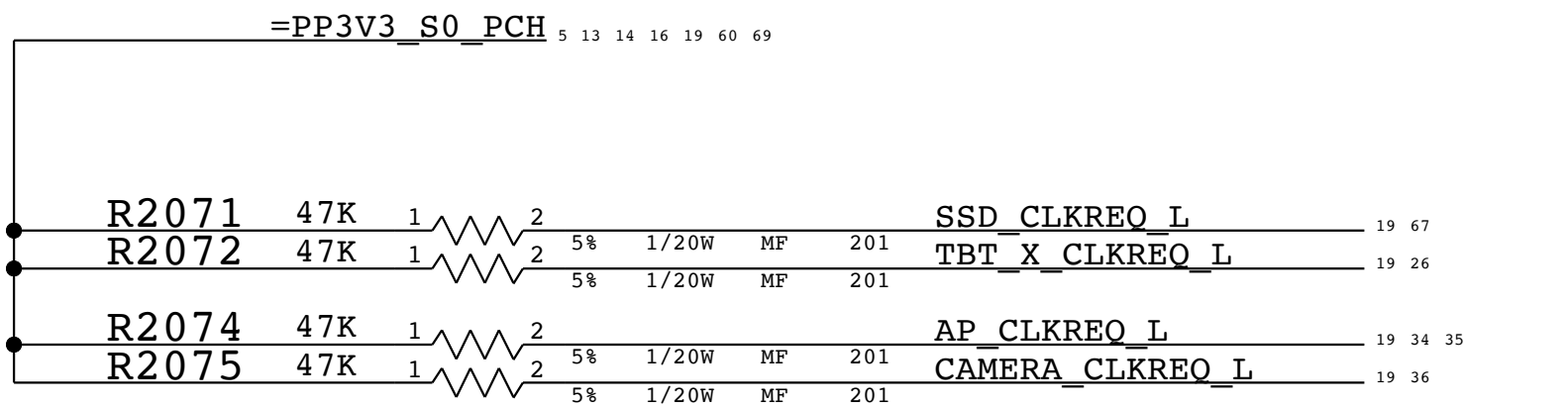
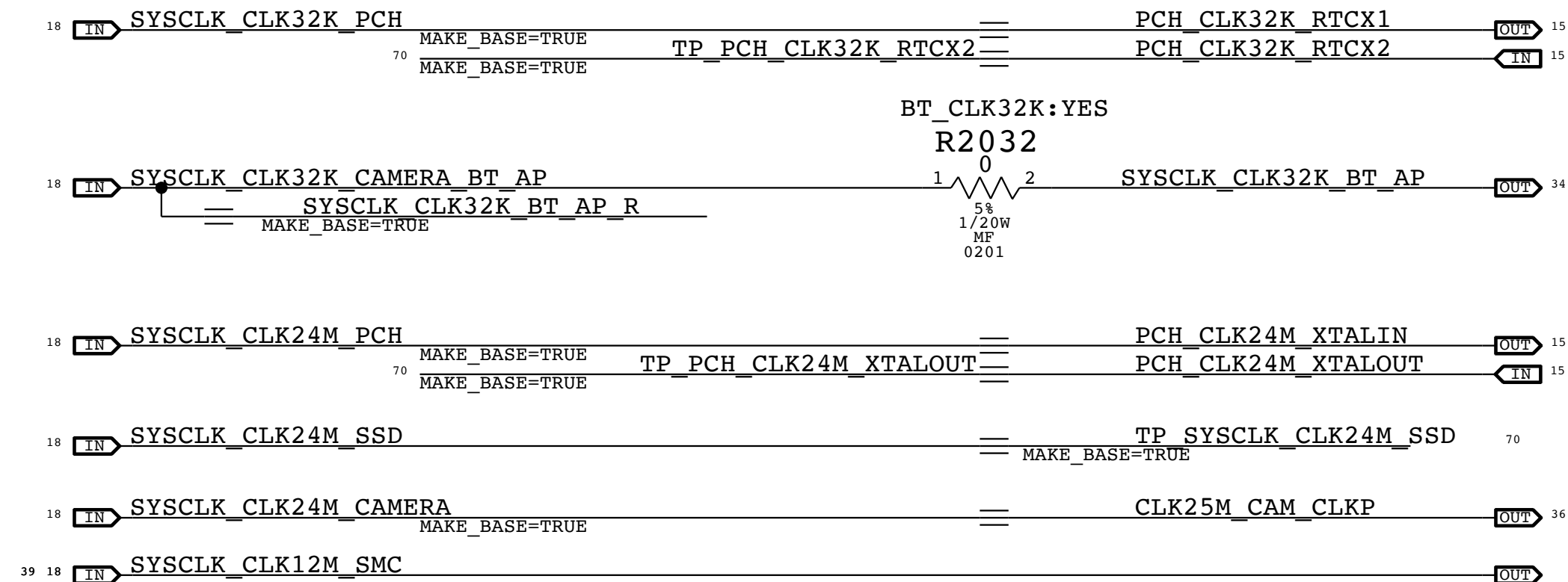
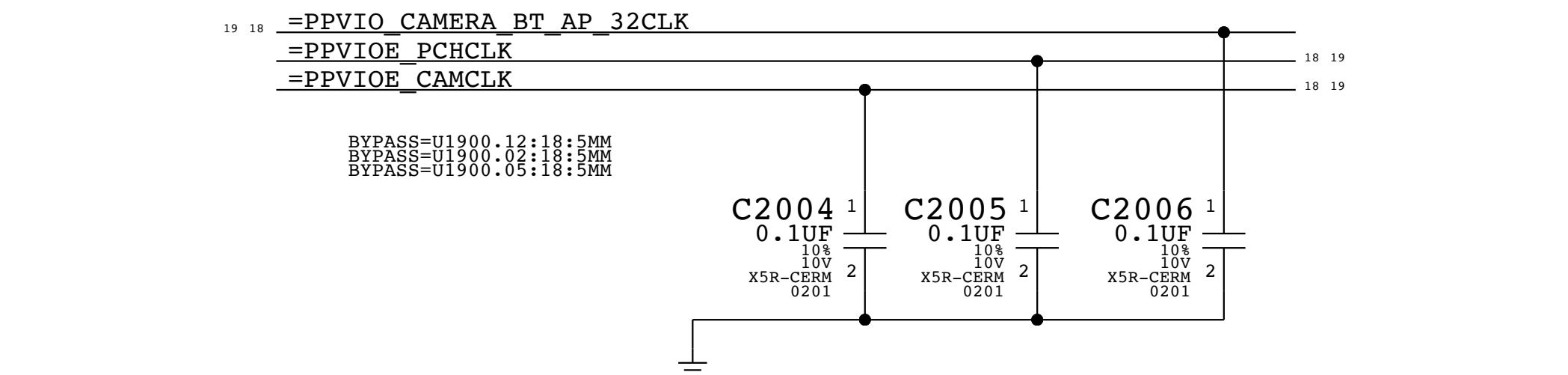
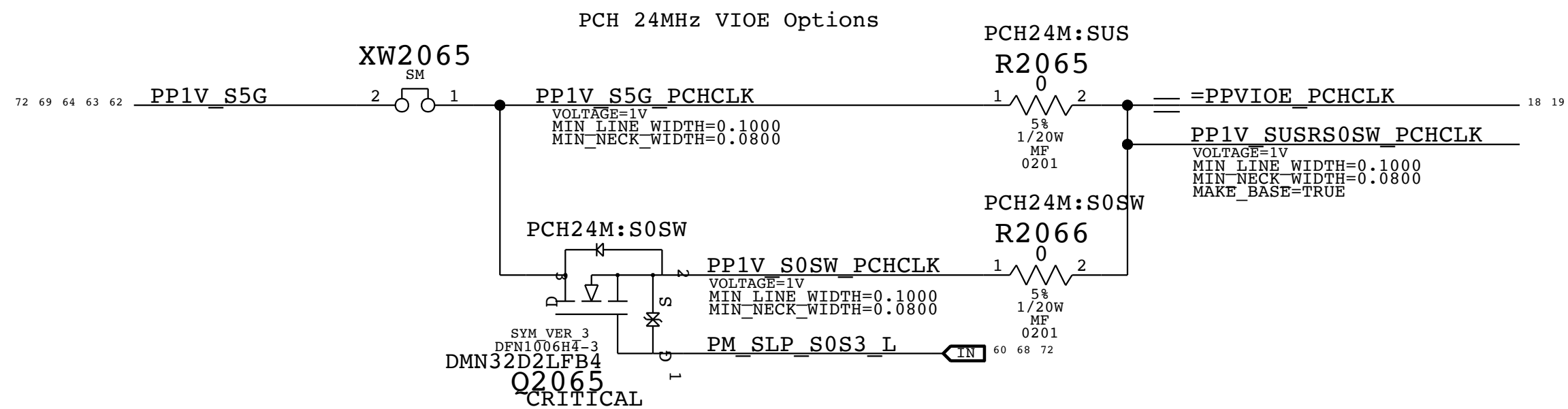
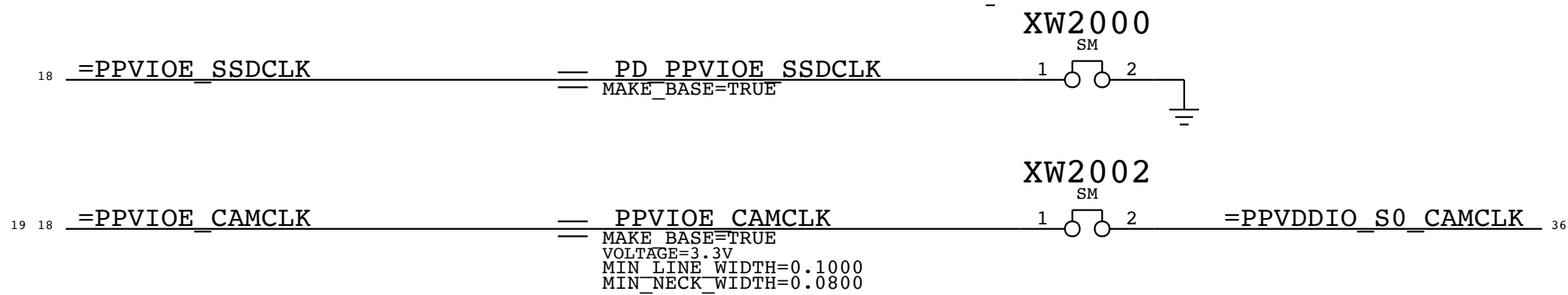
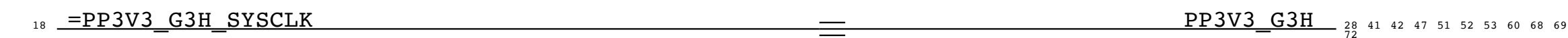
OPTION STRAPS

PROJECT DEPENDANT

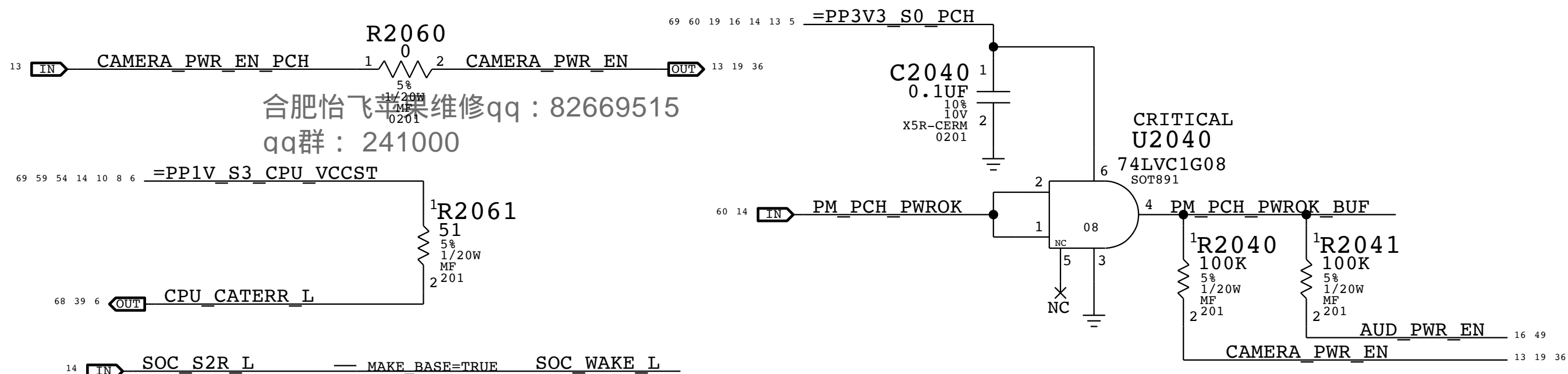
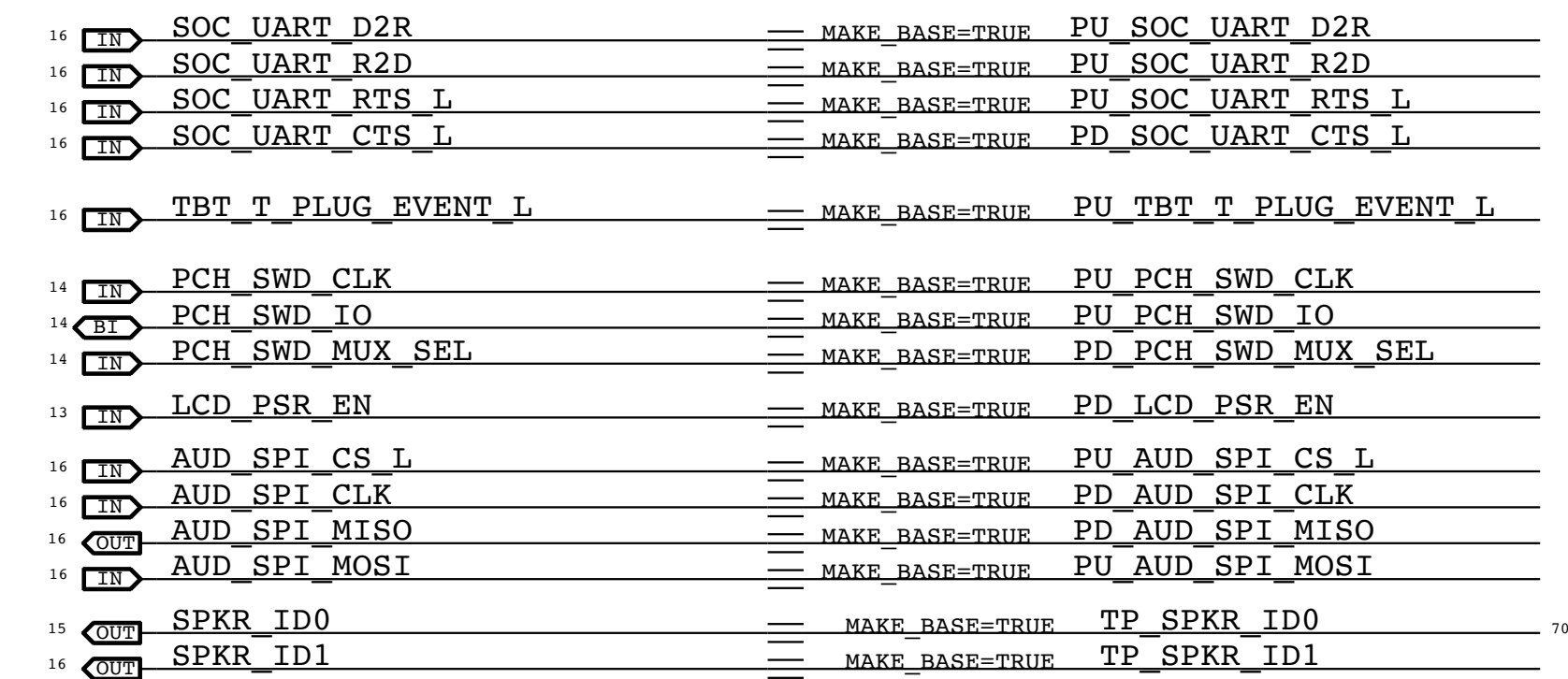
STUFF PULL-UPS TO ENABLE INTERNAL GPU DP PORTS.
NOSTUFF / DELETE TO ALLOW INTERNAL PULL-DOWNS TO DISABLE.



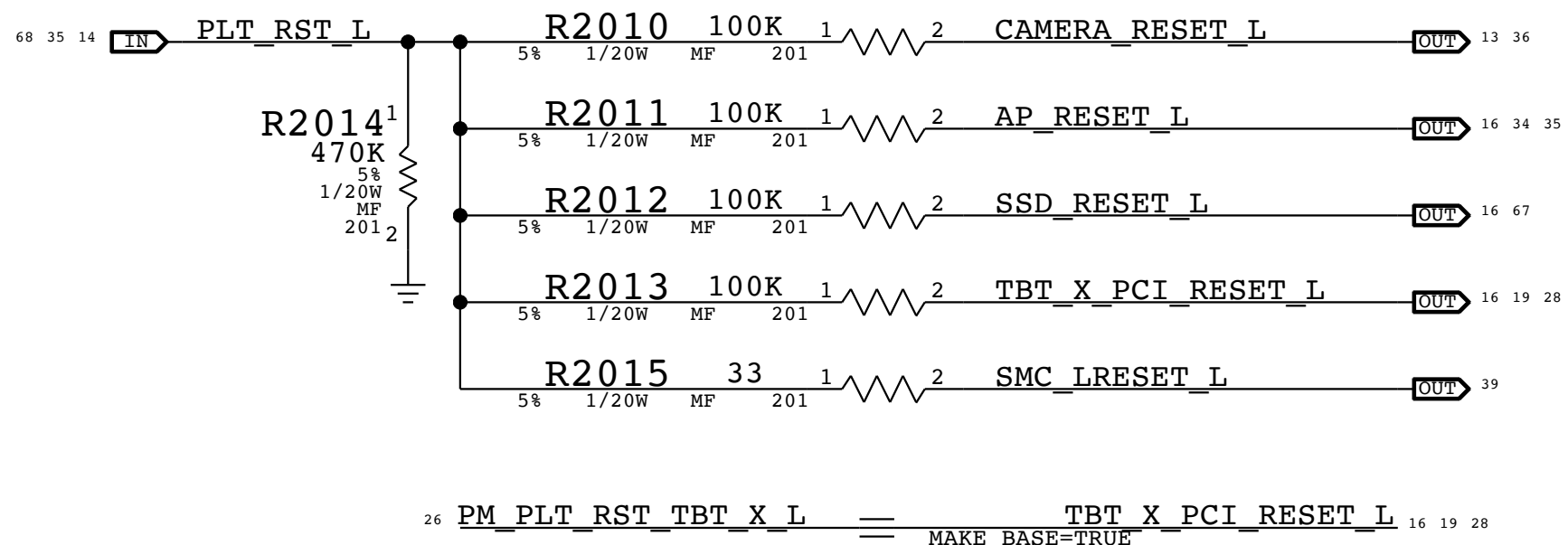
GREENCLK CLOCK CONNECTIONS.



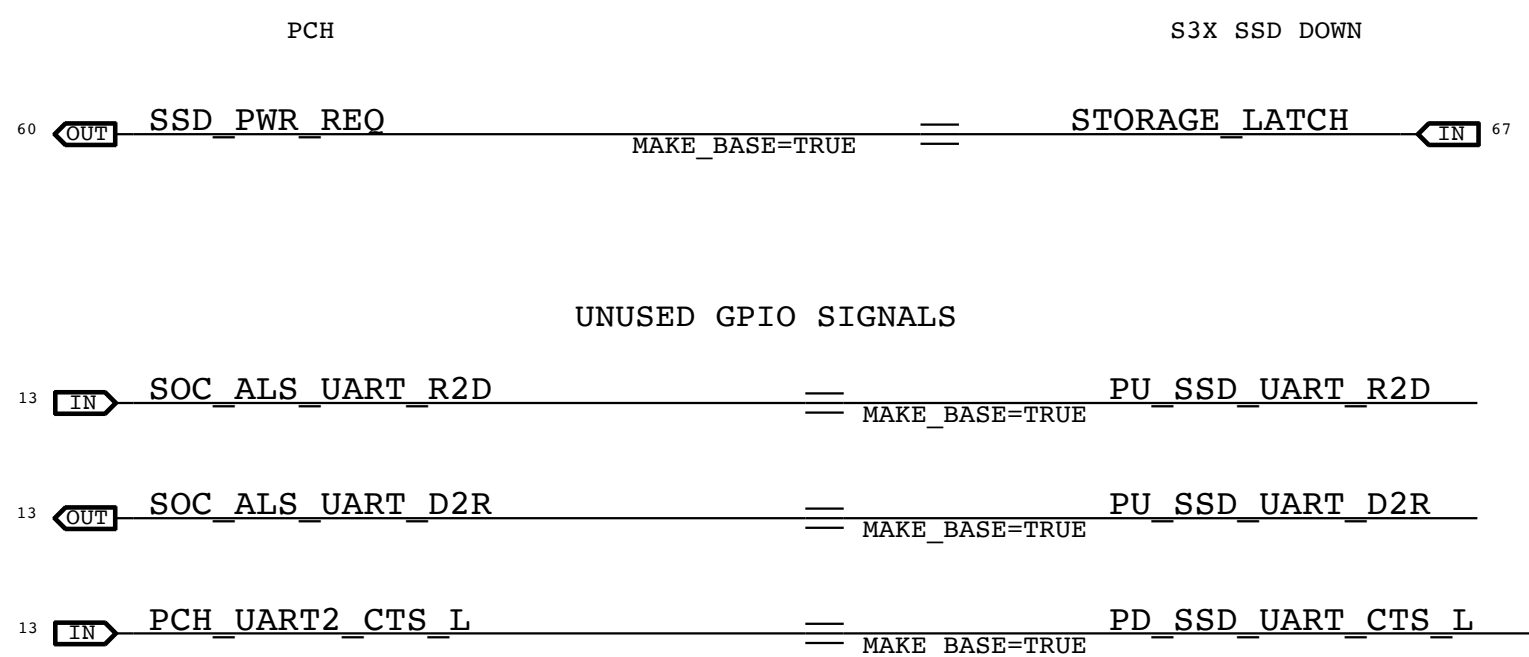
UNUSED GPIO SIGNALS



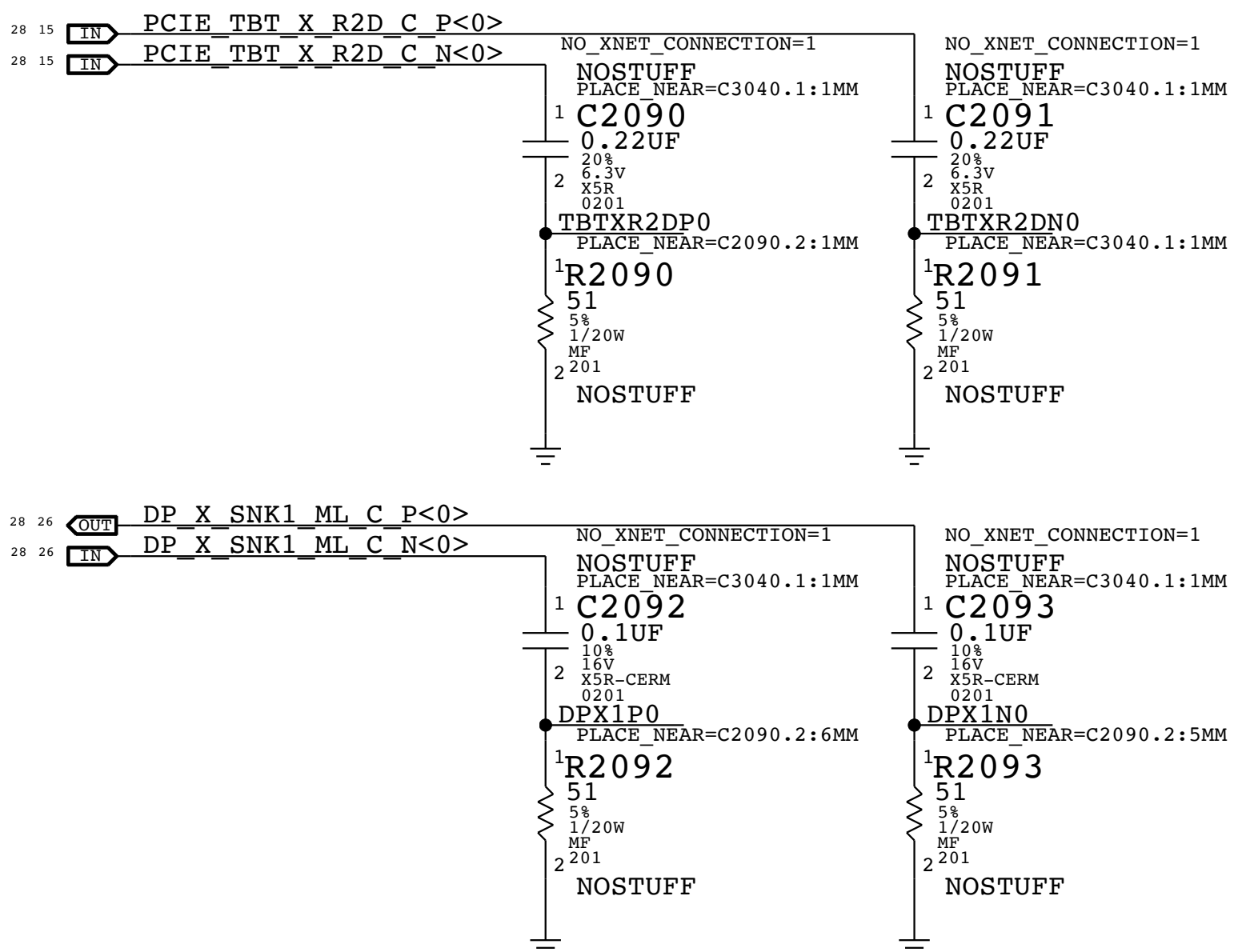
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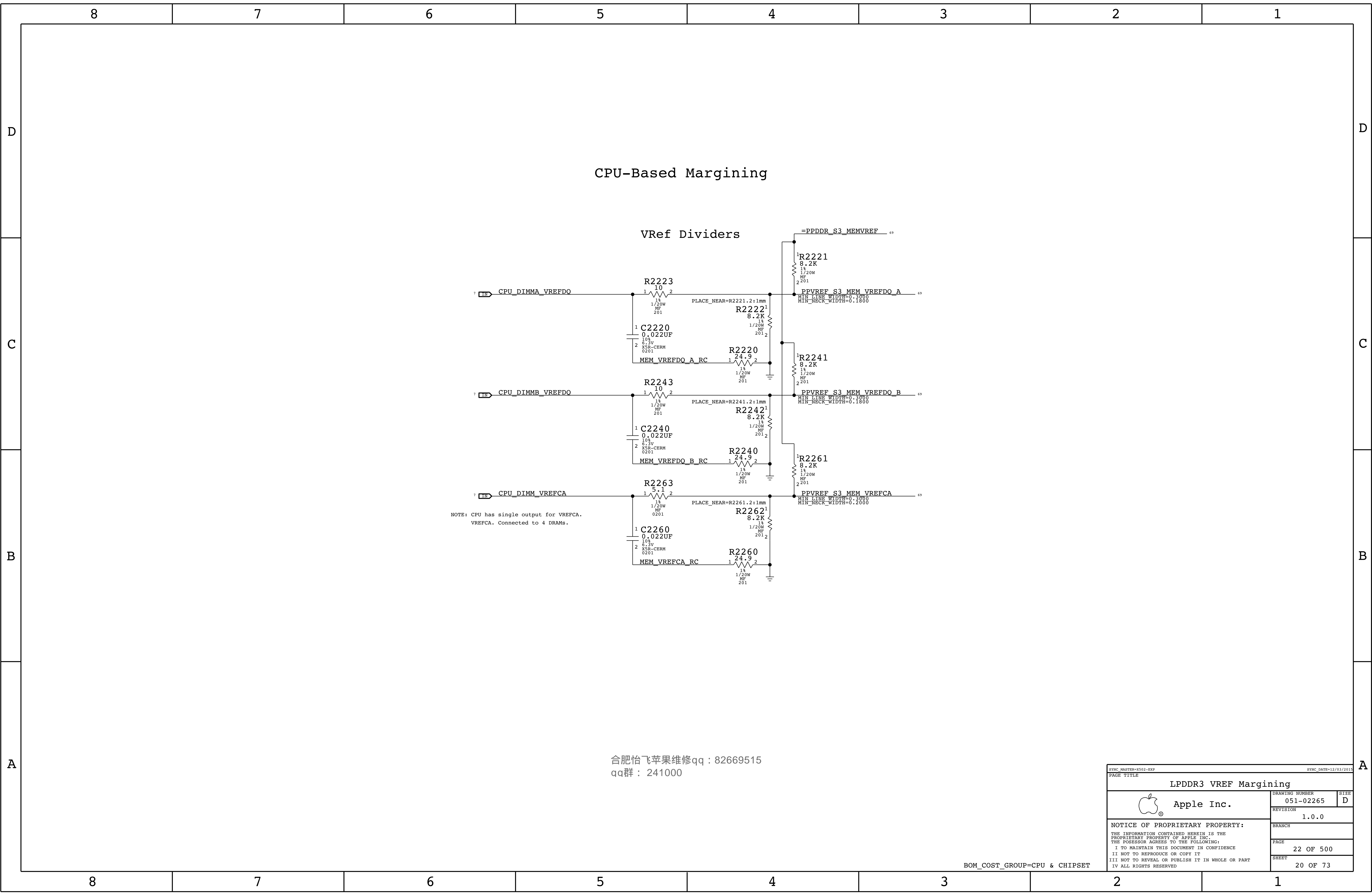
S3X SSD CONTROL



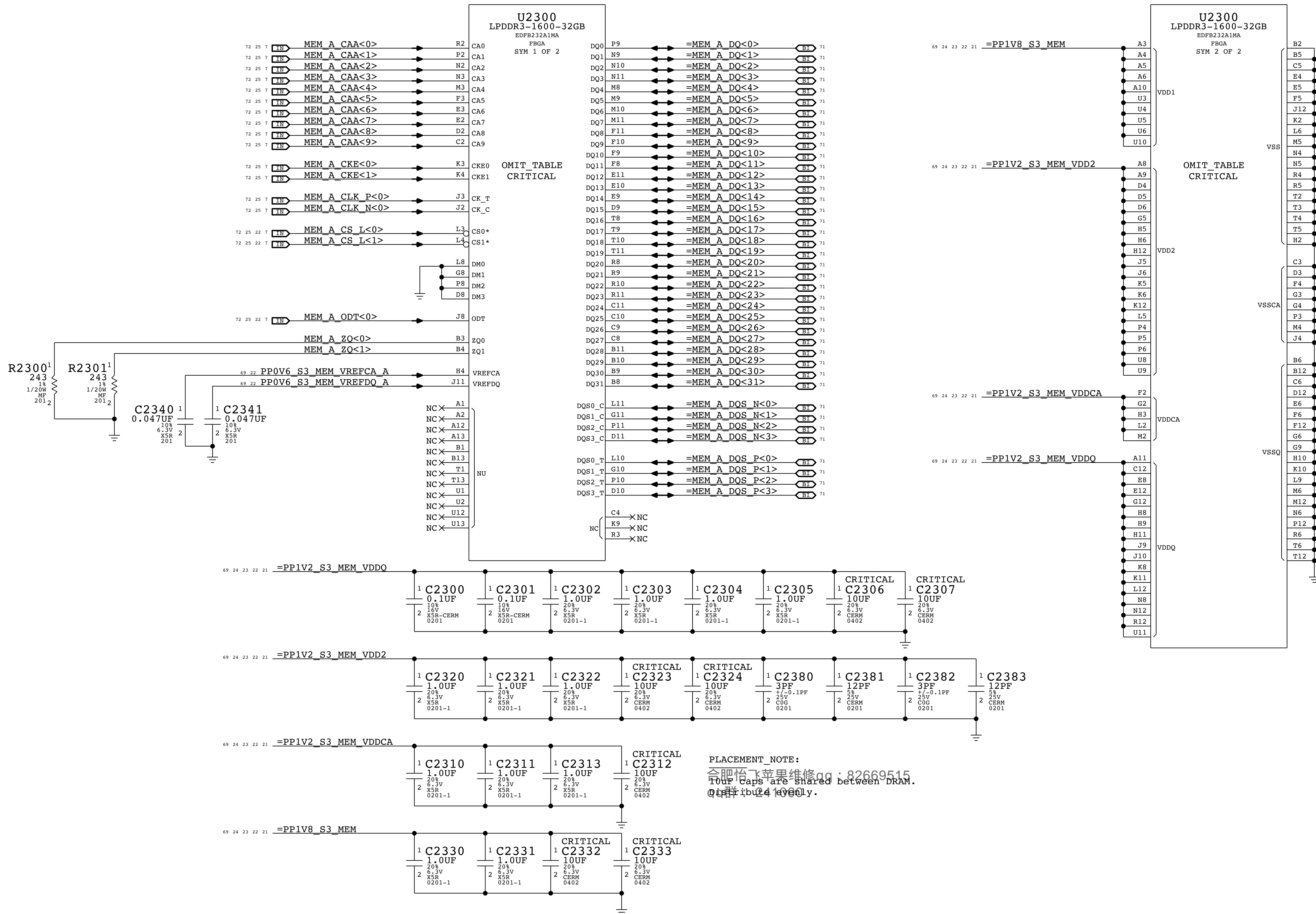
PROBE POINTS




DESIGN: X502/MLB CATZ		
LAST CHANGE: Thu Aug 4 21:00:42 2016		
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	PAGE	20 OF 500
	SHEET	19 OF 73



LPDDR3 CHANNEL A (0-31)



PLACEMENT NOTE:
100pF caps are shared between DRAM.
Distributed evenly.

SYNC MASTER=X502-EXP		SYNC DATE=12/03/2015	
PAGE TITLE			
LPDDR3 DRAM Channel A		(00-31)	
	Apple Inc.	DRAWING NUMBER	051-02265
		REVISION	1.0.0
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BOM_COST_GROUP=DRAM

D



C


C

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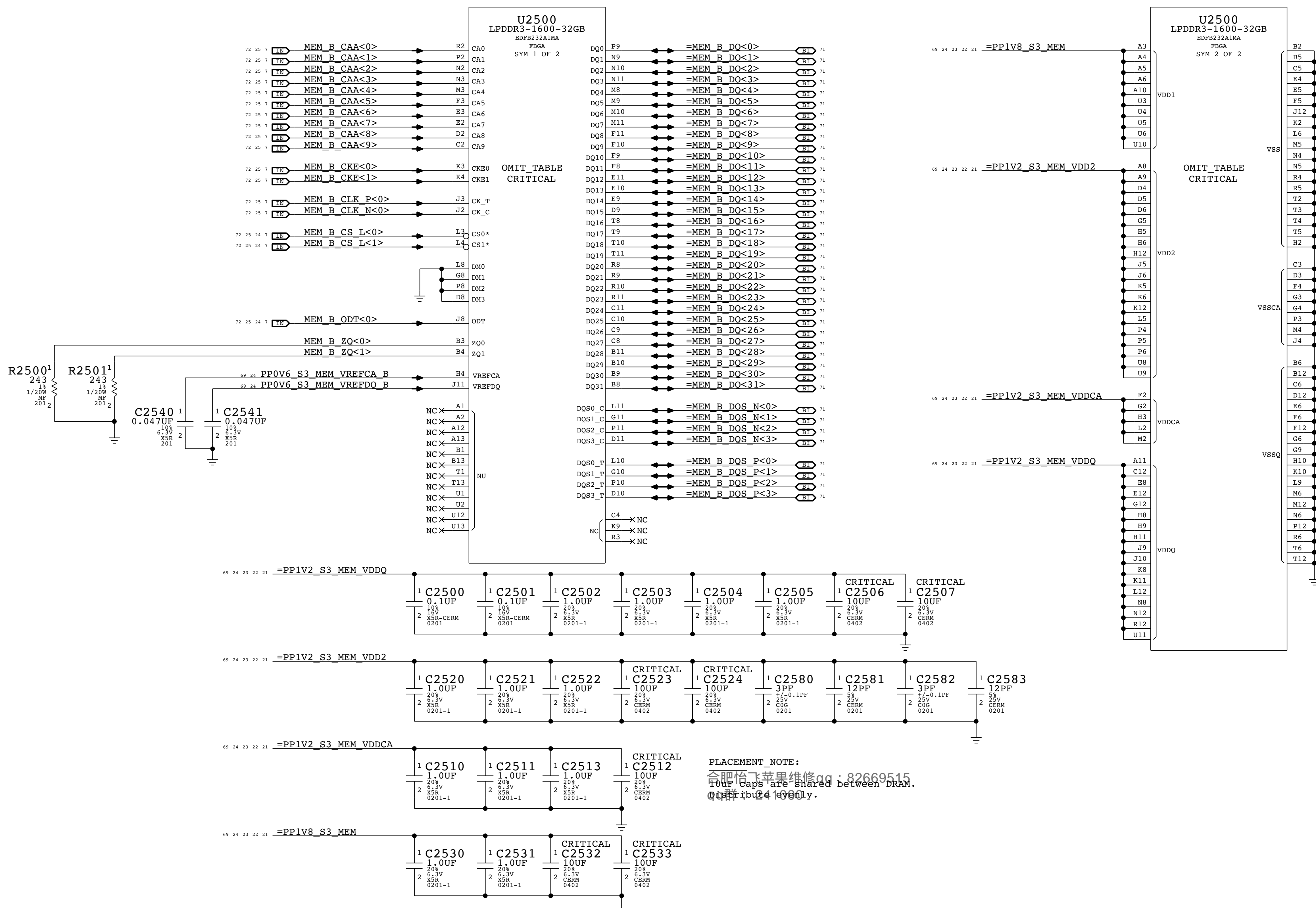
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A

A

SYNC MASTER-X502-EXP		SYNC_DATE=12/03/2015	
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LPDDR3 DRAM Channel A (32-63)			
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		BRANCH	
		PAGE	24 OF 500
		SHEET	22 OF 73

LPDDR3 CHANNEL B (0-31)



BOM_COST_GROUP=DRAM

D



C


C

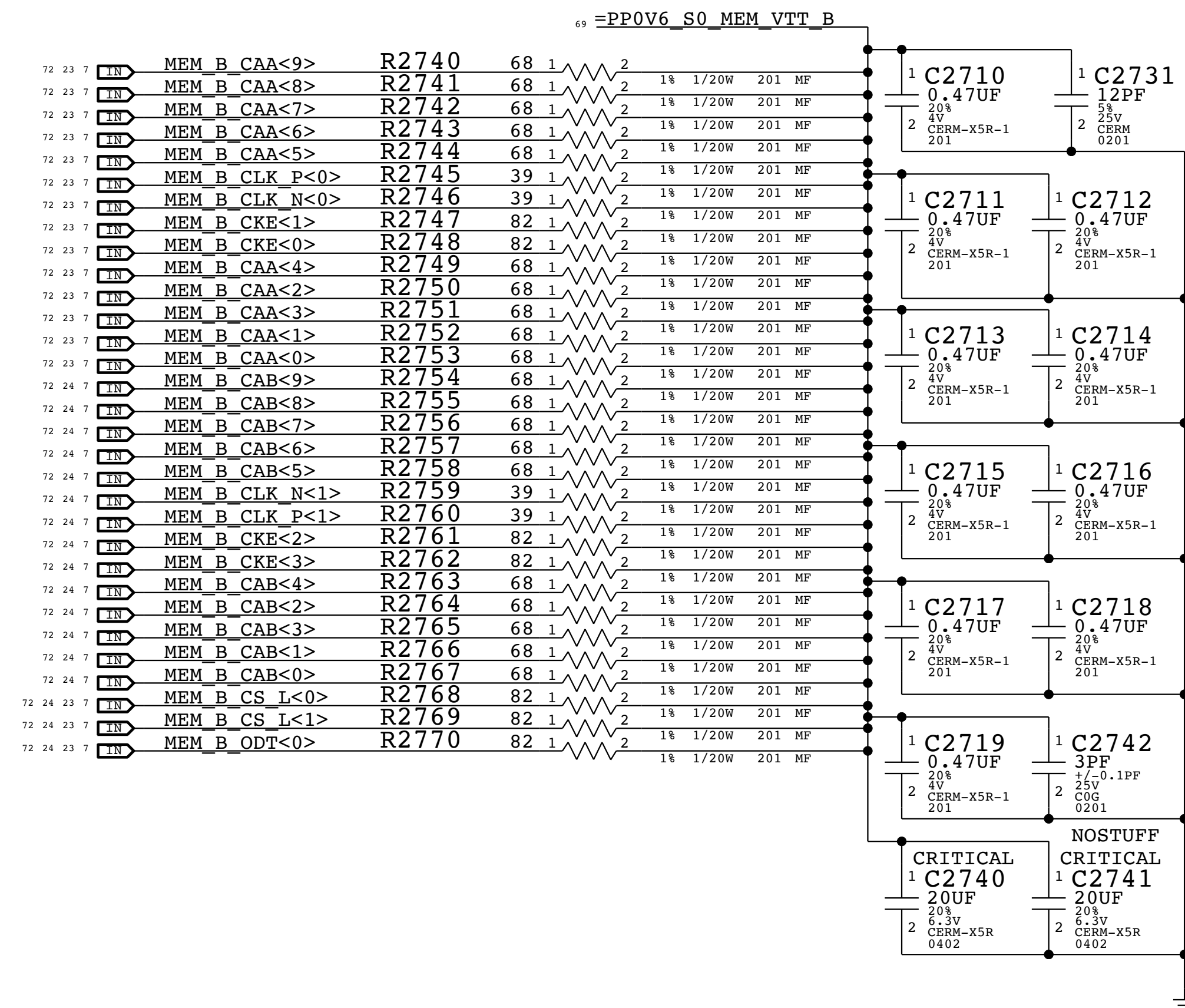
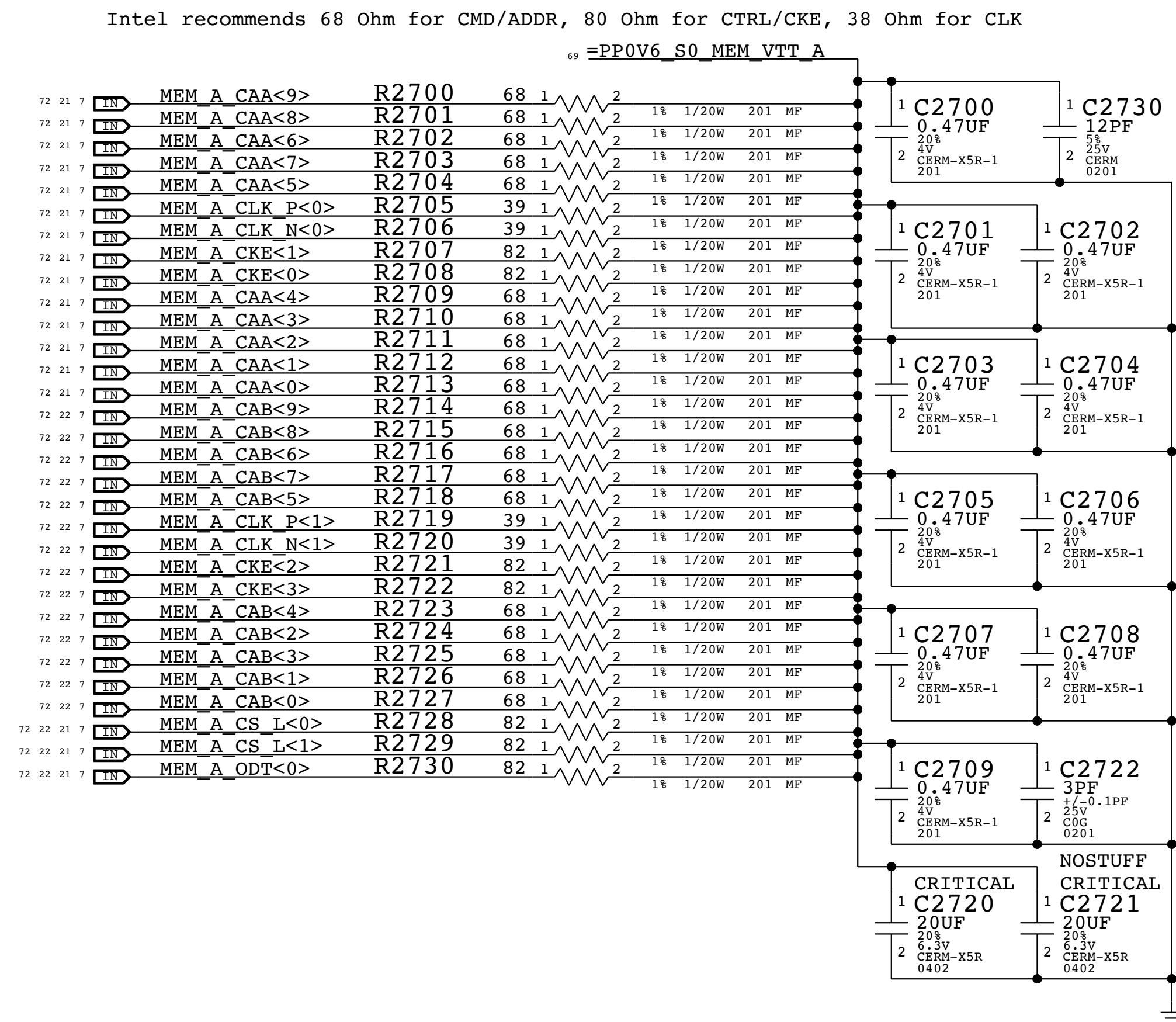
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B


A

A

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SYNC MASTER=X502-EXP		SYNC DATE=12/03/2015	
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LPDDR3 DRAM Termination			
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BOM_COST_GROUP=DRAM

D

C

B

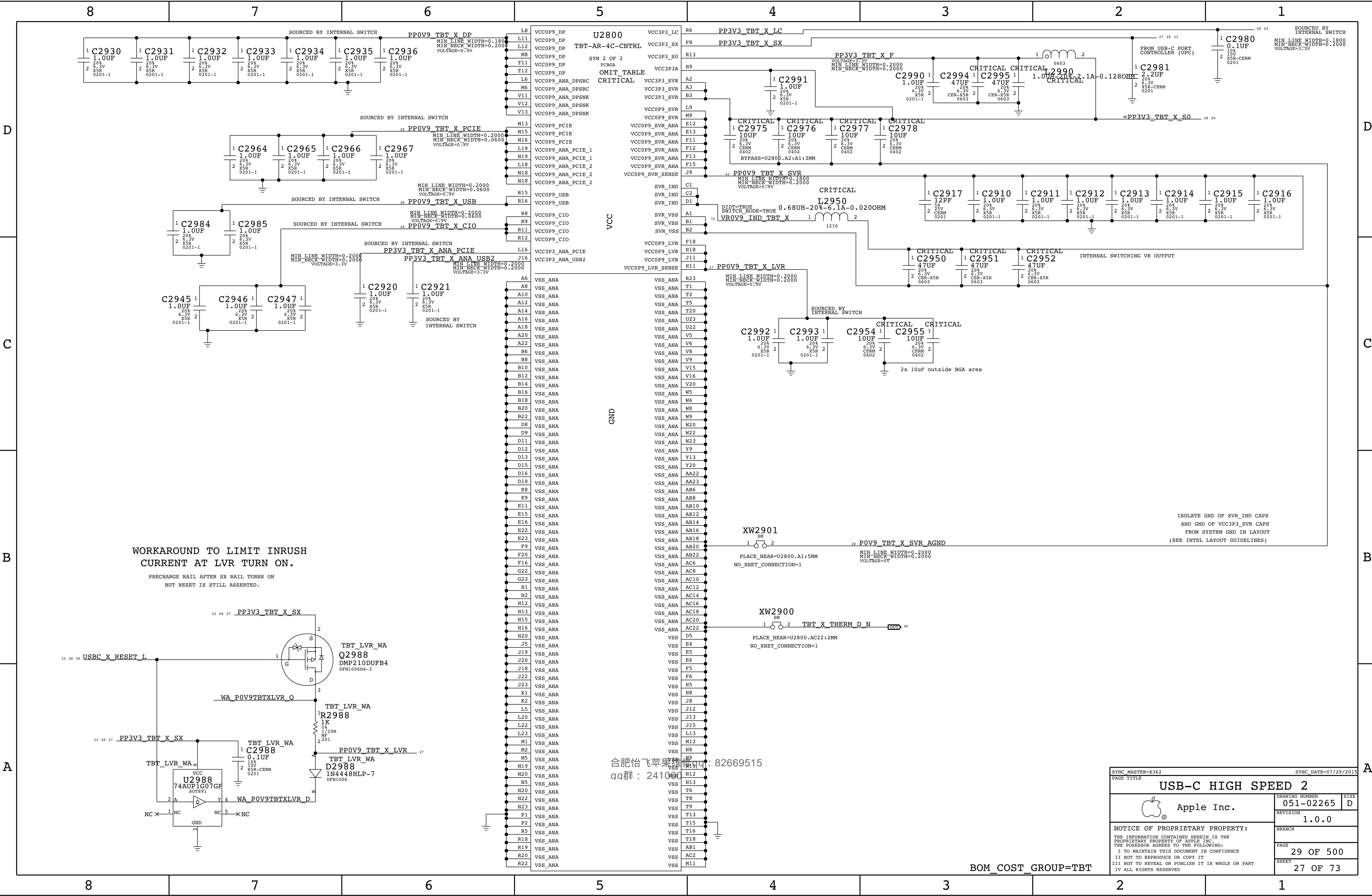
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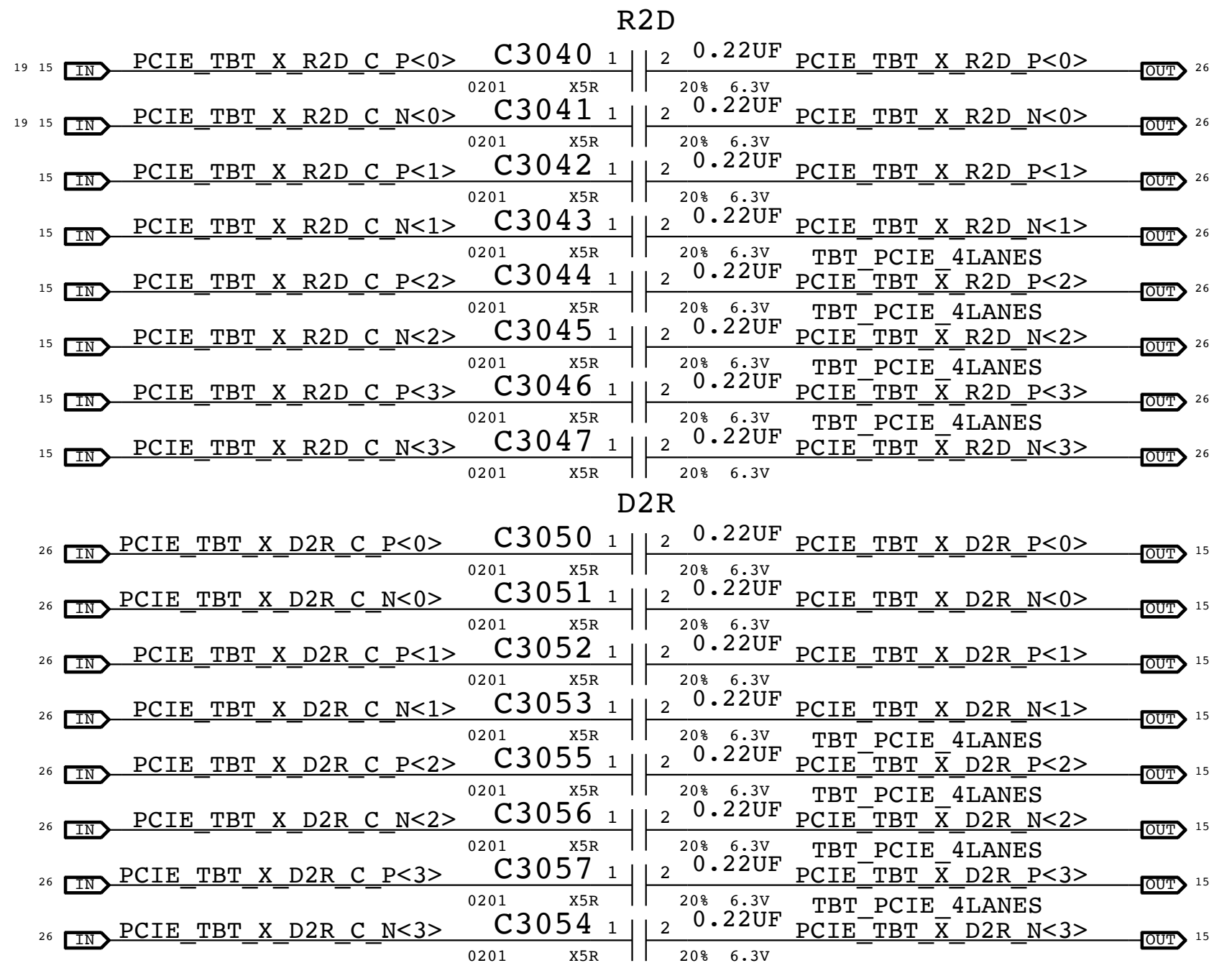
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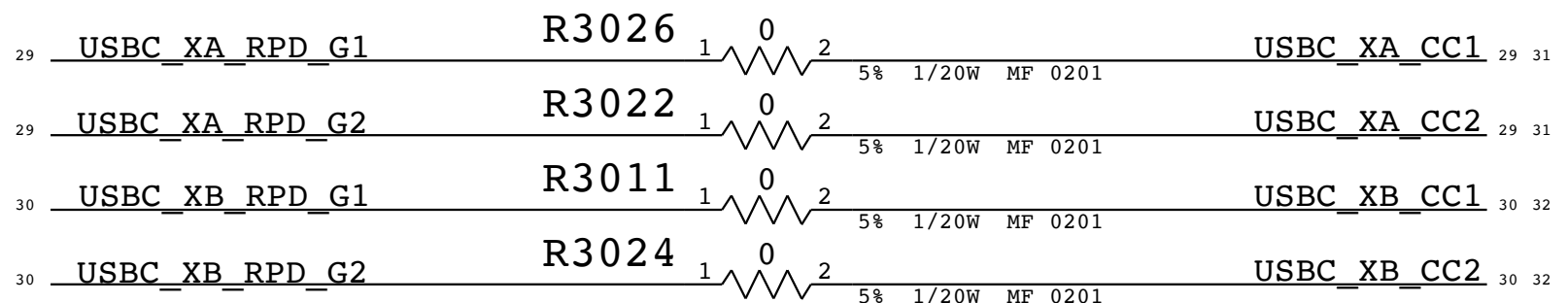
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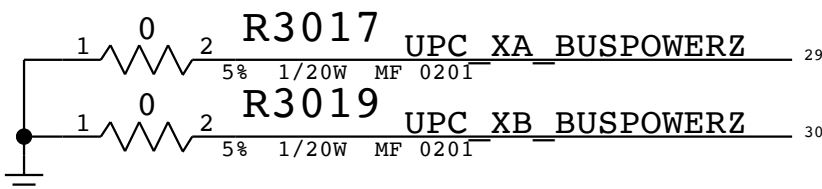


ACE RPD STRAPPING

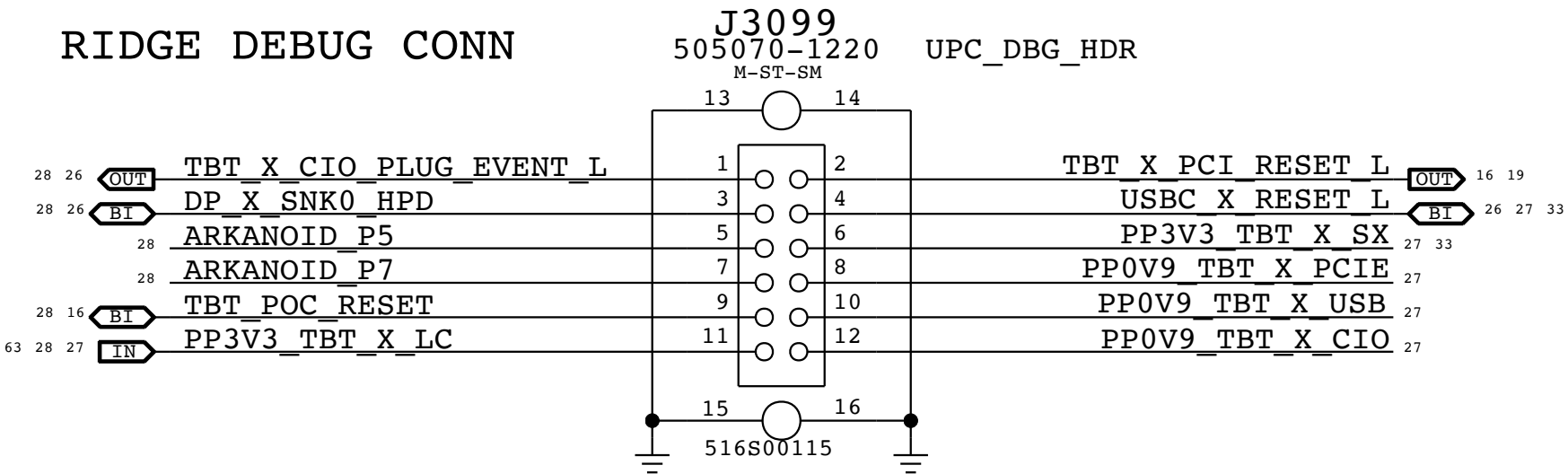
CONNECT G1/G2 TO CC1/CC2 TO RECEIVE POWER UNDER DB CASE
CONNECT G1/G2 TO GND TO NOT RECEIVE POWER UNDER DB CASE



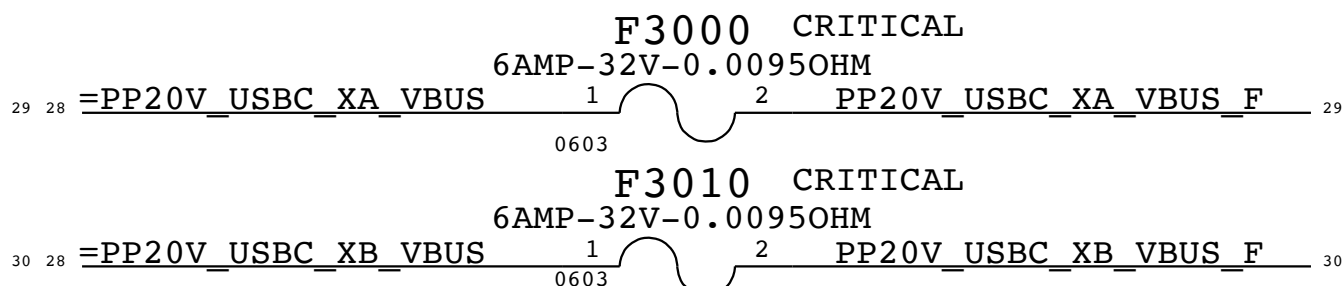
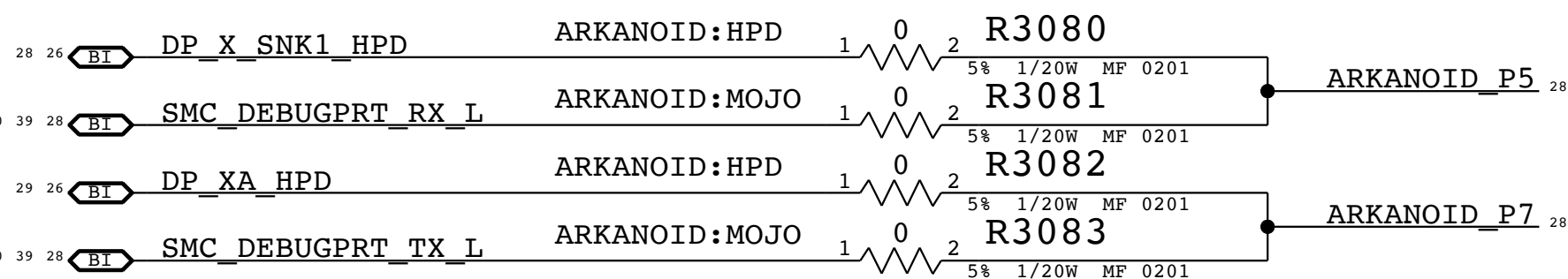
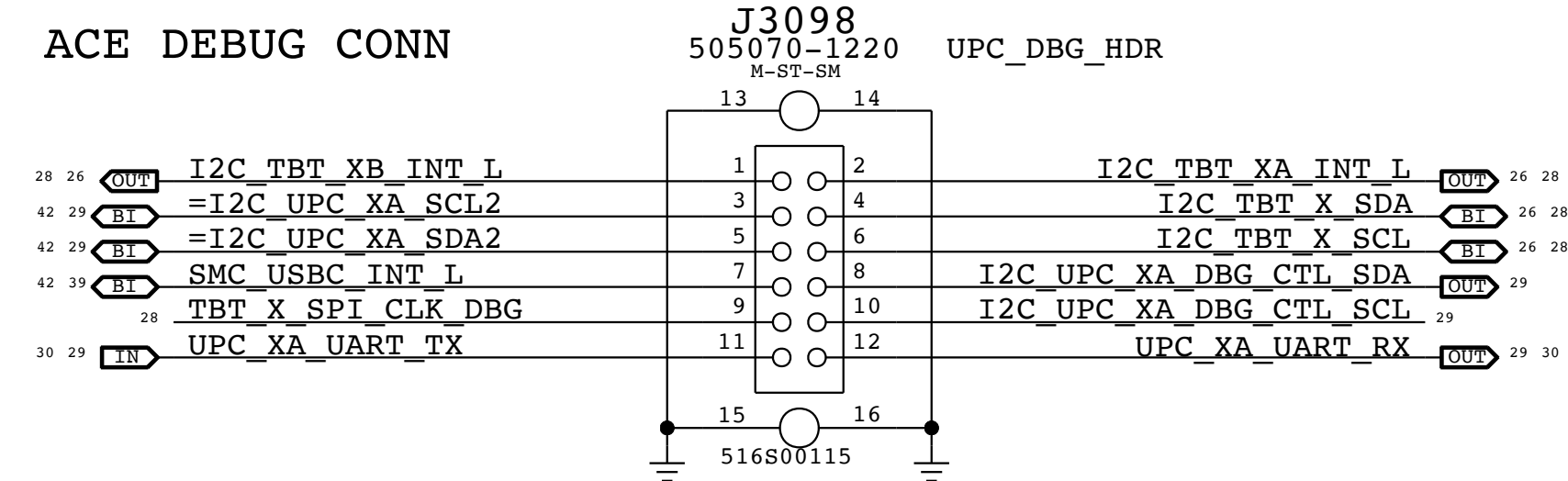
ACE BUSPOWERZ STRAPPING



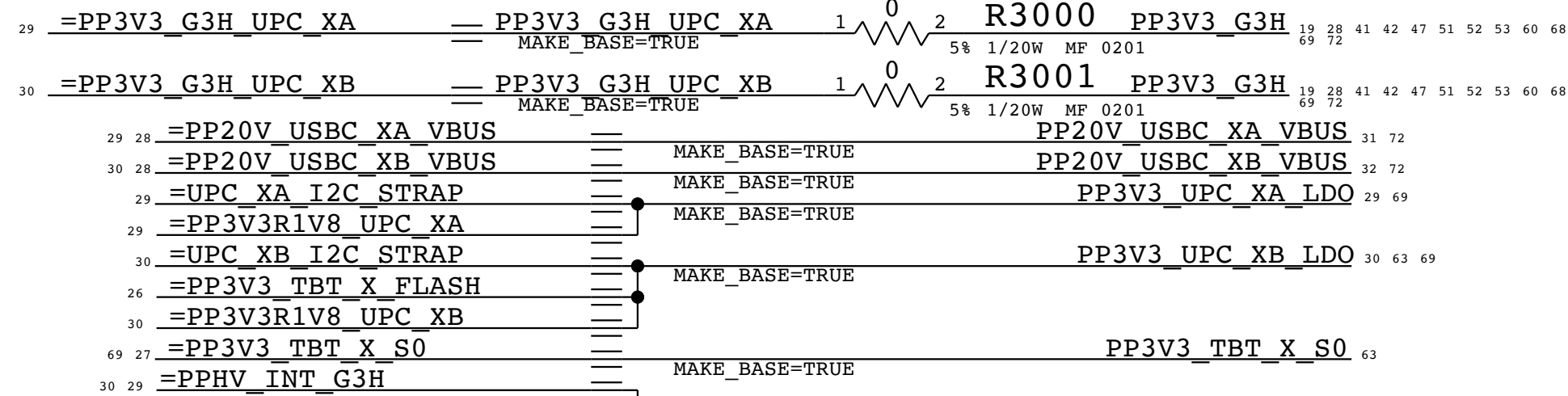
RIDGE DEBUG CONN



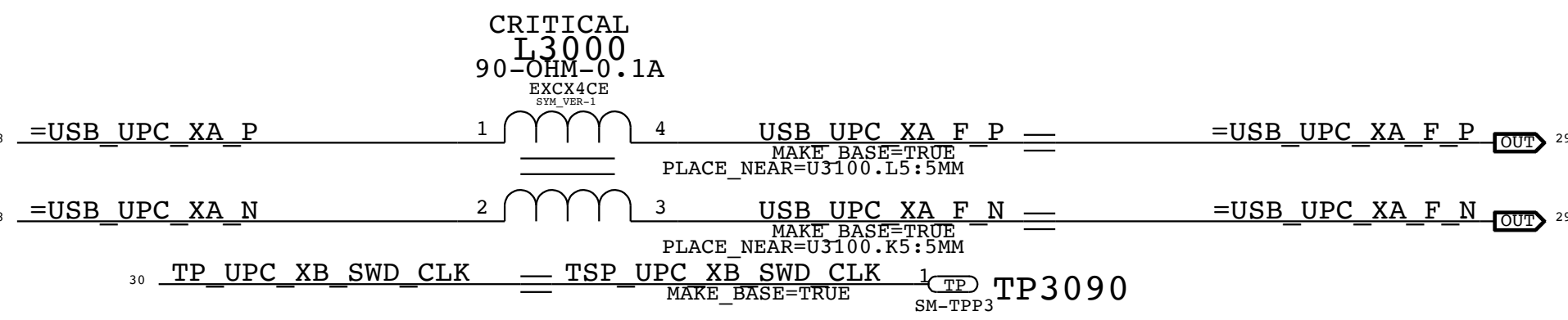
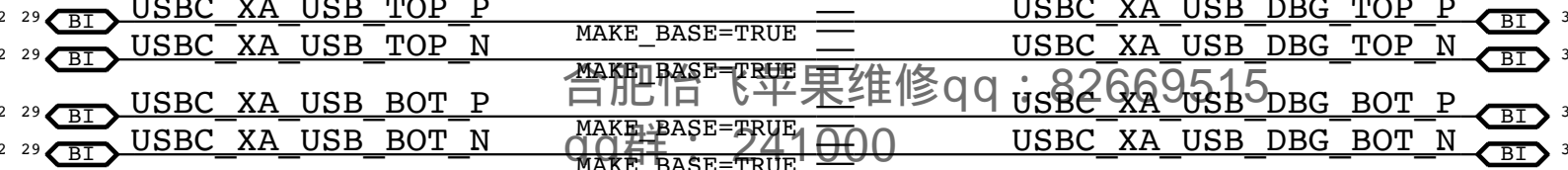
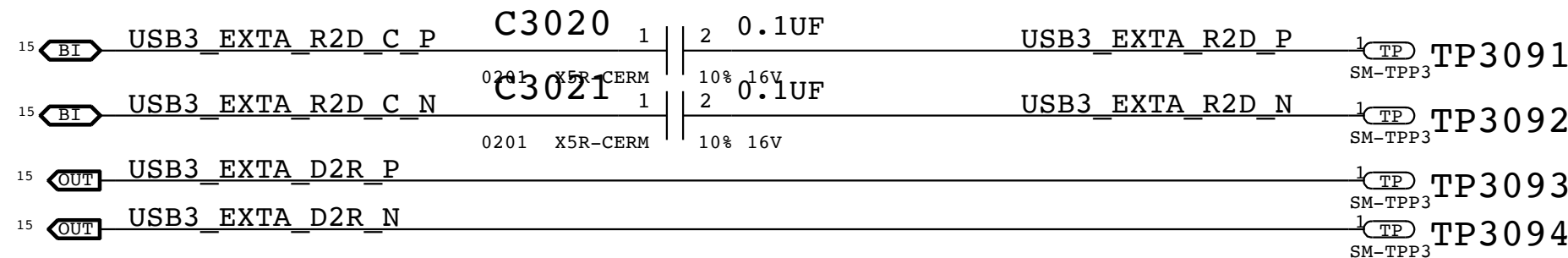
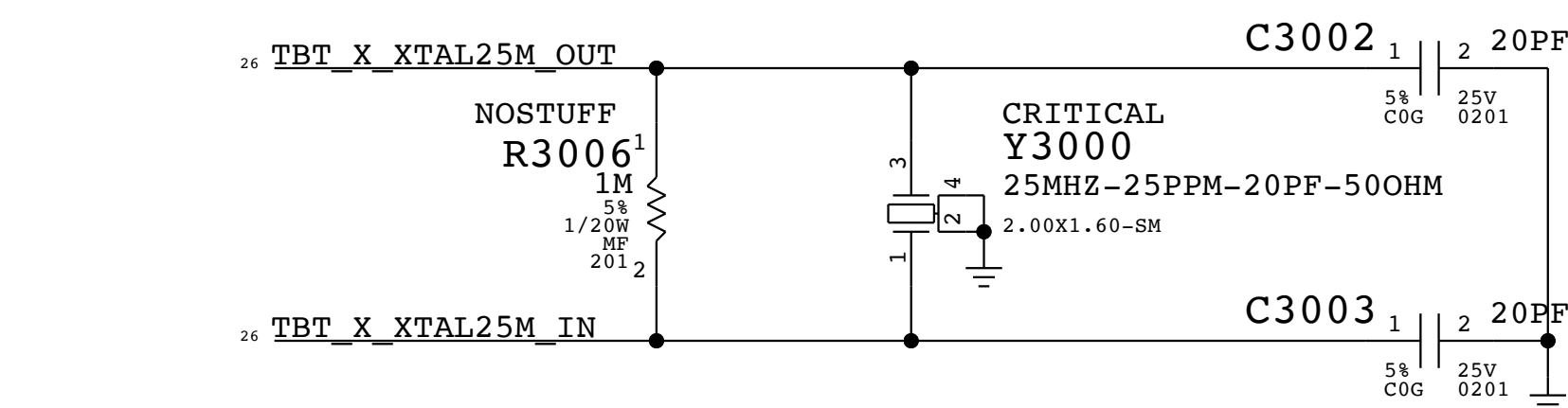
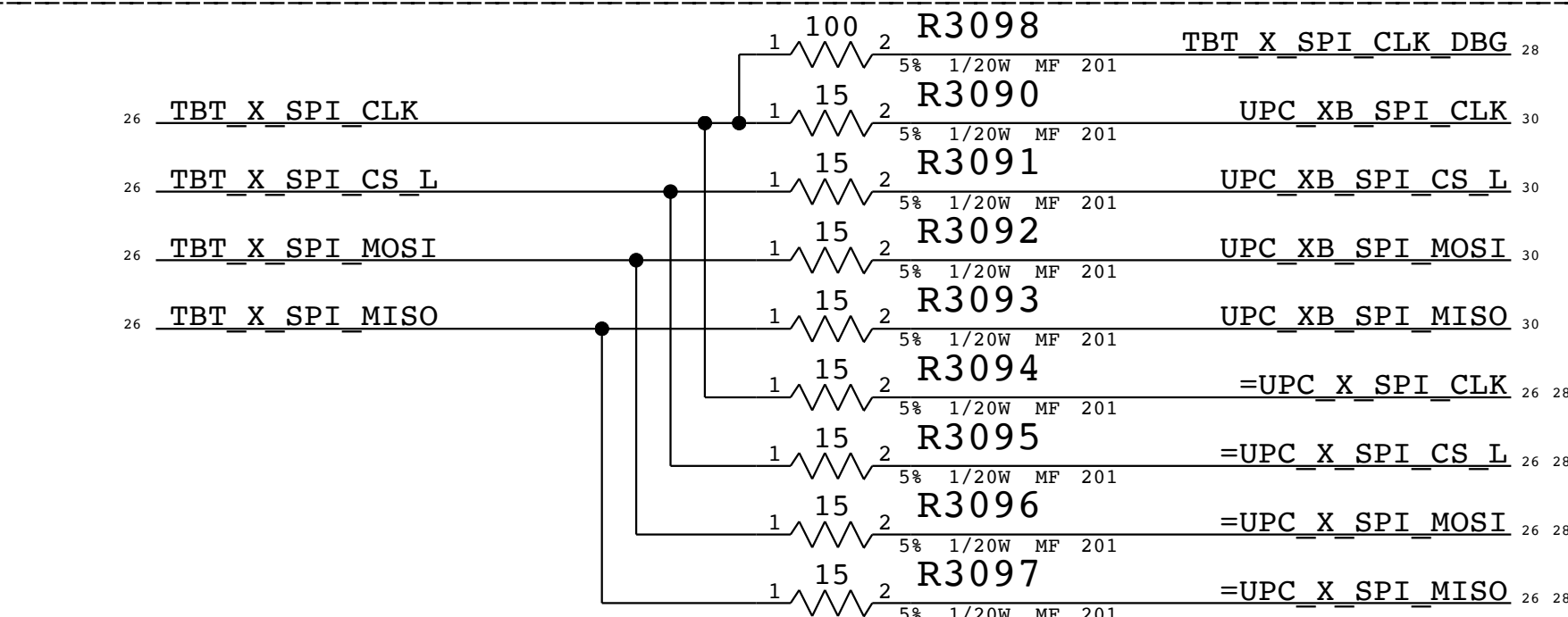
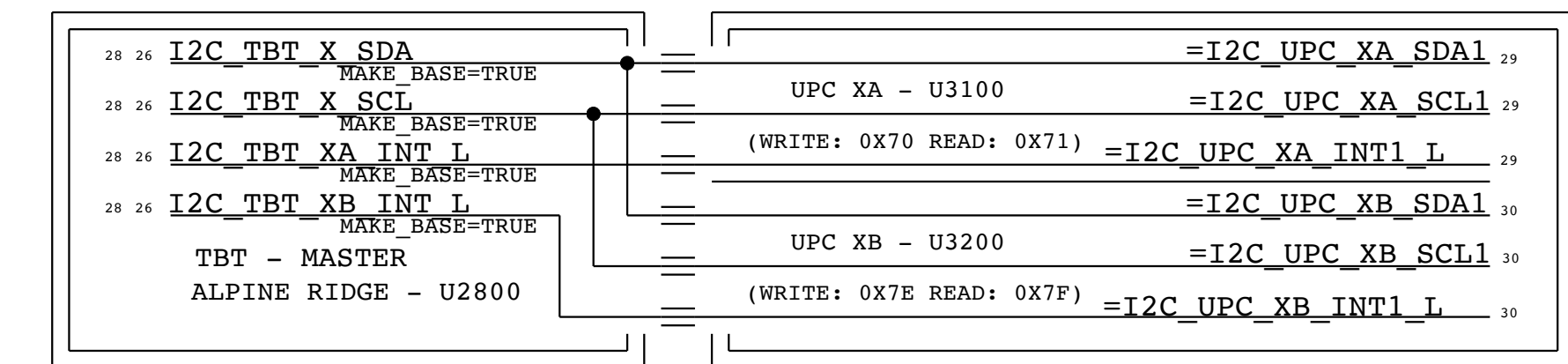
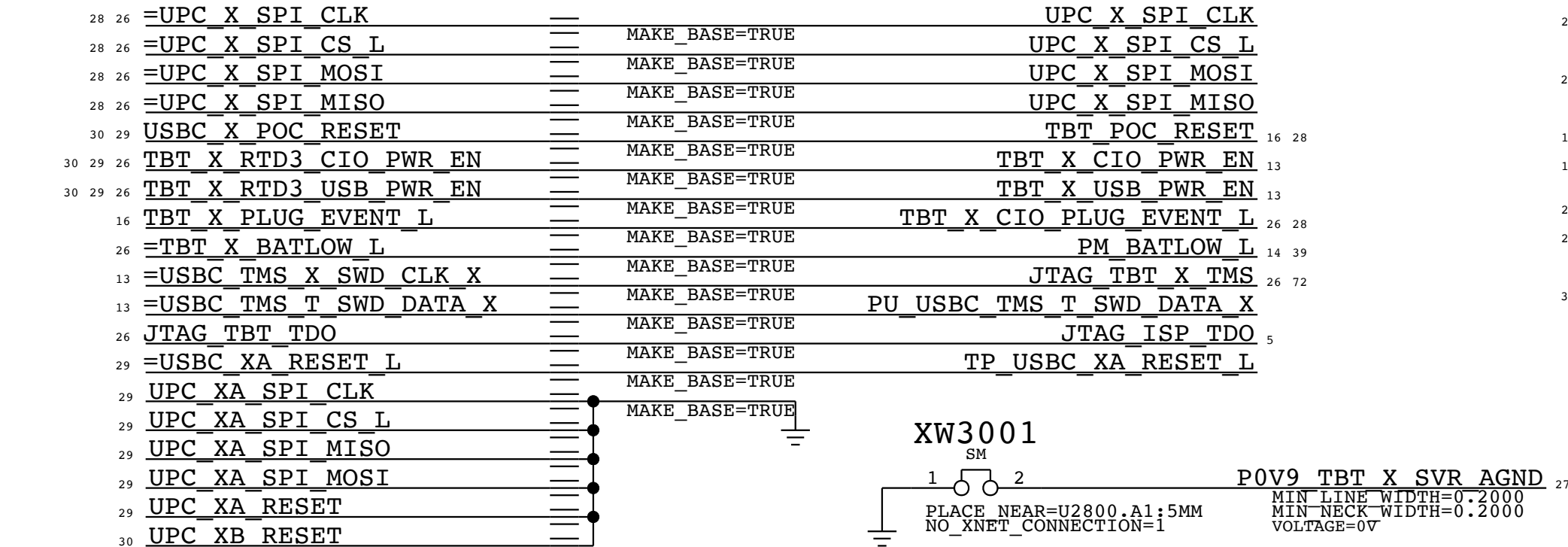
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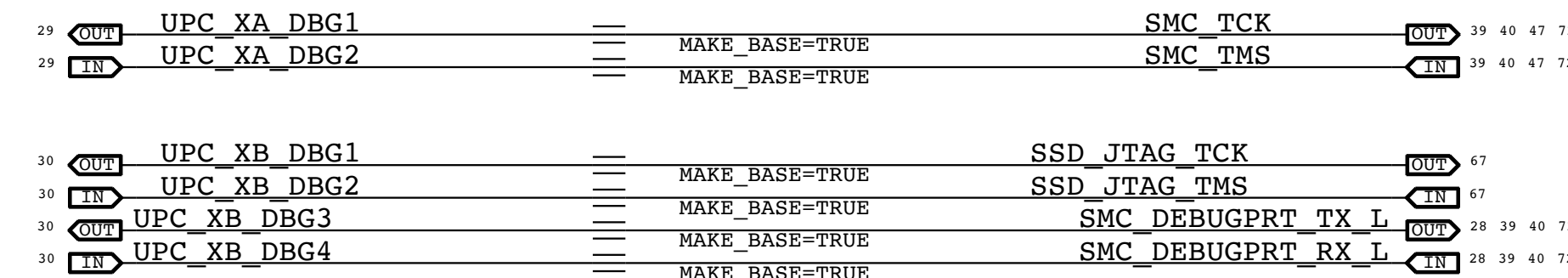
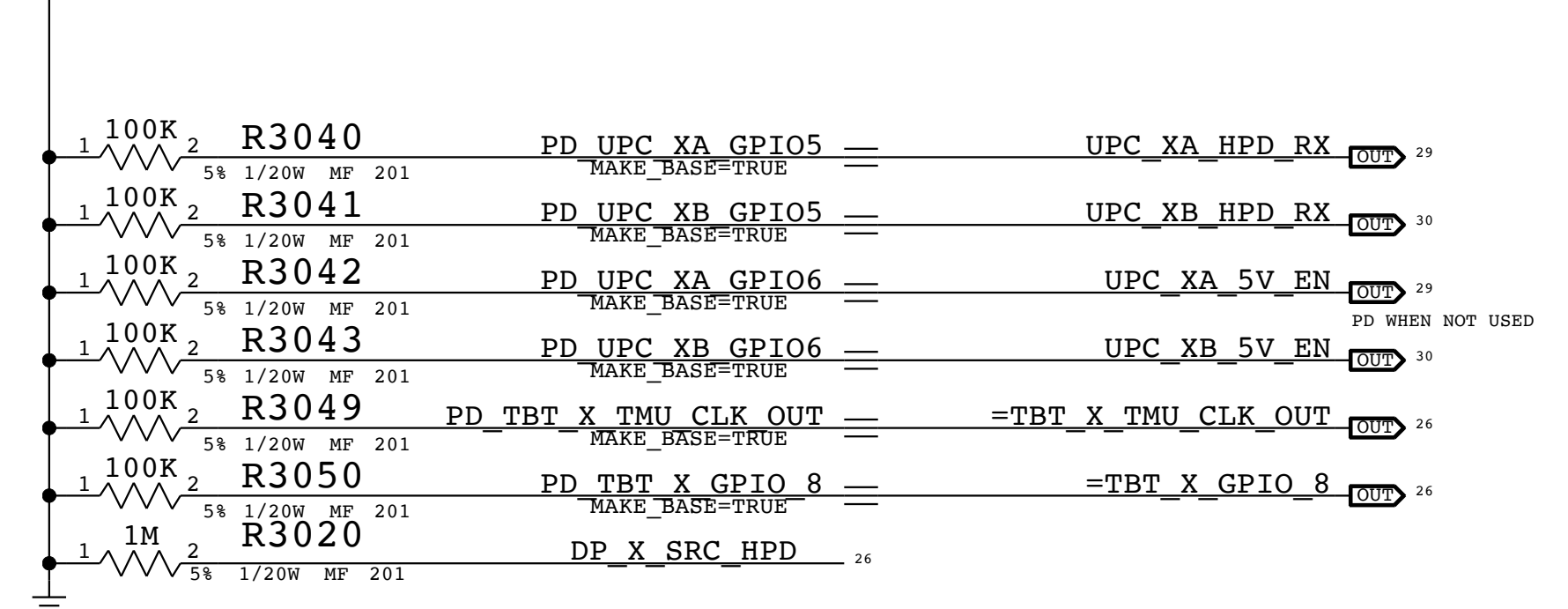
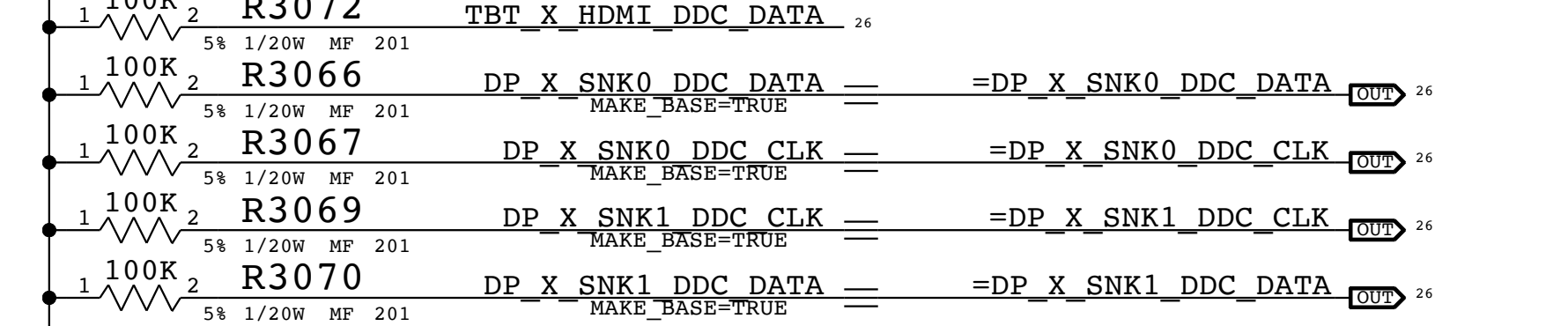
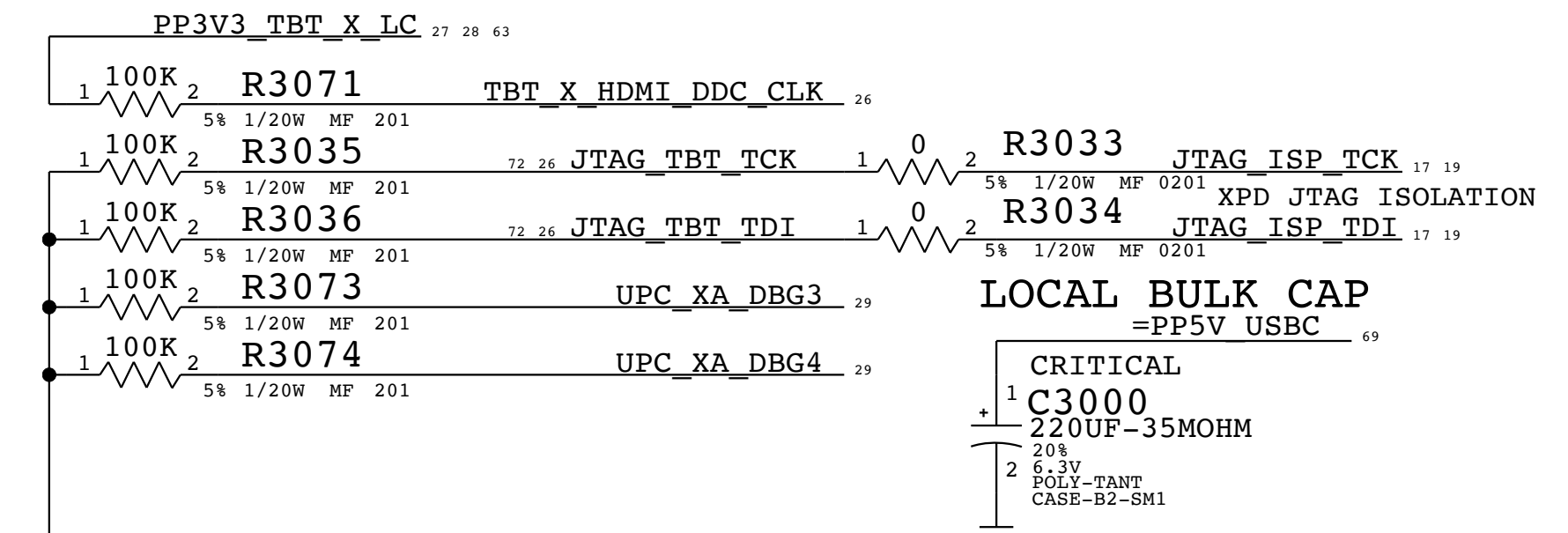
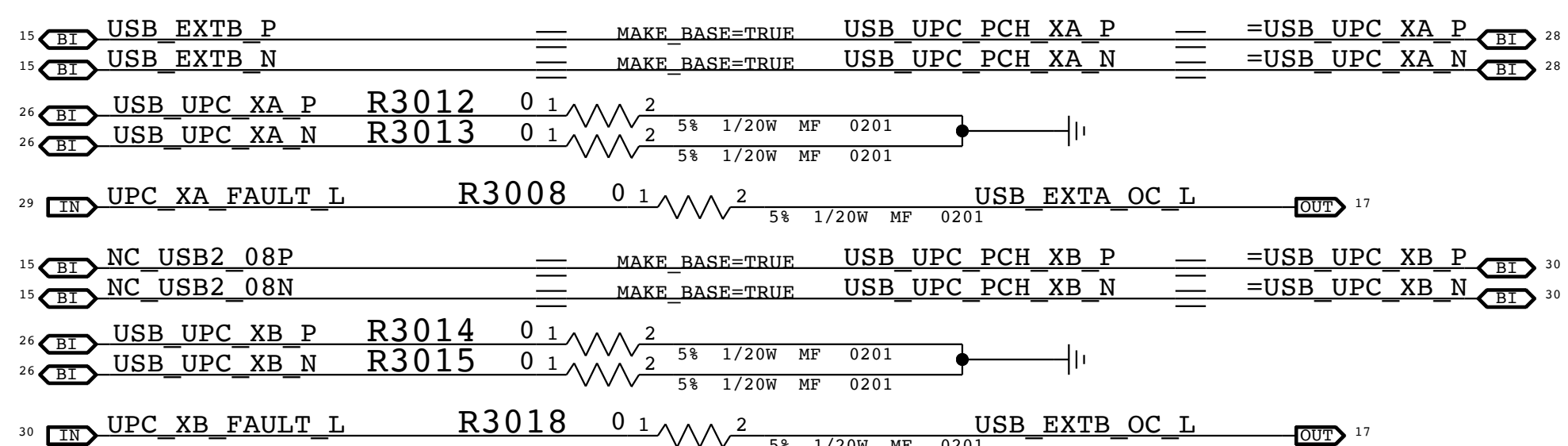
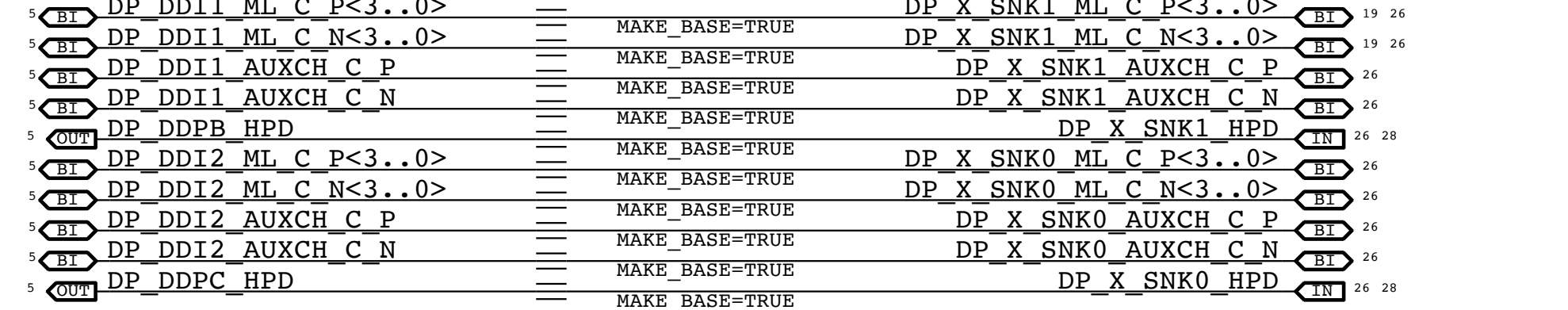
POWER ALIASES




MISC ALIASES



DP / USB SOURCE ALIASES



DESIGN: X502/MLB CATZ
LAST CHANGE: Fri Aug 5 13:34:33 2016

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USB-C SUPPORT		
	DRAWING NUMBER	051-02265
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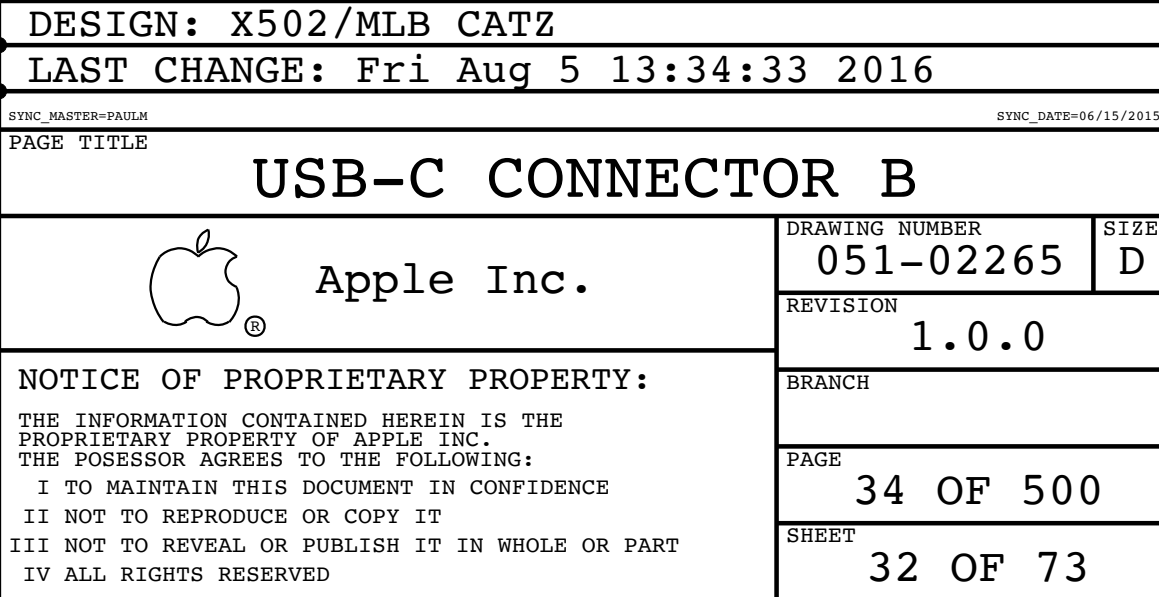
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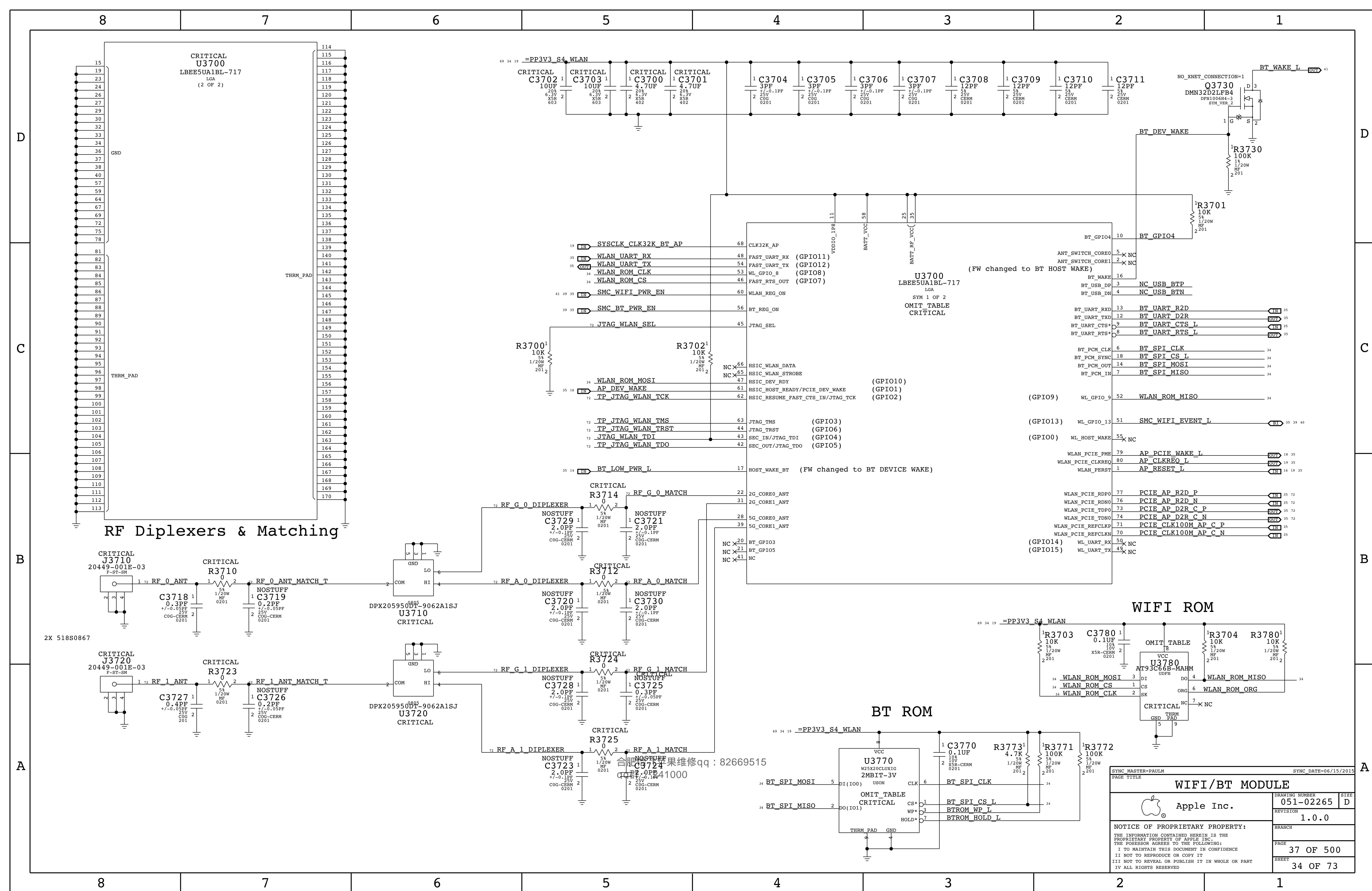
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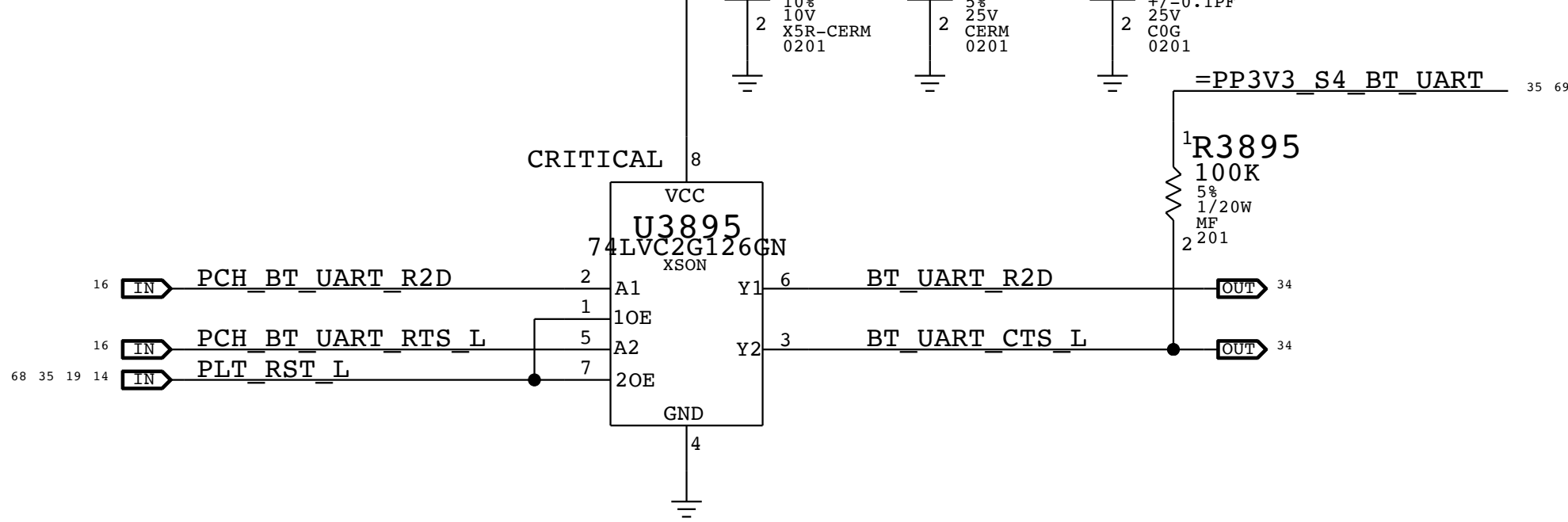
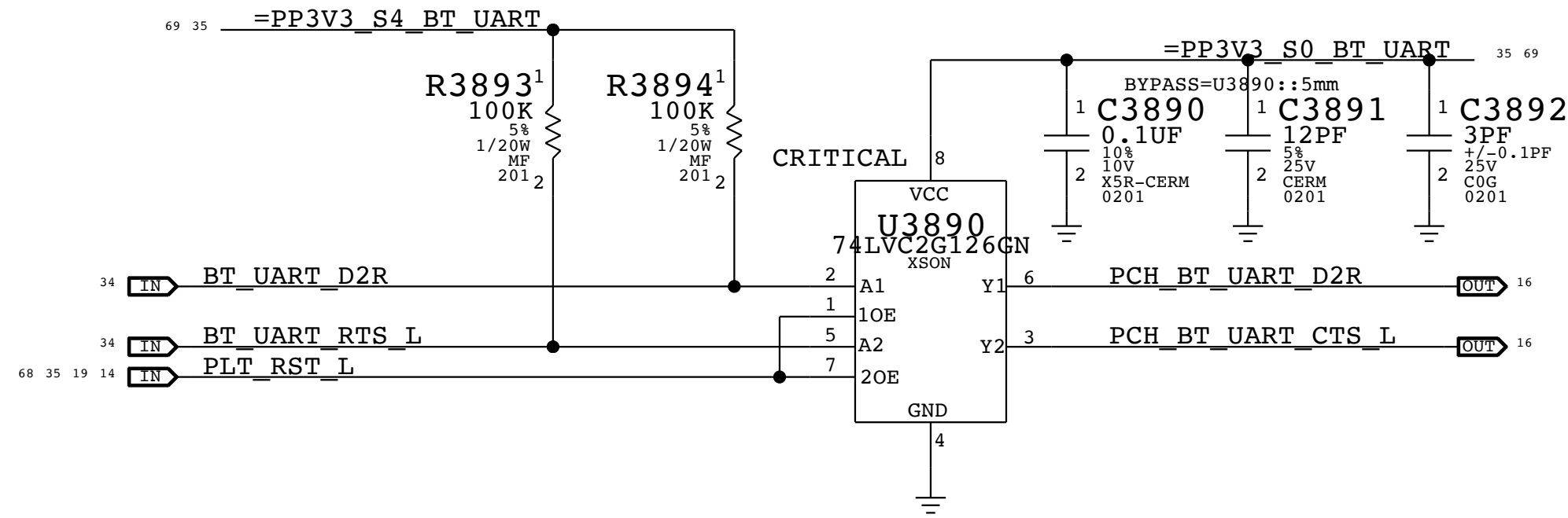
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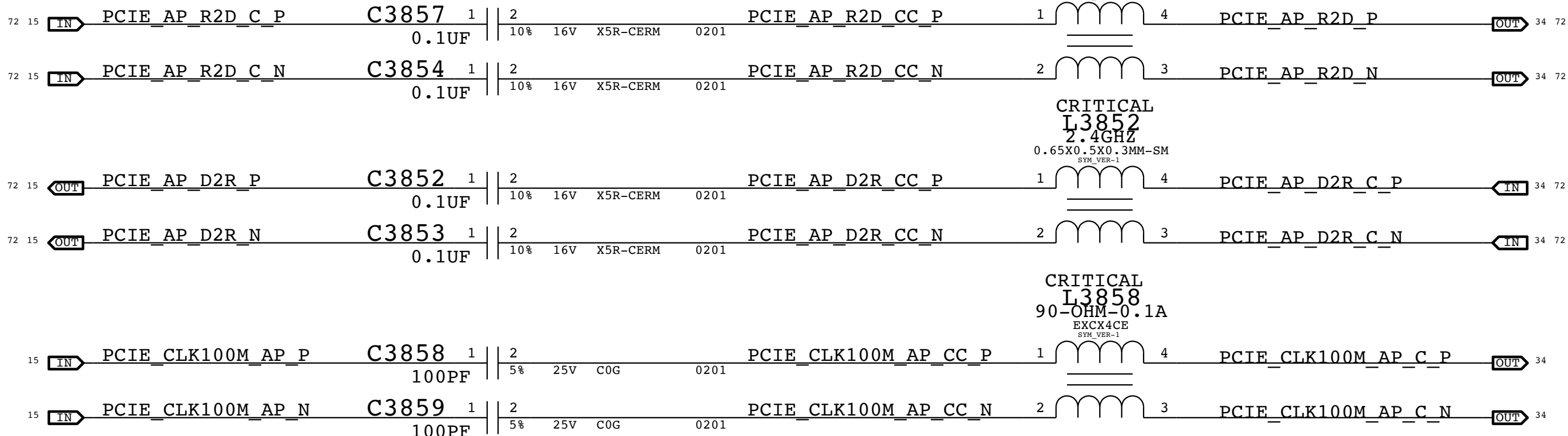
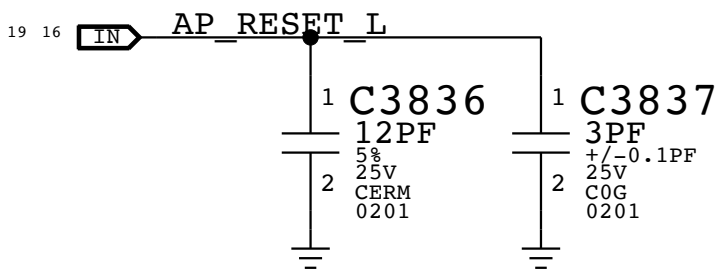
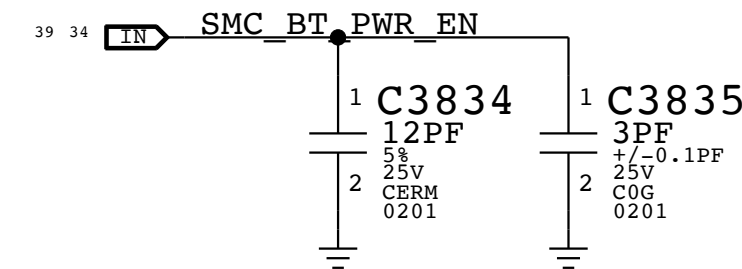
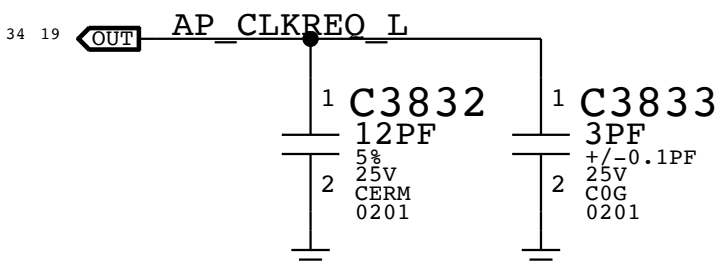
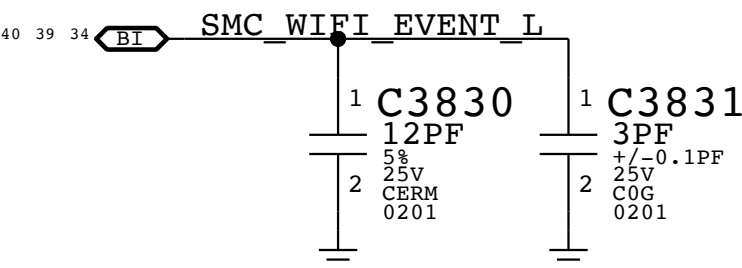
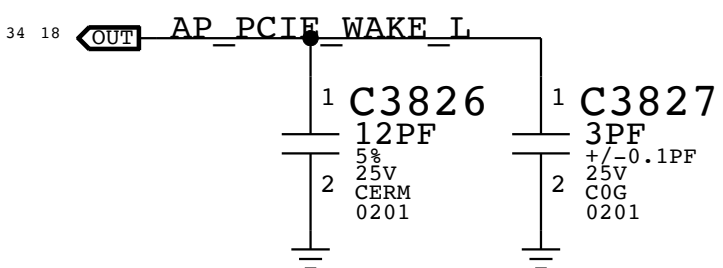
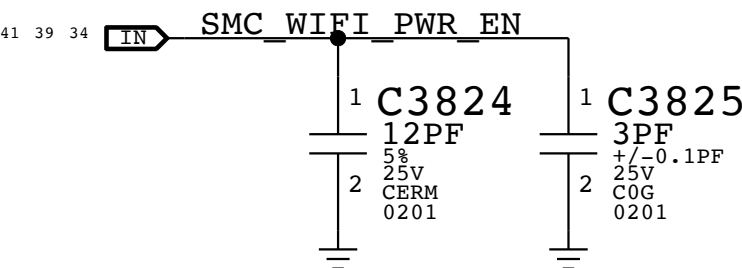
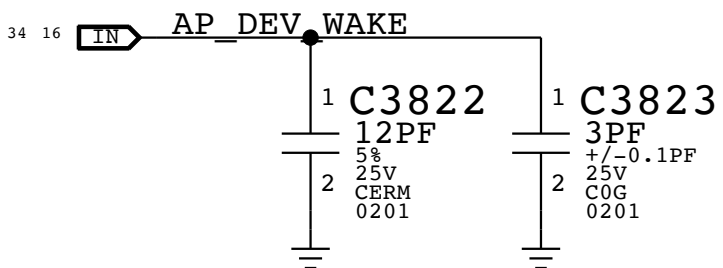
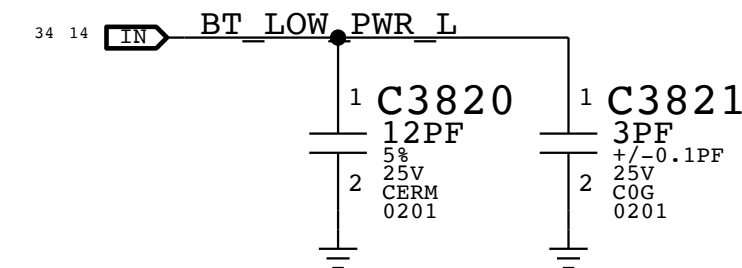
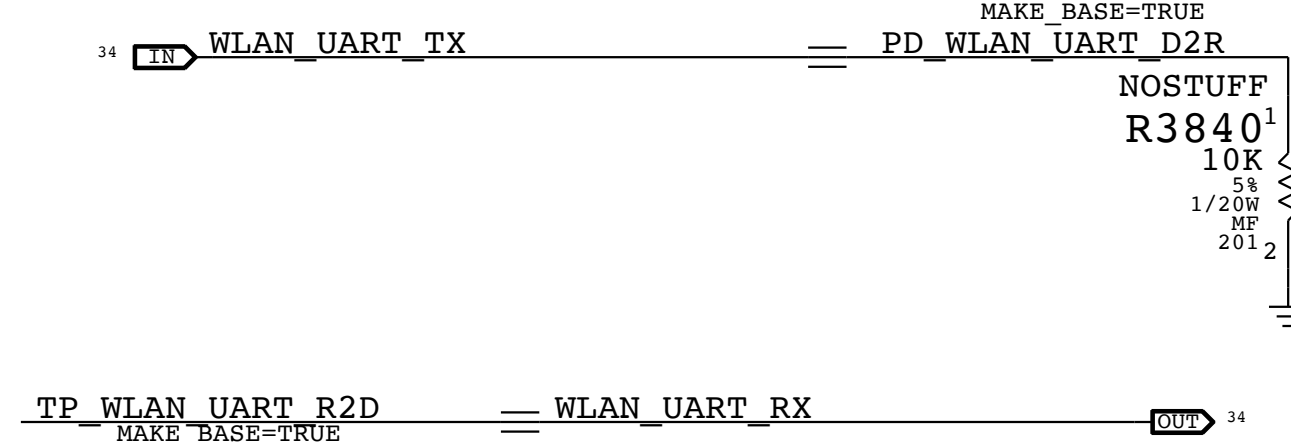





BT UART Isolation

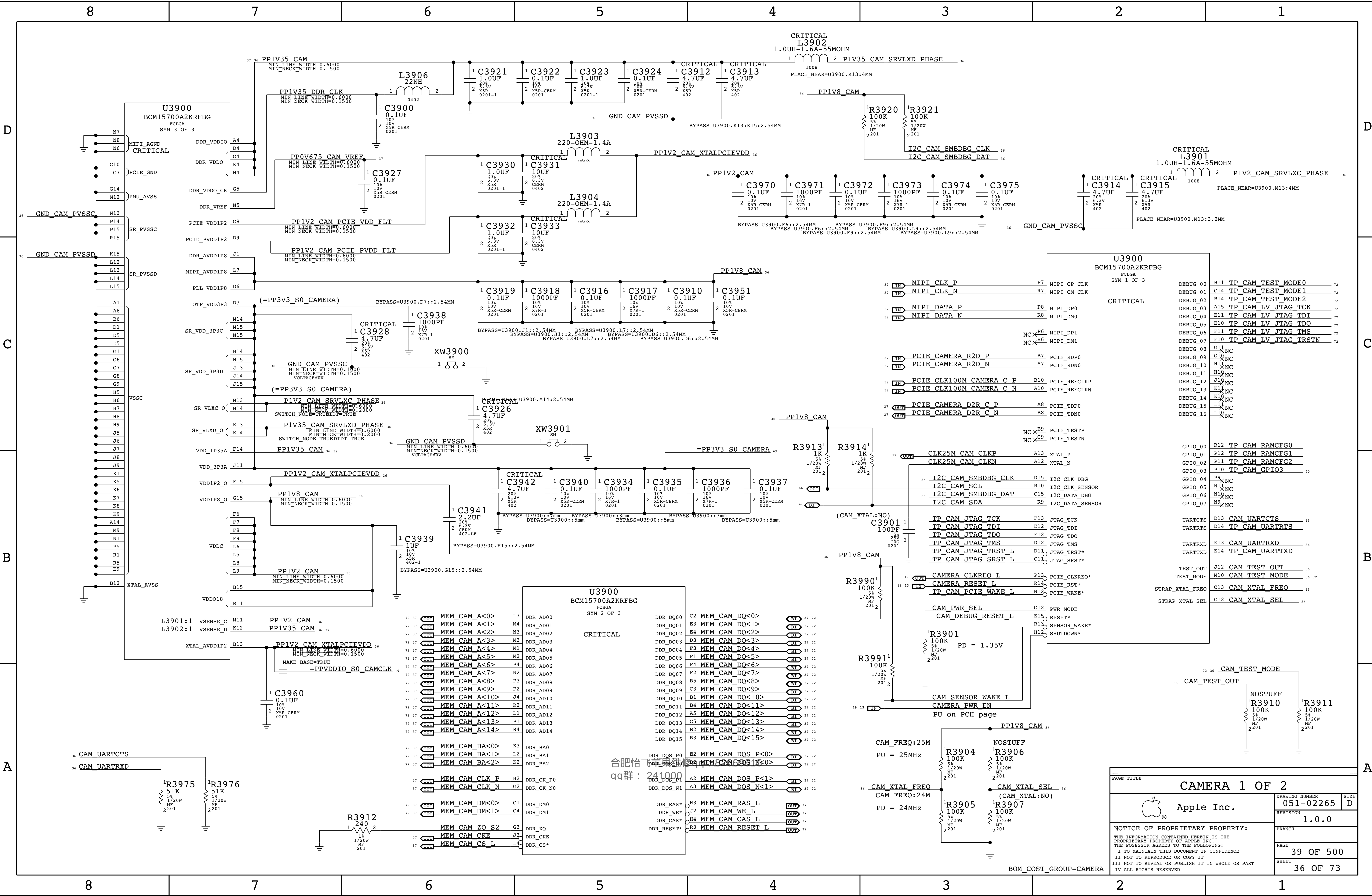


WIFI UART ISOLATION



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qq群：241000

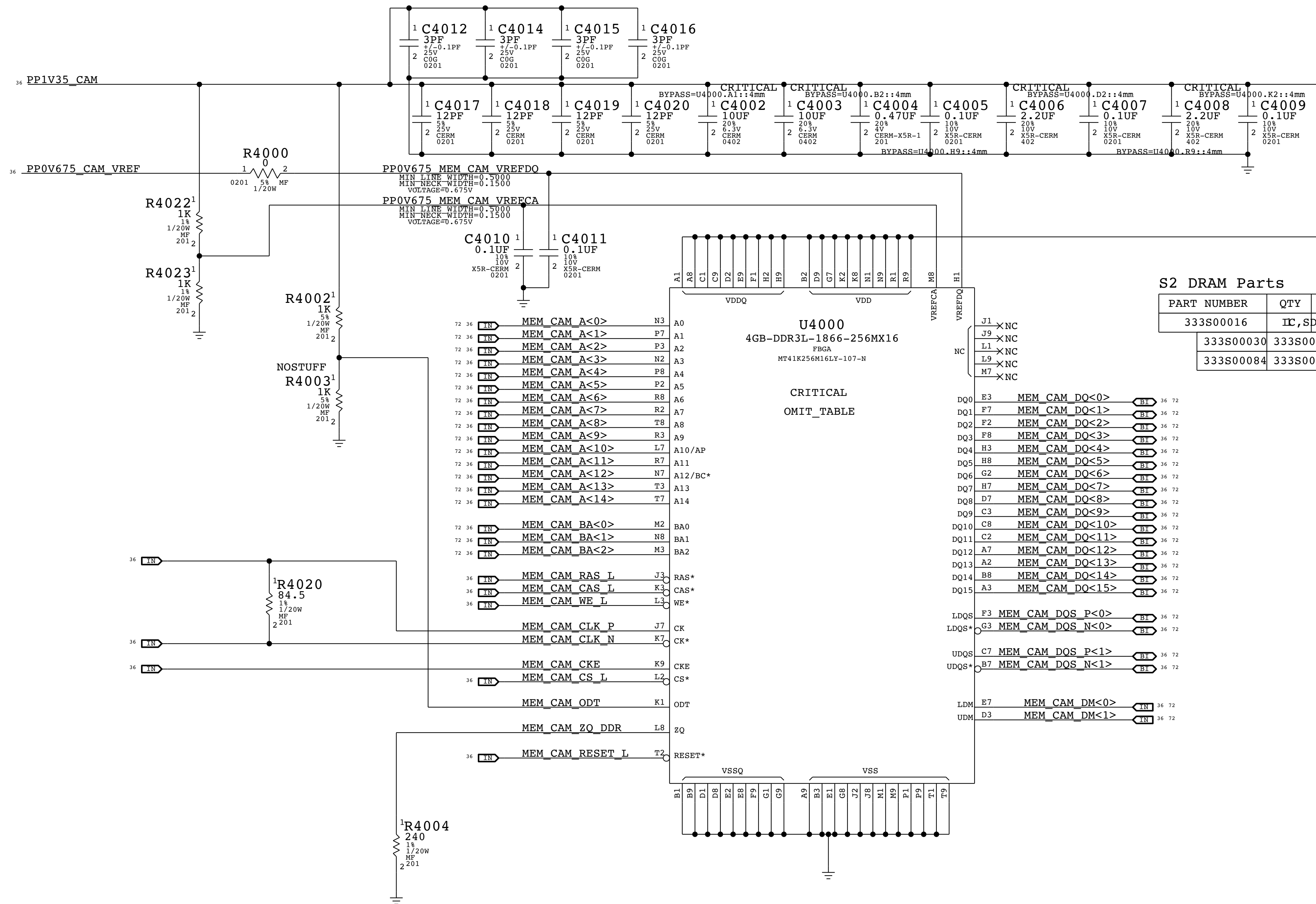
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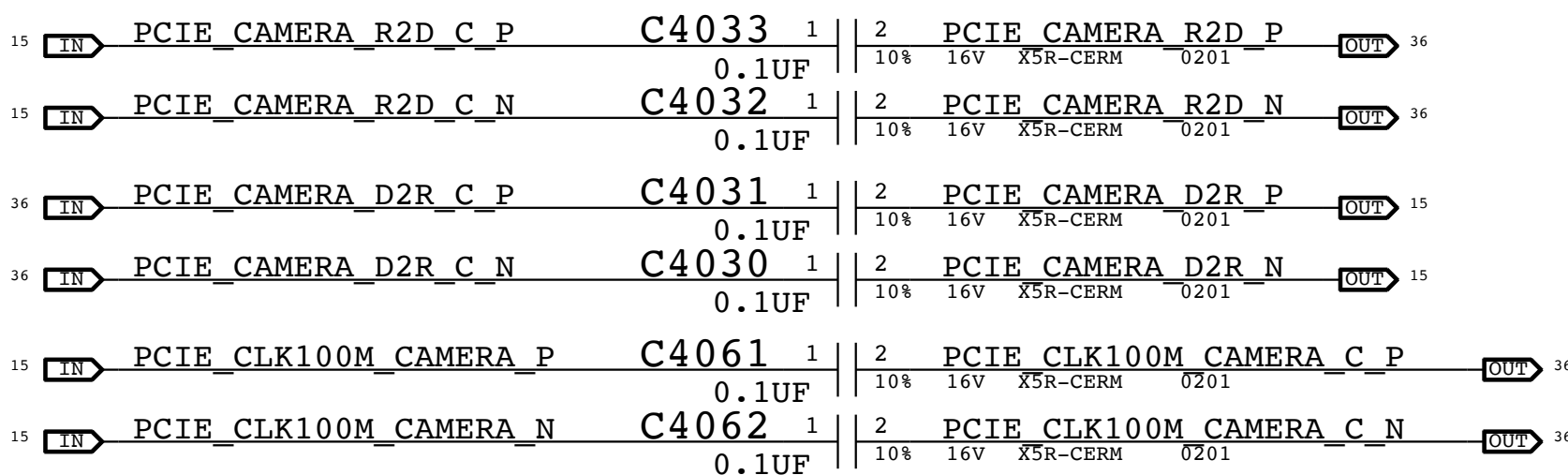
合肥怡飞
qq群: 241000

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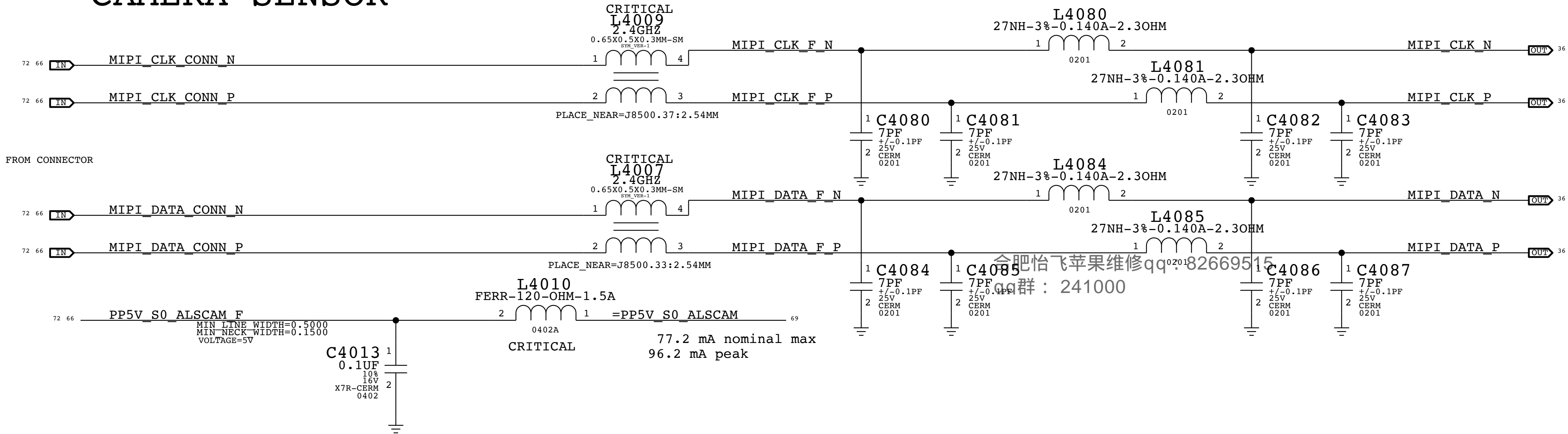


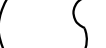
S2 DRAM Parts

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	333S00030	333S00016			HYNIX ALT TO MICRON FOR S2 CAMERA DDR3 MEMORY
	333S00084	333S00016			MICRON 20NM FOR S2 CAMERA DDR3 MEMORY



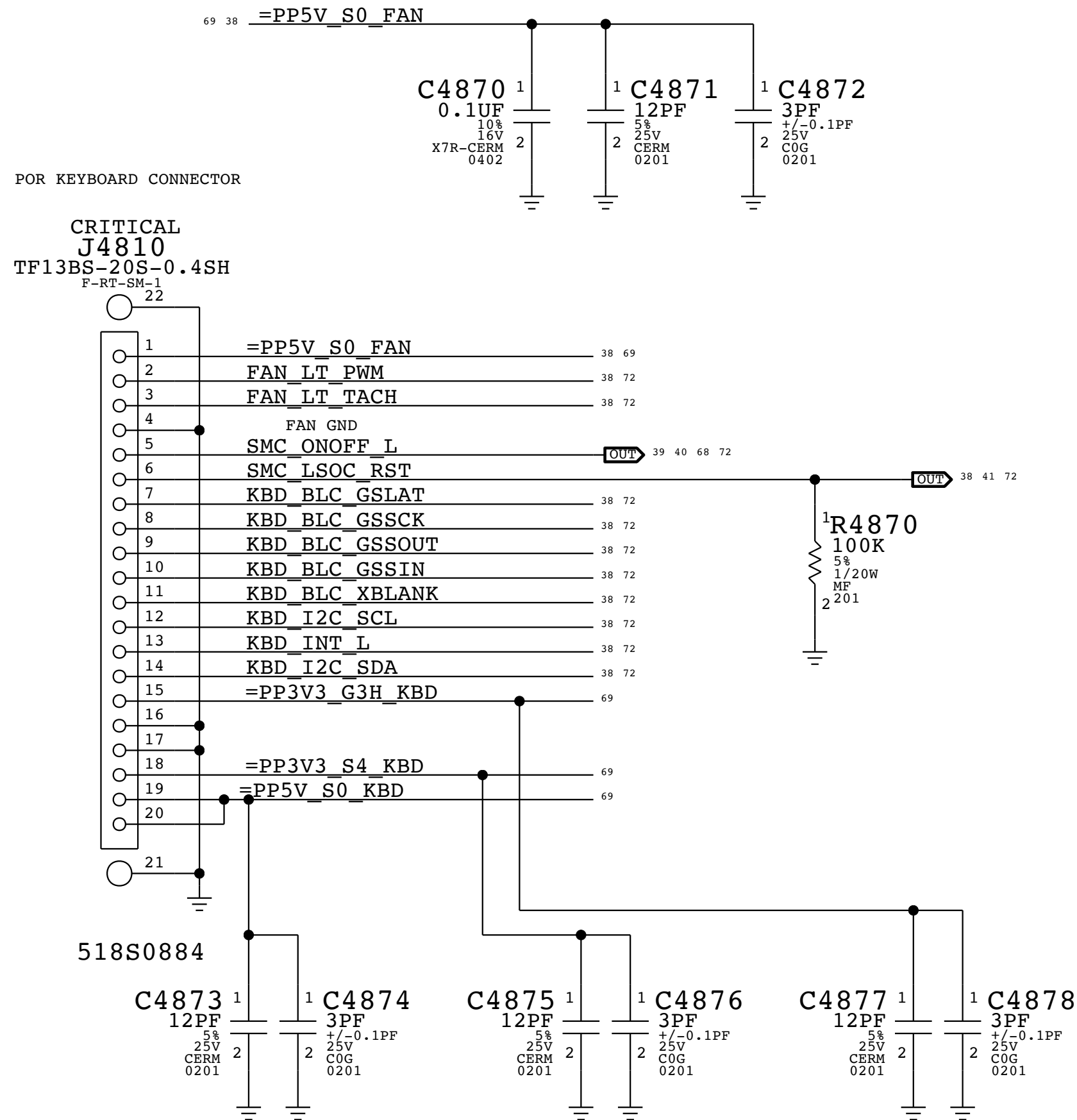
CAMERA SENSOR



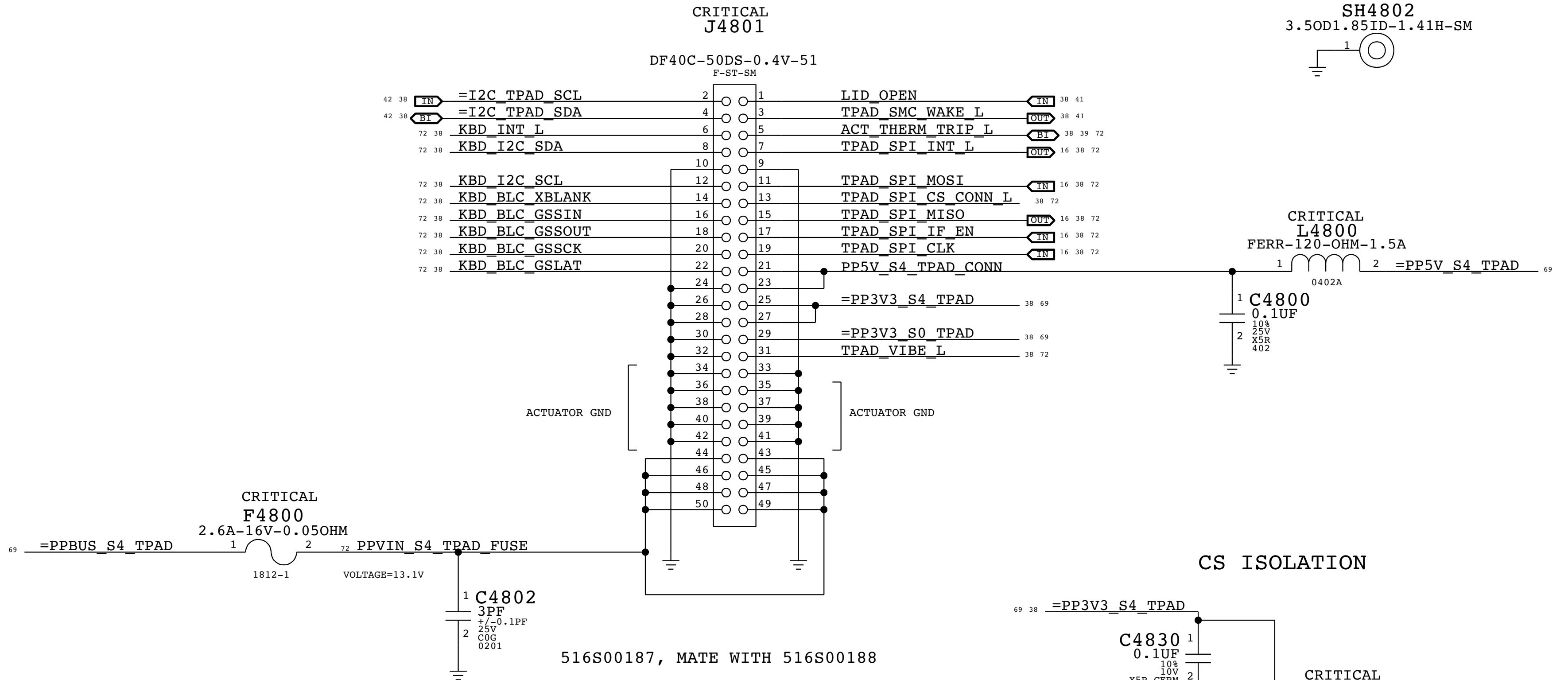
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CAMERA 2 OF 2			
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BOM_COST_GROUP=CAMERA

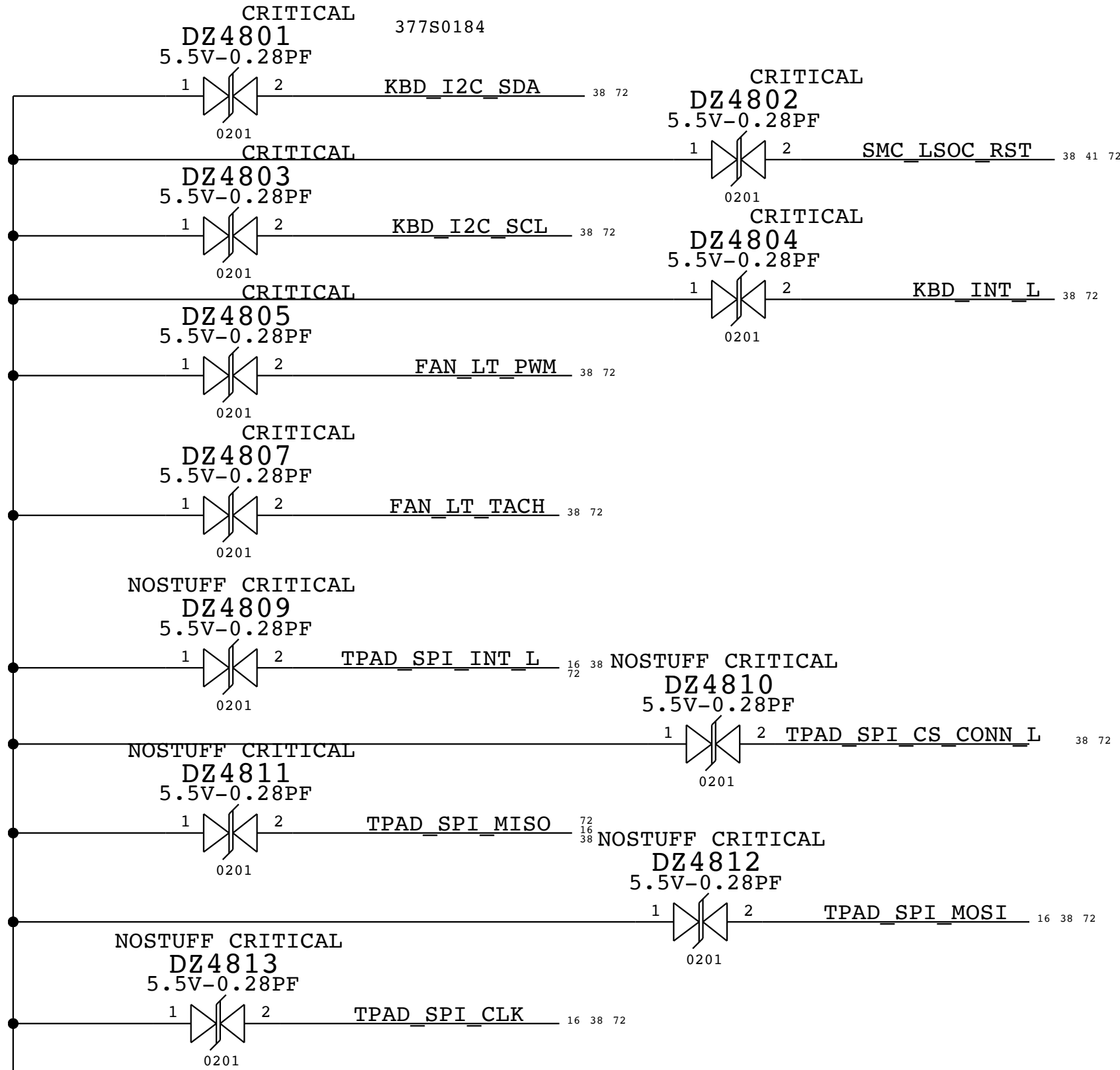
KEYBOARD CONNECTOR



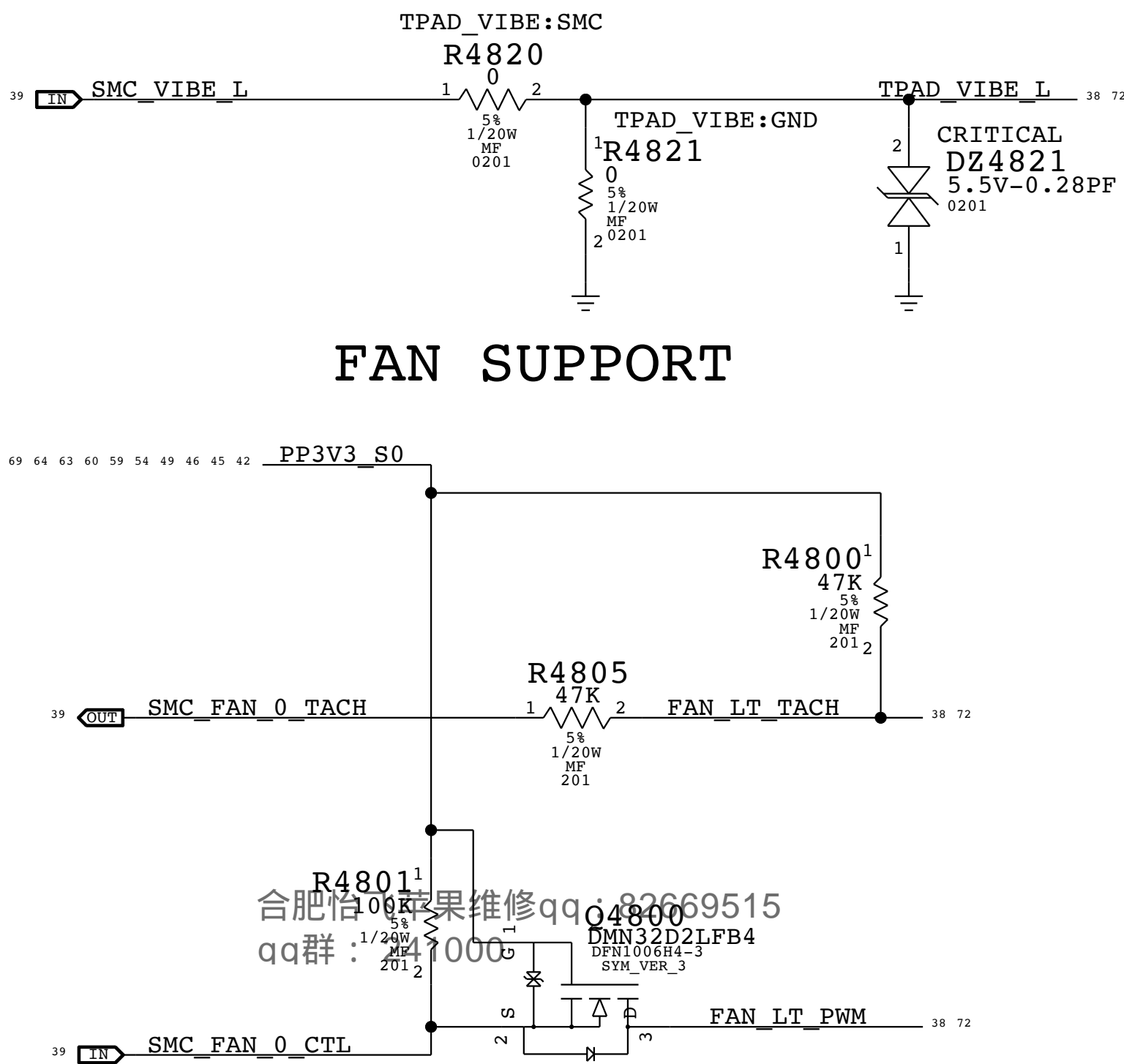
TPAD CONNECTOR



ESD DIODES

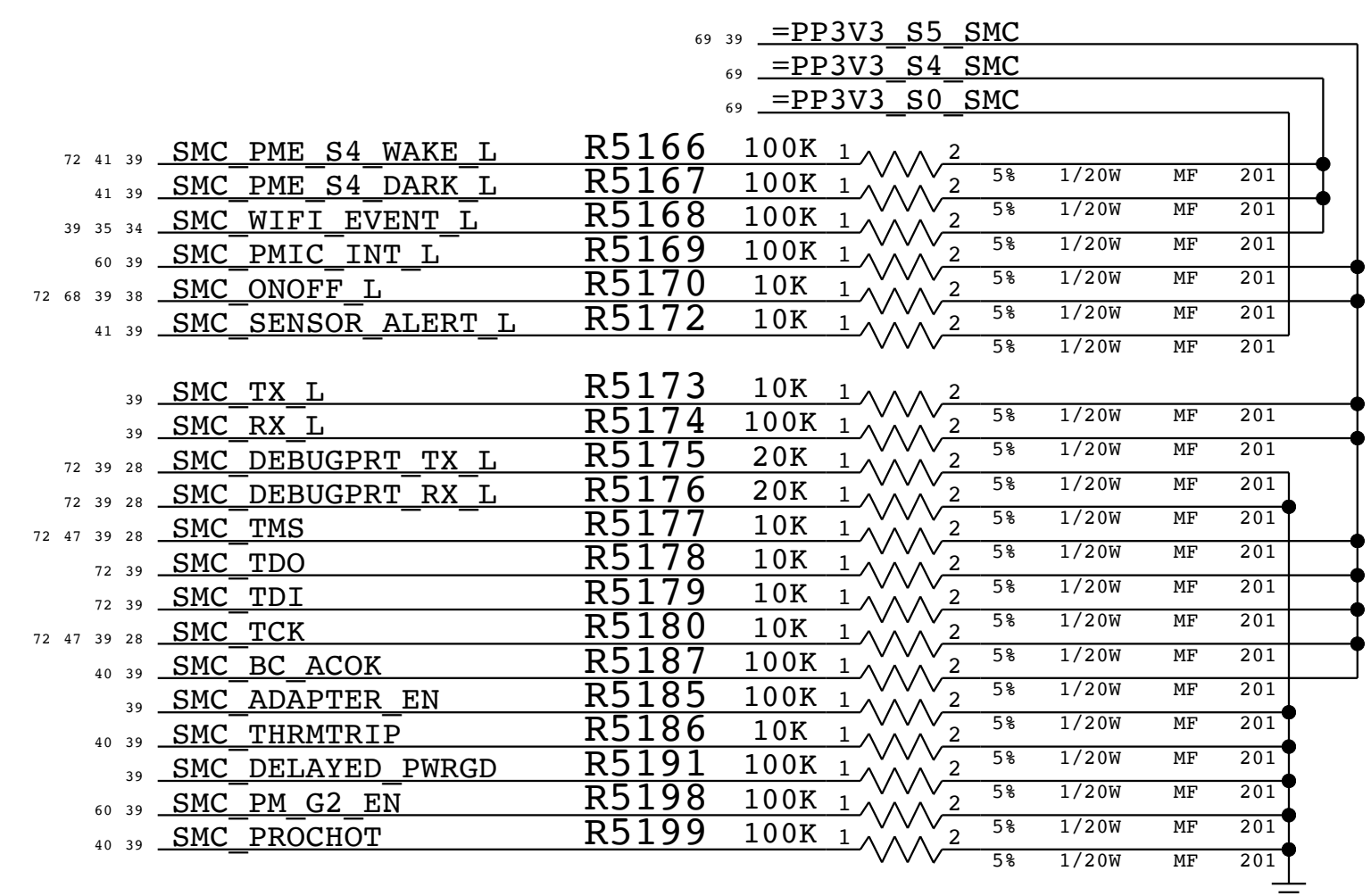
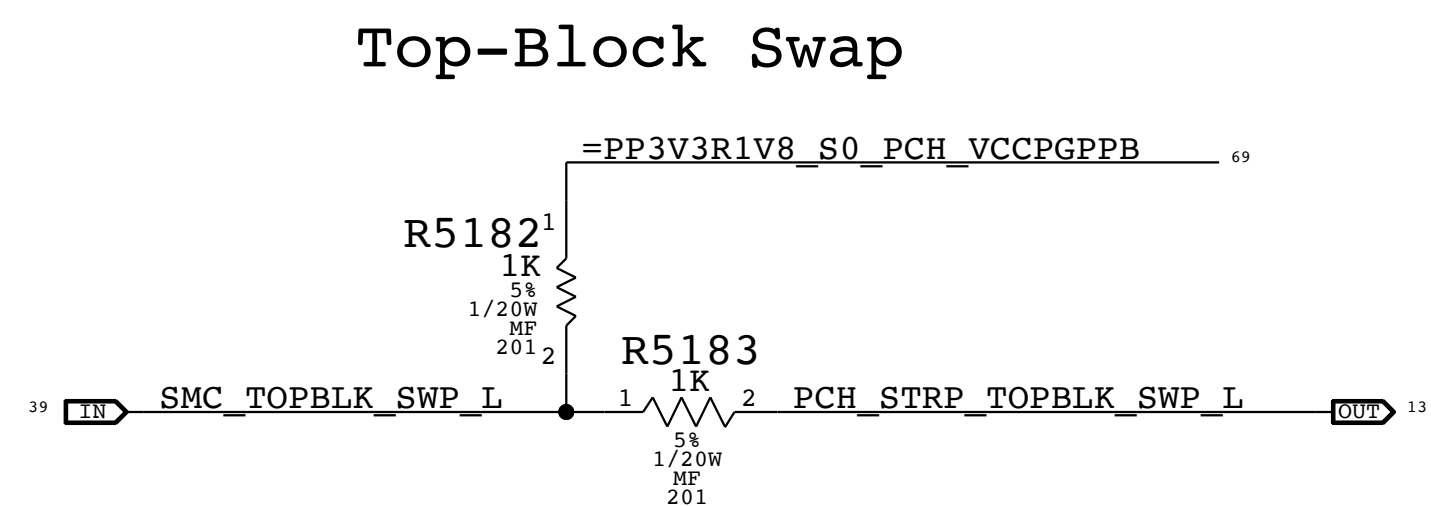
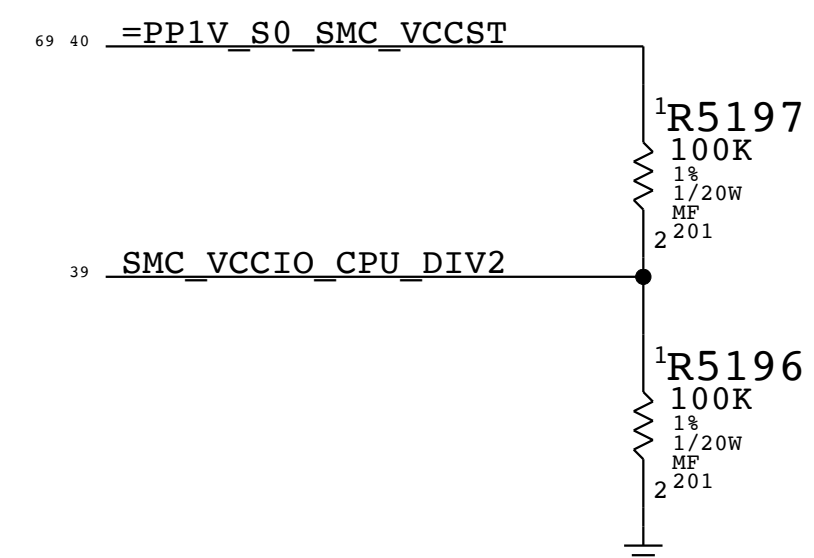
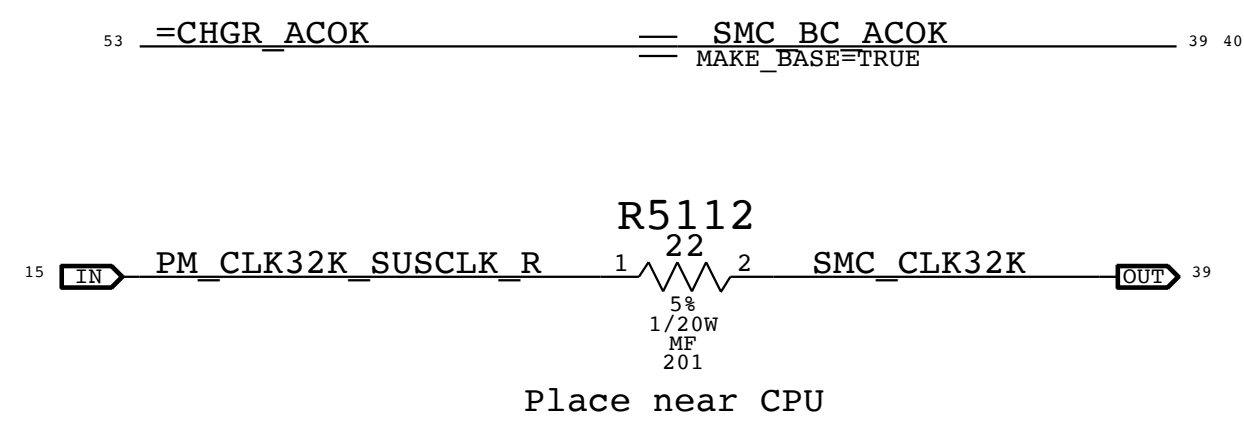
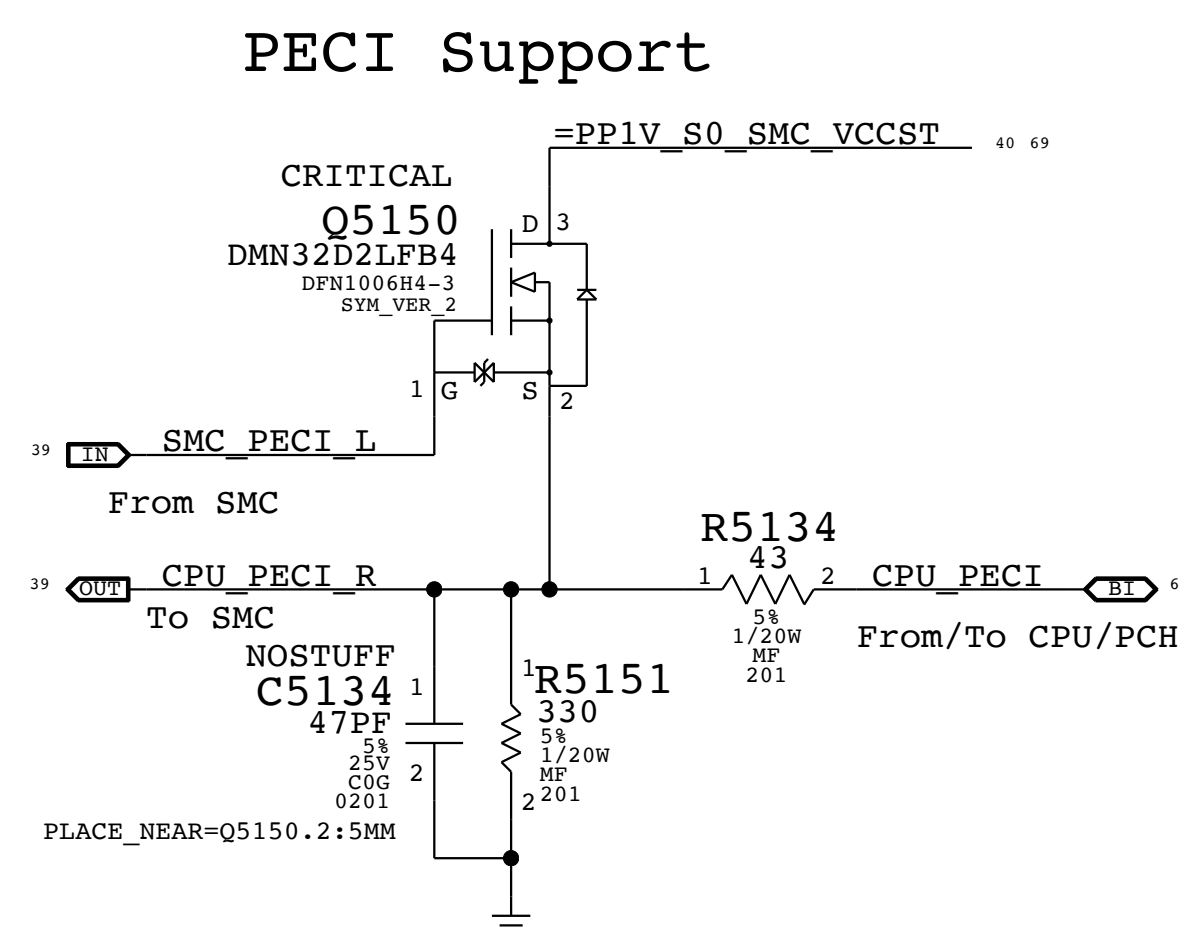
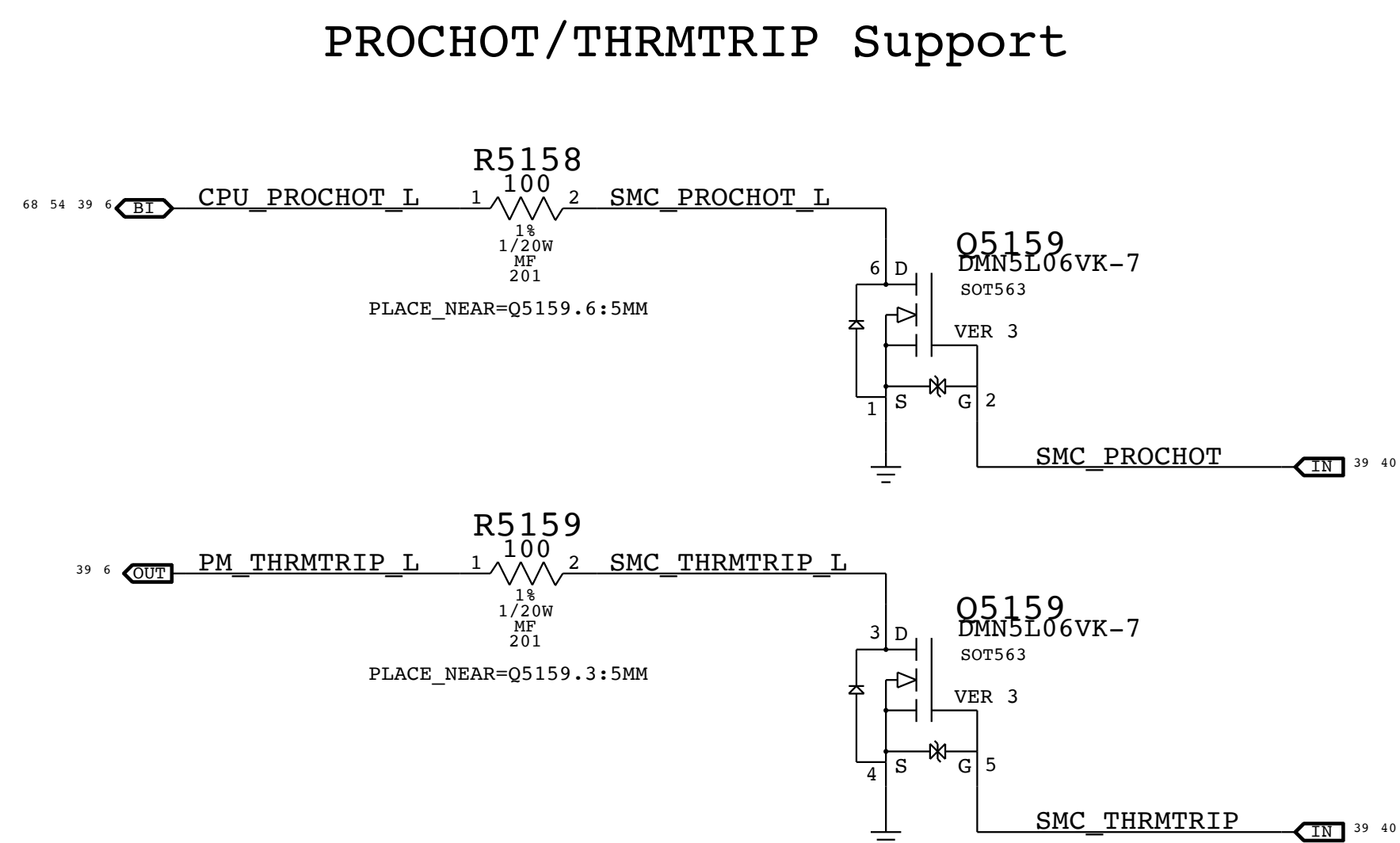
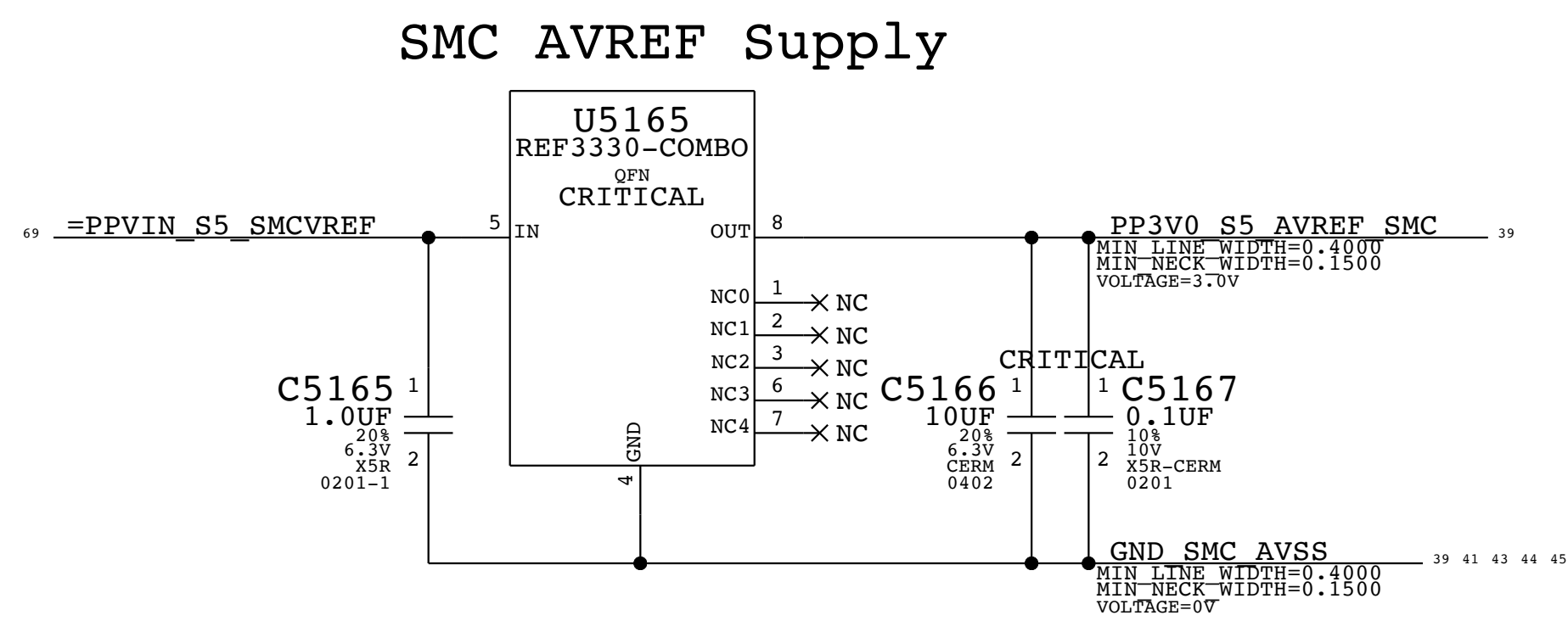


FAN SUPPORT




PAGE TITLE		
P1:KEYBOARD & TRACKPAD CONN		
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		38 OF 73

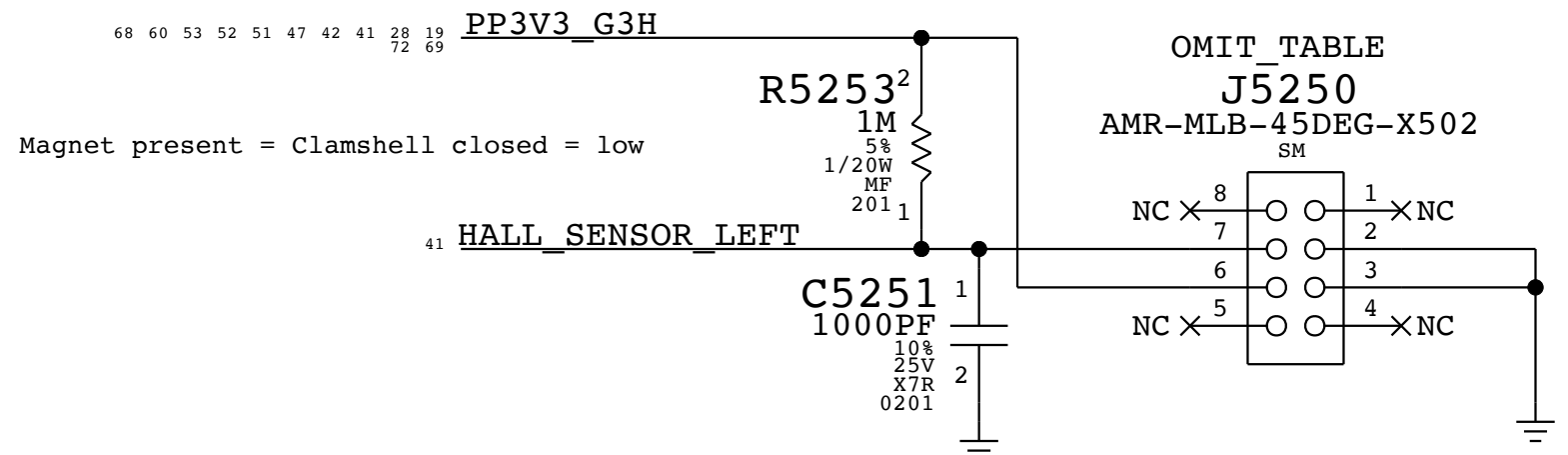
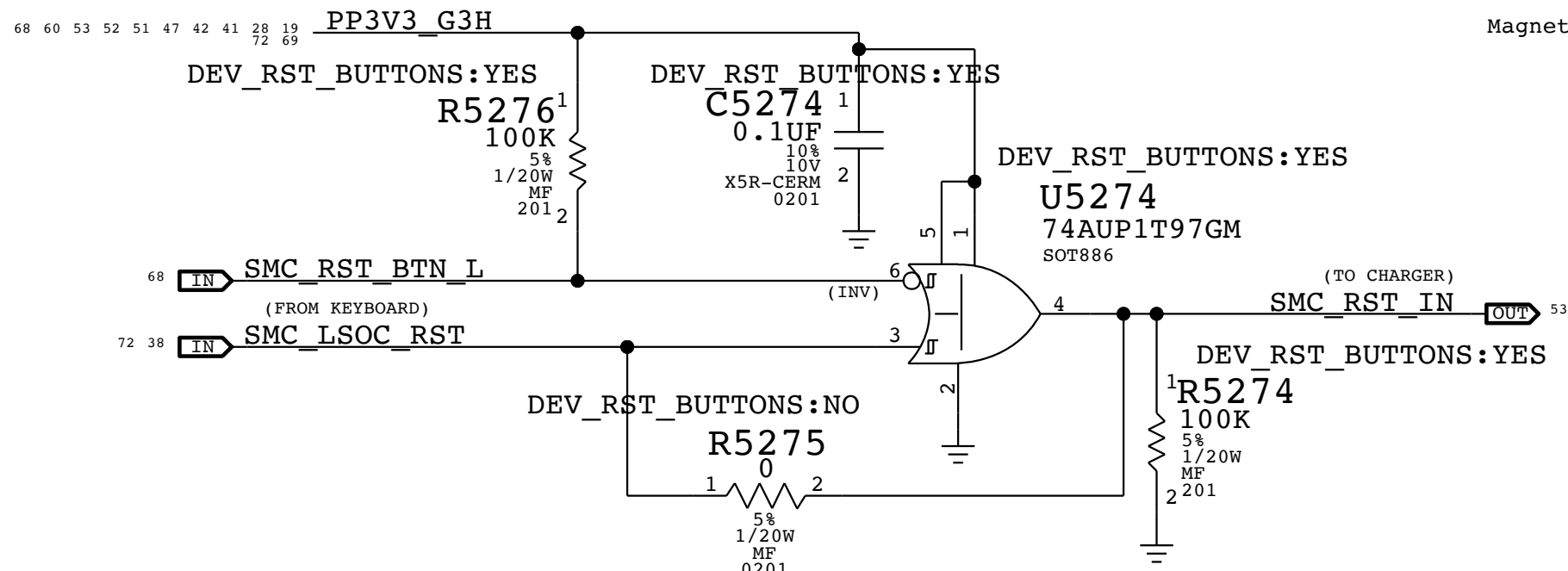
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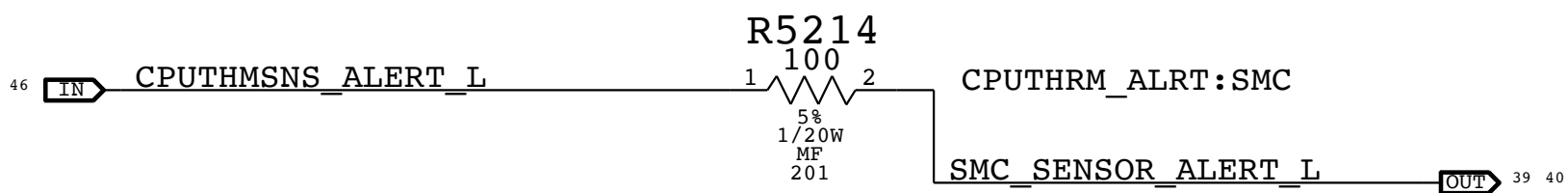
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qq群 : 241000

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AMR SENSOR PADS



Thermal Alerts



The diagram shows two signal traces, SMC_PME_S4_WAKE_L and SMC_PME_S4_DARK_L, with their respective inputs and timing parameters.

SMC_PME_S4_WAKE_L:

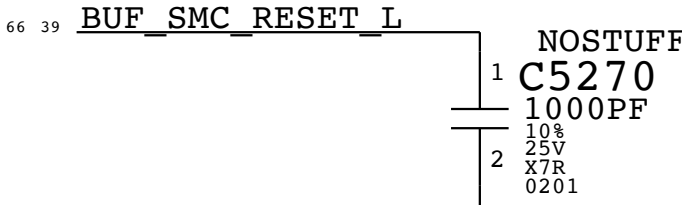
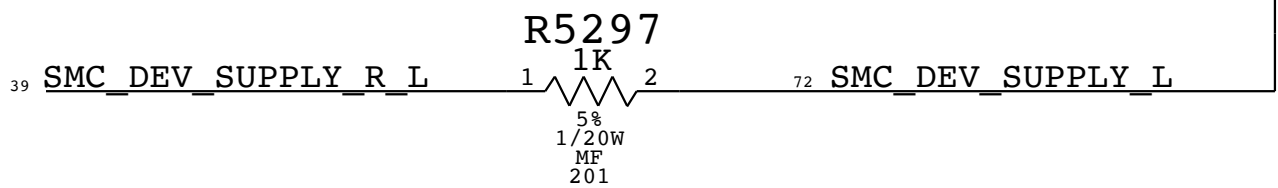
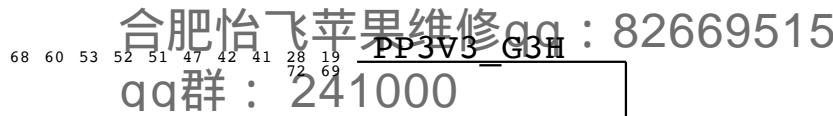
- Input: `TPAD_SMC_WAKE_L` (Signal 38)
- Output: `SMC_PME_S4_WAKE_L` (Signal 39)
- Timing: `MAKE_BASE=TRUE` (Signal 40)
- Delay: `OUTP` (Signal 42)


SMC_PME_S4_DARK_L:

- Inputs: `BT_WAKE_L` (Signal 34), `=UPC_WAKE_L` (Signal 29), and `TBT_WAKE_L` (Signal 26)
- Output: `SMC_PME_S4_DARK_L` (Signal 39)
- Timing: `MAKE_BASE=TRUE` (Signal 40)
- Delay: `OUTP` (Signal 40)

PM_PWRBTN_L:

- Input: `PM_PWRBTN_L` (Signal 17)
- Output: `PCH_PWRBTN_L` (Signal 14)
- Timing: `MAKE_BASE=TRUE` (Signal 14)
- Delay: `OUTP` (Signal 14)

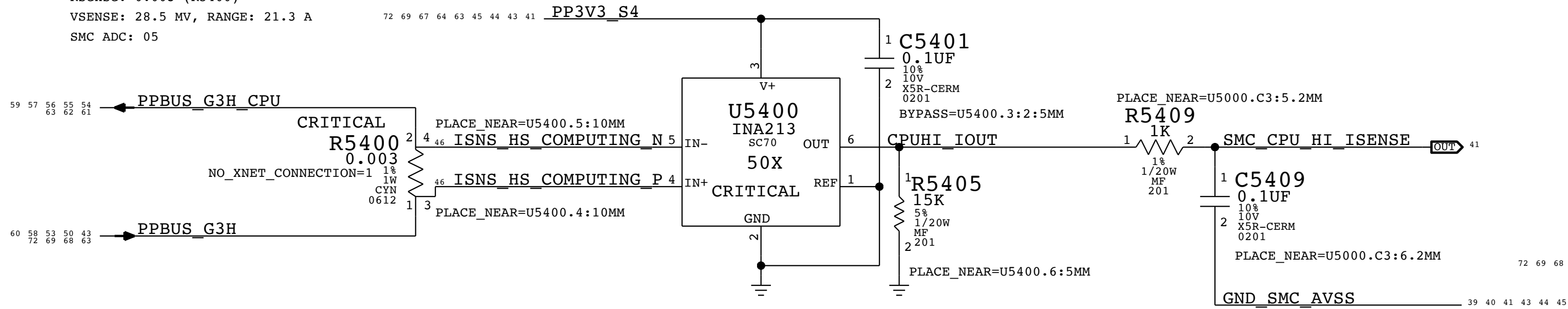


DESIGN: X502/MLB CATZ			
SYNC MASTER=PAULM			
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BOM_COST_GROUP=SMC

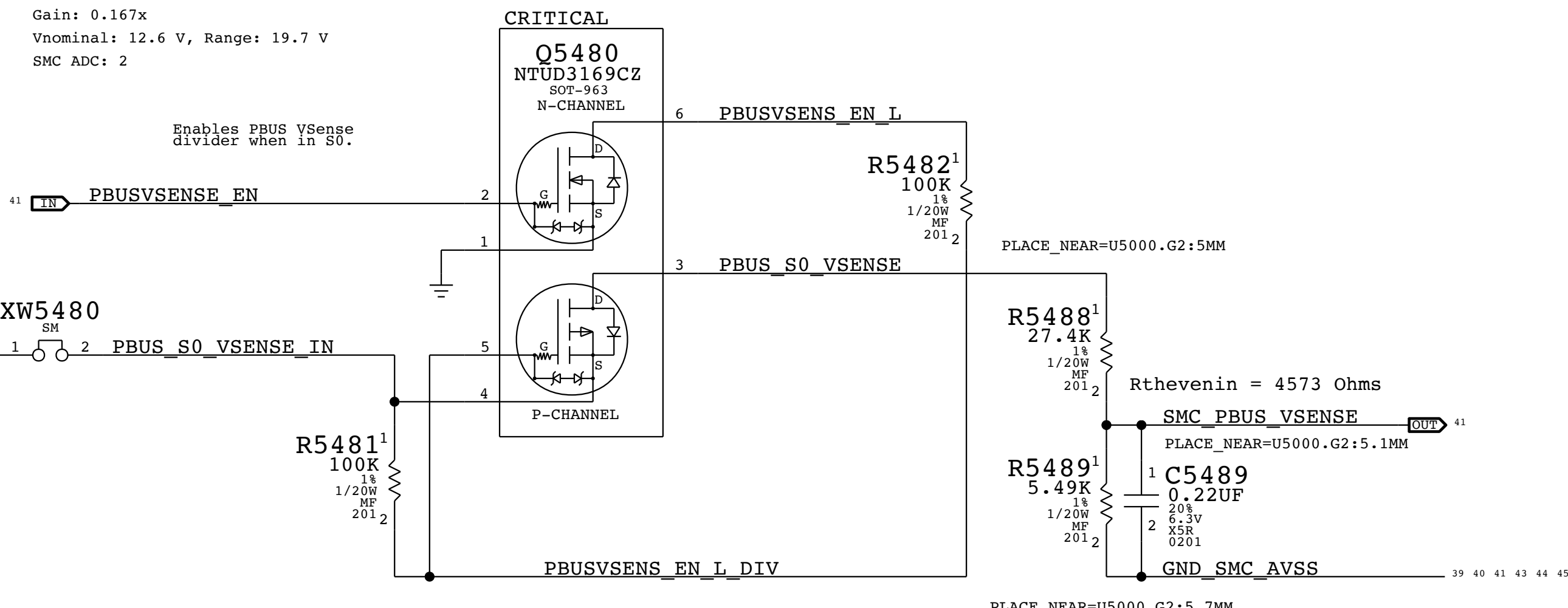
CPU High Side Current Sense (IC0R)

GAIN: 50X, EDP: 9.5 A
Rsense: 0.003 (R5400)
VSENSE: 28.5 MV, RANGE: 21.3 A
SMC ADC: 05



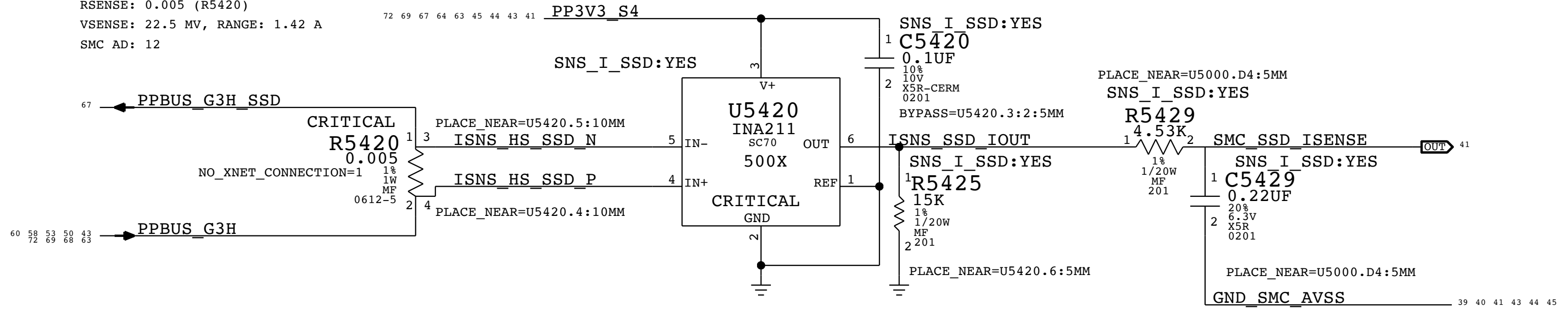
PBUS Voltage Sense & Enable (VP0R)

Gain: 0.167x
Vnominal: 12.6 V, Range: 19.7 V
SMC ADC: 2



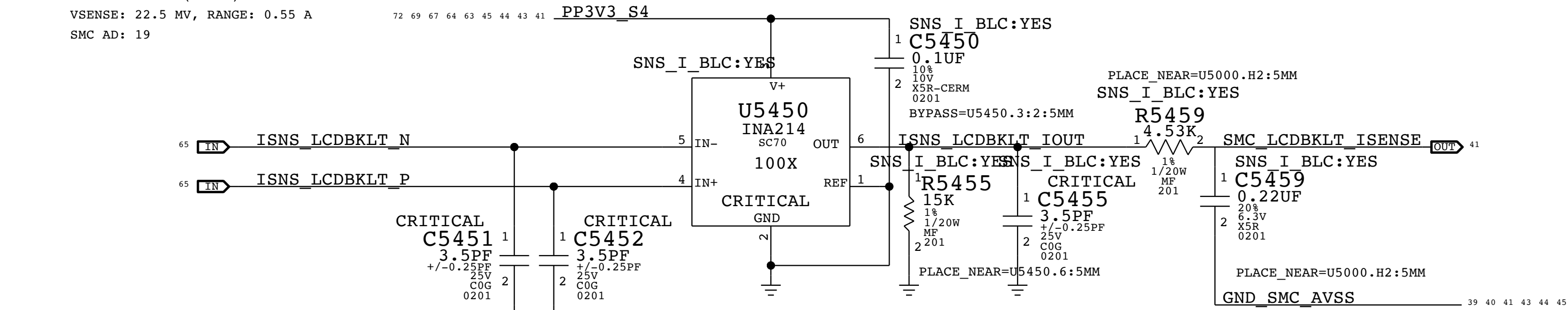
SSD NAND CURRENT SENSE (IHNC)

GAIN: 500X, EDP: 0.9 A
RSense: 0.005 (R5420)
VSENSE: 22.5 MV, RANGE: 1.42 A
SMC AD: 12



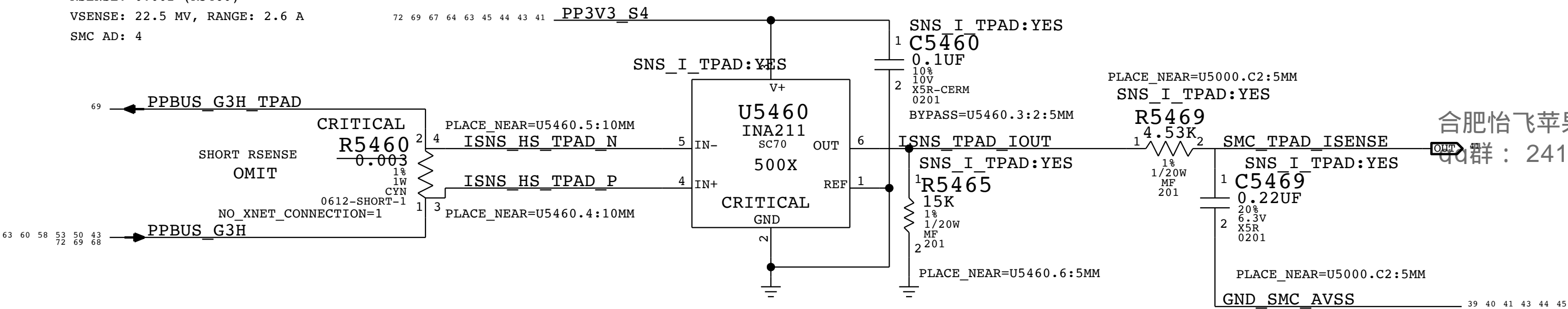
LCD BACKLIGHT CURRENT SENSE (IBLR)

GAIN: 100X, EDP: 0.9 A
Rsense: 0.025 (R7700)
VSENSE: 22.5 MV, RANGE: 0.55 A
SMC AD: 19



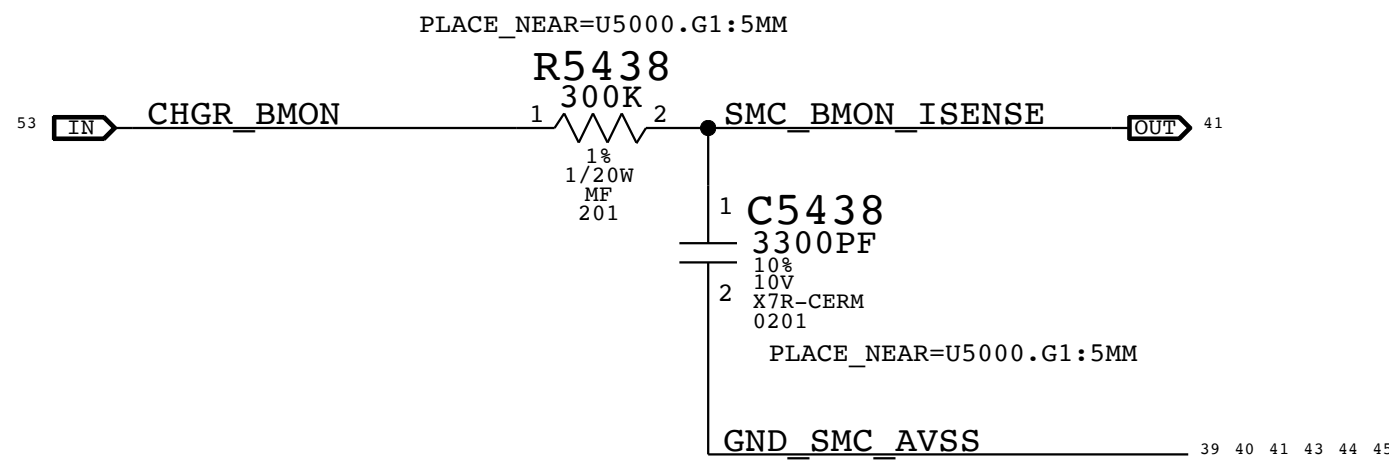
TRACKPAD ACTUATOR X239 CURRENT SENSE (ITAR)

GAIN: 200X, EDP: 0.9 A
RSense: 0.002 (R5460)
VSENSE: 22.5 MV, RANGE: 2.6 A
SMC AD: 4



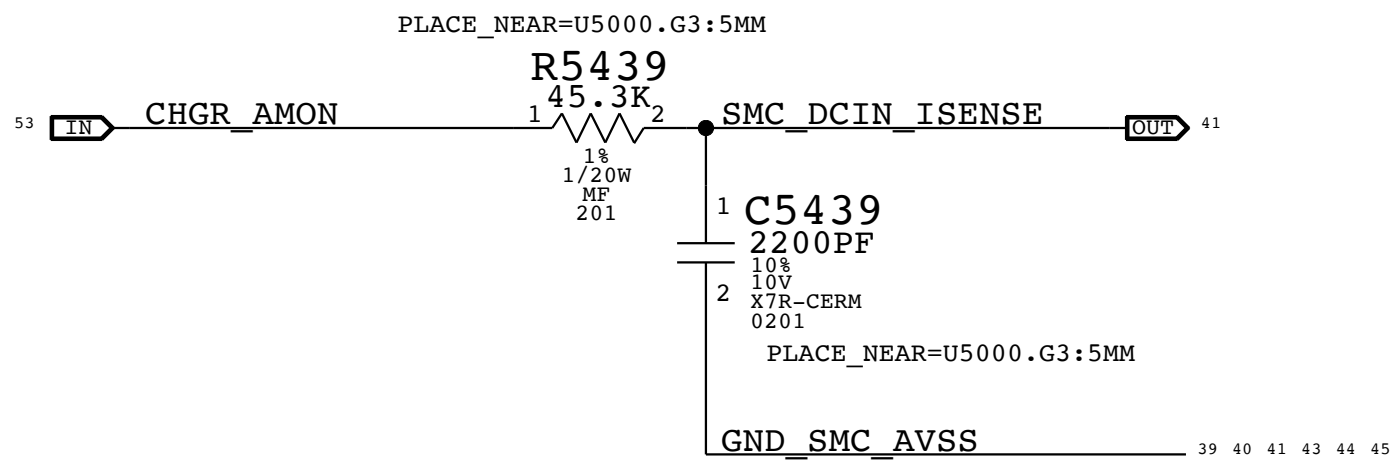
Charger (BMON) Current Sense (IPBR)

Charger Gain: 36x, EDP: 8 A
RSense: 0.005 (R7160)
SMC ADC: 03



DC-IN (AMON) Current Sense (ID0R)

Charger Gain: 20x, EDP: 4.6 A
RSense: 0.010 (R7120)
SMC ADC: 01



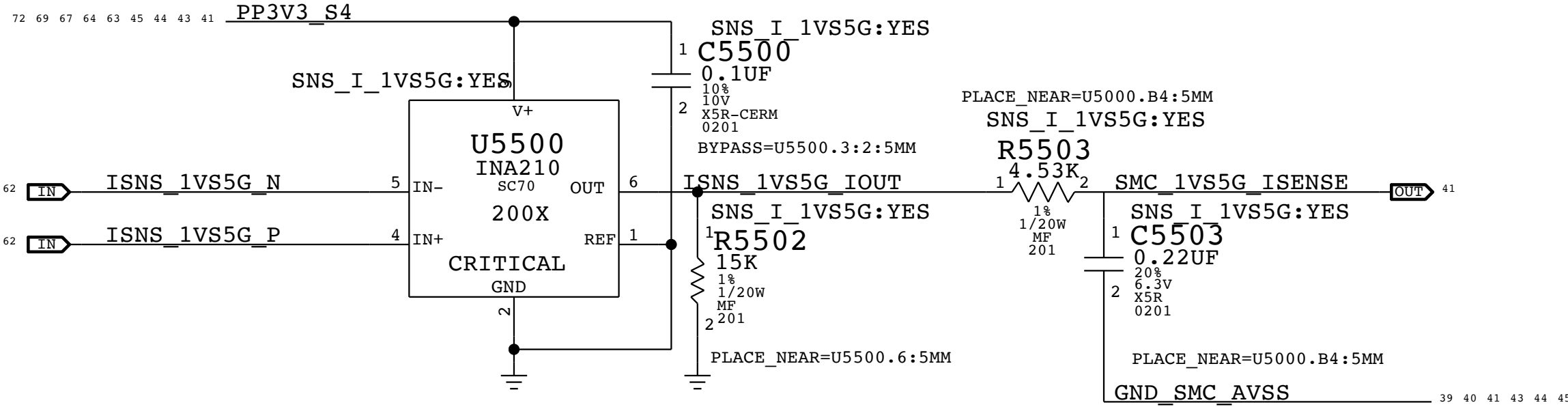
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5429		SNS_I_SSD:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5459		SNS_I_BLC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5469		SNS_I_TPAD:NO

DESIGN: X502/MLB CATZ		
LAST CHANGE: Thu Aug 4 21:00:42 2016		
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Power Sensors High Side		
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BOM_COST_GROUP=SENSORS

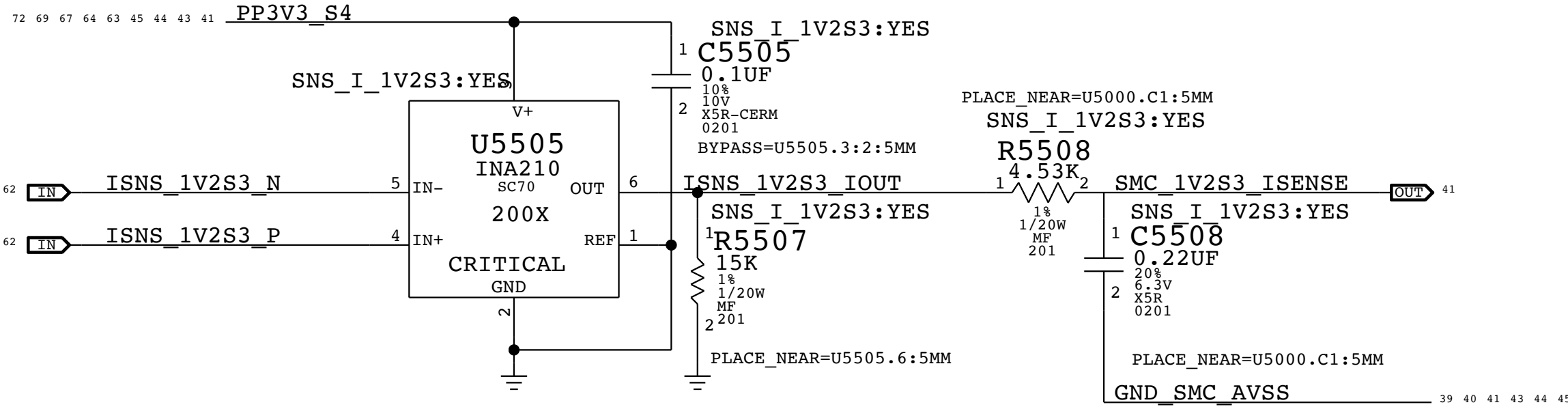
1V_S5G CURRENT SENSE (ISIC)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.003 (R7700)
VSENSE: 22.5 MV, RANGE: 3.0 A
SMC AD: 11



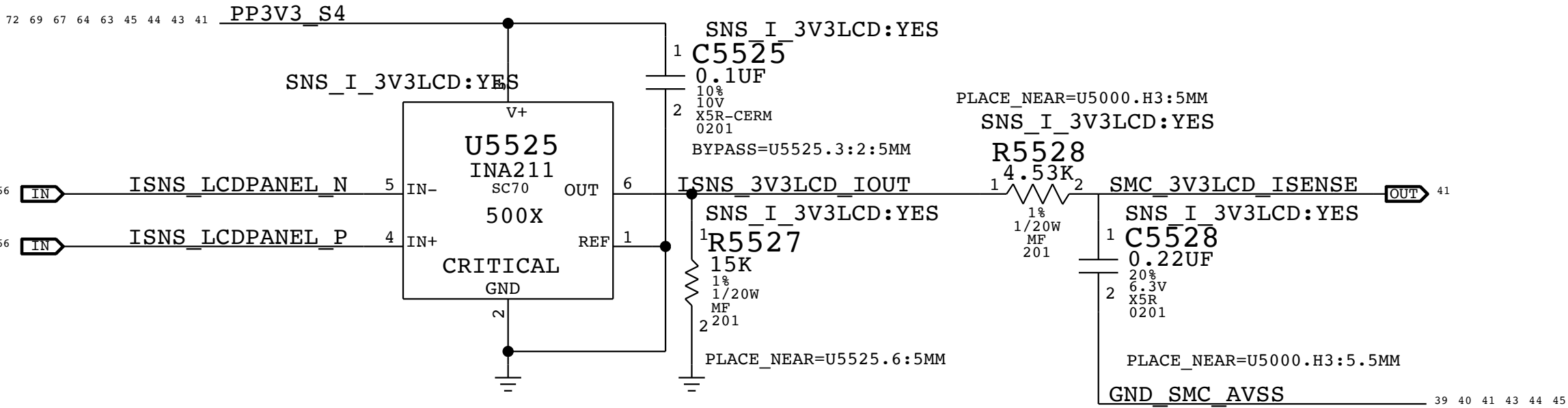
1V2_S3 CURRENT SENSE (IMOC)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.002 (R7700)
VSENSE: 22.5 MV, RANGE: 7.67 A
SMC AD: 14



3V3_S0 LCD CURRENT SENSE (ILDC)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.005 (R5525)
VSENSE: 22.5 MV, RANGE: 1.6 A
SMC AD: 17

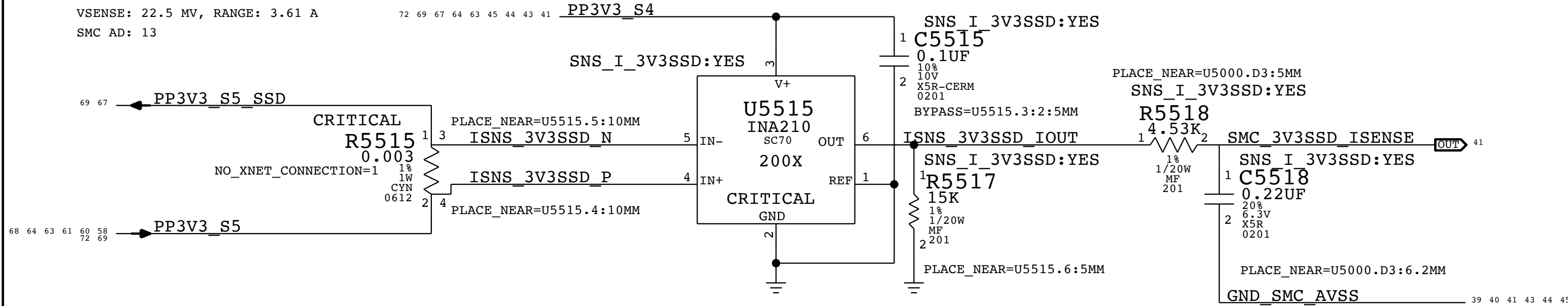


5V_S0 LCD CURRENT SENSE (I____)

GAIN: 500X. EDP: 0.9 A
RSENSE: 0.005 (R8520)
VSENSE: 22.5 MV, RANGE: 1.6 A
SMC AD: 17

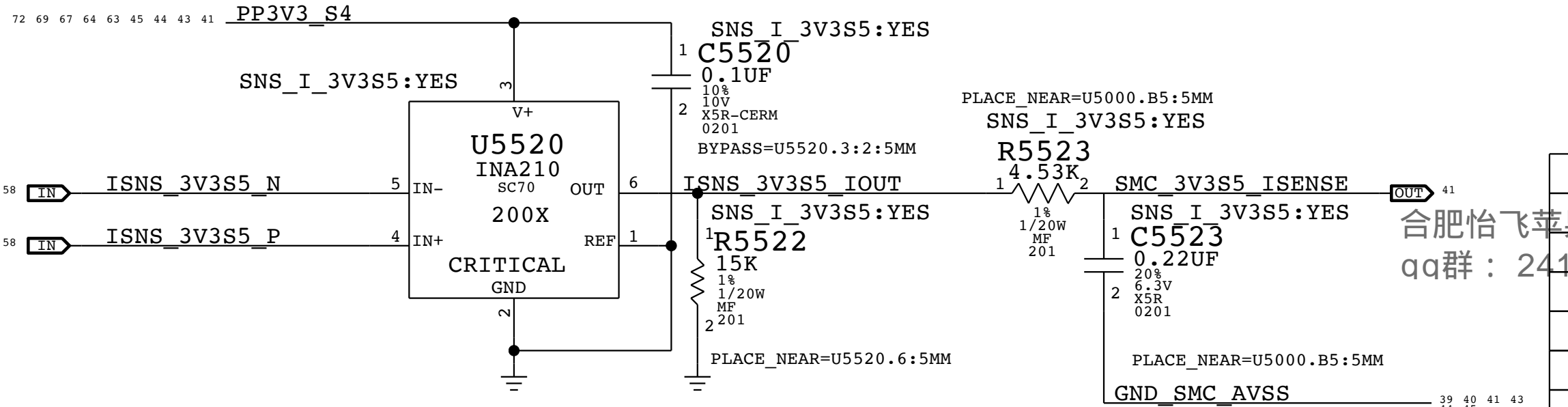
3V3_SSD CURRENT SENSE (IHCC)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.003 (R5515)
VSENSE: 22.5 MV, RANGE: 3.61 A
SMC AD: 13



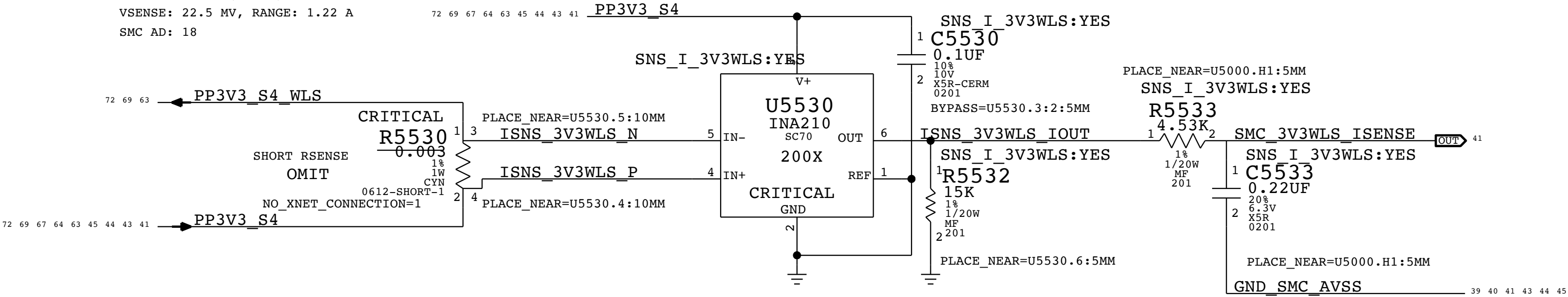
3V3_S5 CURRENT SENSE (IO3R)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.003 (R7710)
VSENSE: 22.5 MV ?, RANGE: 4 A
SMC AD: 22



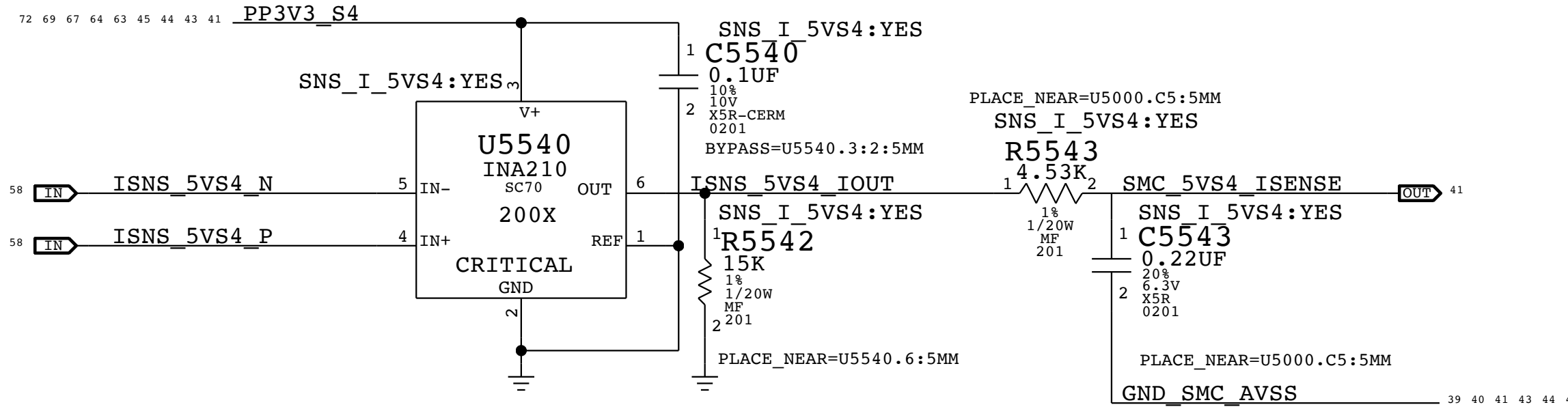
3V3_S4 WIRELESS CURRENT SENSE (IAPC)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.010 (R7700)
VSENSE: 22.5 MV, RANGE: 1.22 A
SMC AD: 18



5V_S4 CURRENT SENSE (IO5R)

GAIN: 200X. EDP: ?? A
RSENSE: 0.003 (R7900)
VSENSE: 22.5 MV ?, RANGE: 6.8 A
SMC AD: 21



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5503		SNS_I_1VS5G:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5508		SNS_I_1V2S3:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5518		SNS_I_3V3SSD:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5523		SNS_I_3V3S5:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5528		SNS_I_3V3LCD:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5533		SNS_I_3V3WLS:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5543		SNS_I_5VS4:NO

DESIGN: X502/MLB CATZ		
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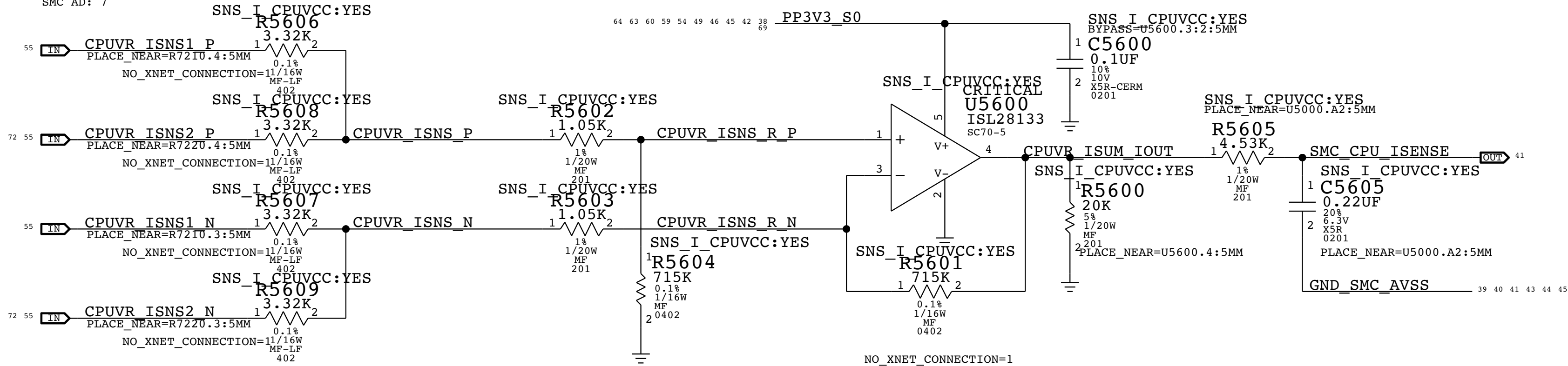
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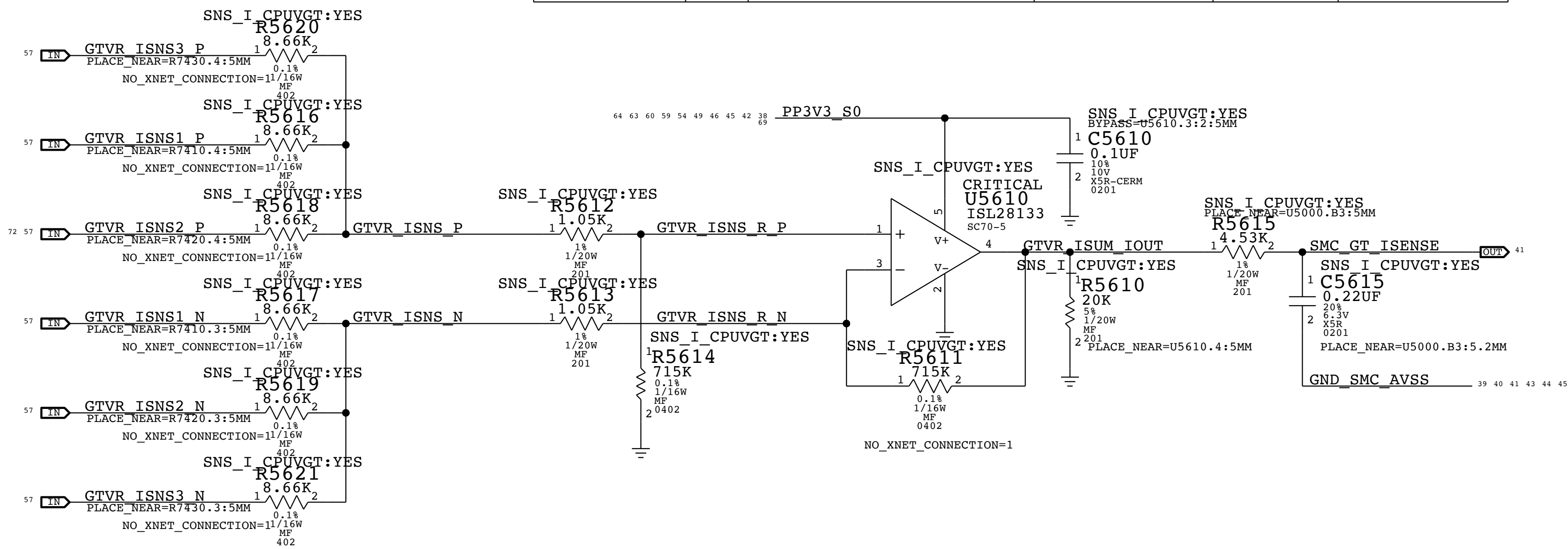
CPU VCC CURRENT SENSE (ICAC)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.005 (R7700)
VSENSE: 22.5 MV, RANGE: 2.27 A
SMC AD: 7



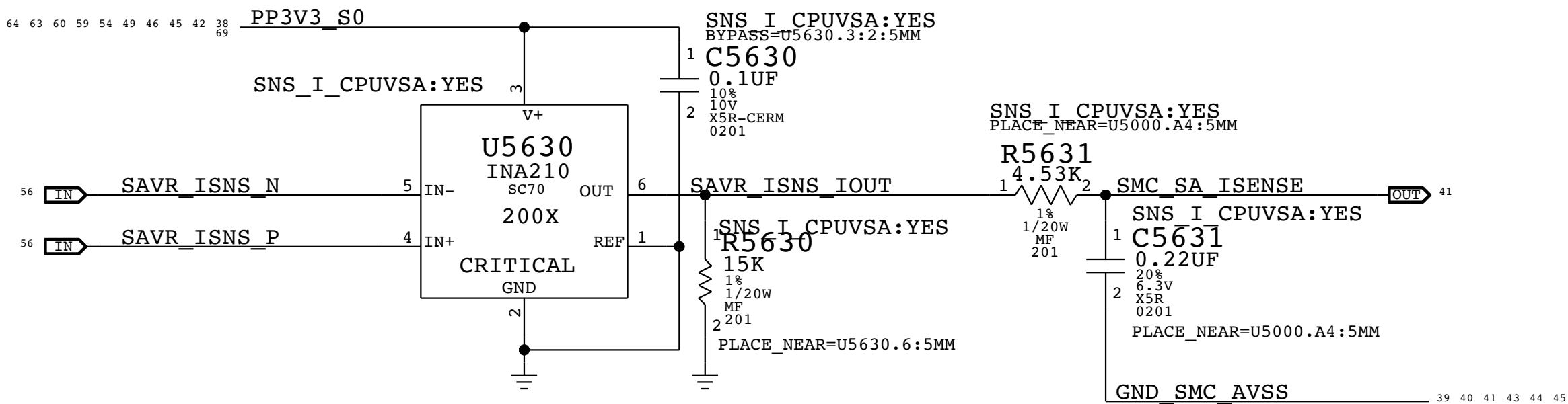
CPU GT CURRENT SENSE (ICGC)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.005 (R7700)
VSENSE: 22.5 MV, RANGE: 2.27 A
SMC AD: 9



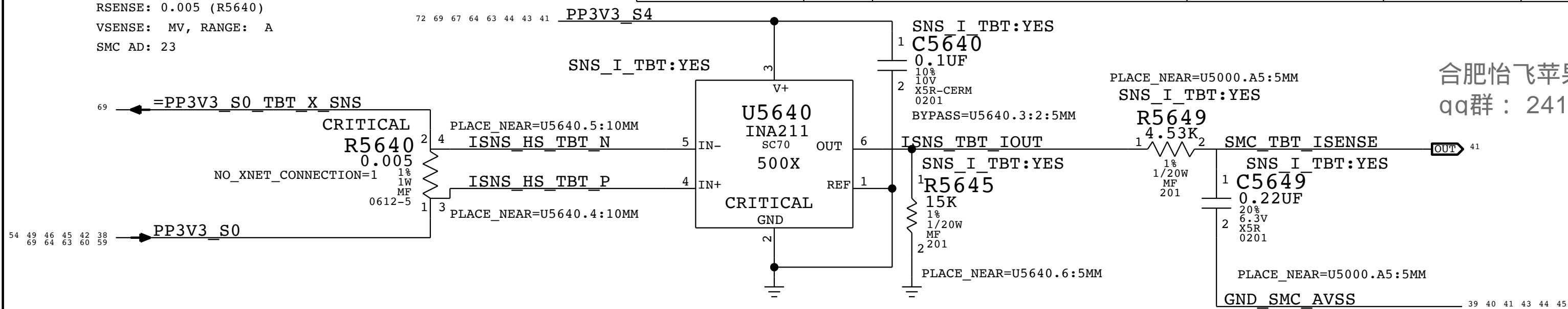
CPU SA CURRENT SENSE (ICSC)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.002 (R7700)
VSENSE: 22.5 MV, RANGE: 7.67 A
SMC AD: 10



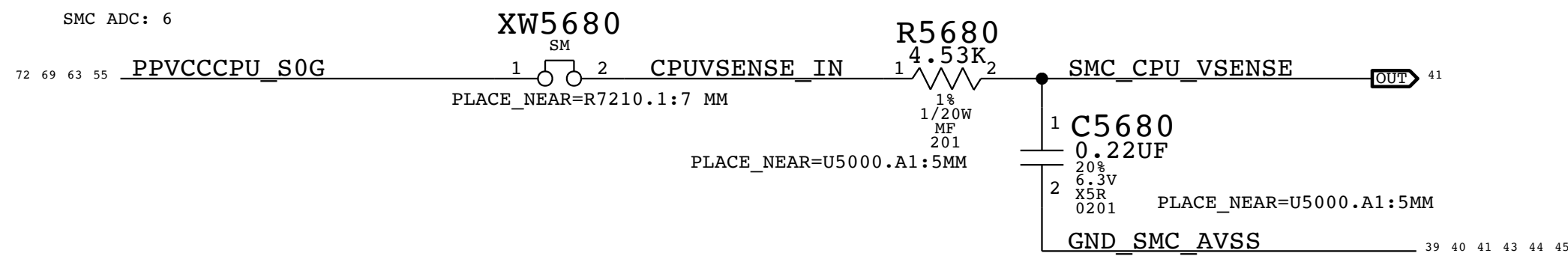
TBT CURRENT SENSE (IULC)

GAIN: 500X. EDP: A
RSENSE: 0.005 (R5640)
VSENSE: MV, RANGE: A
SMC AD: 23



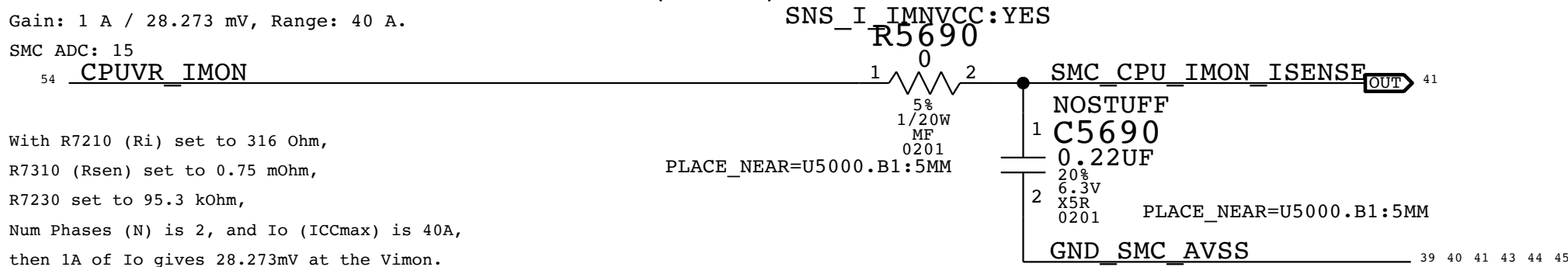
CPU CORE VOLTAGE SENSE (VCAC)

SMC ADC: 6



CPU CORE IMON CURRENT SENSE (ICAM)

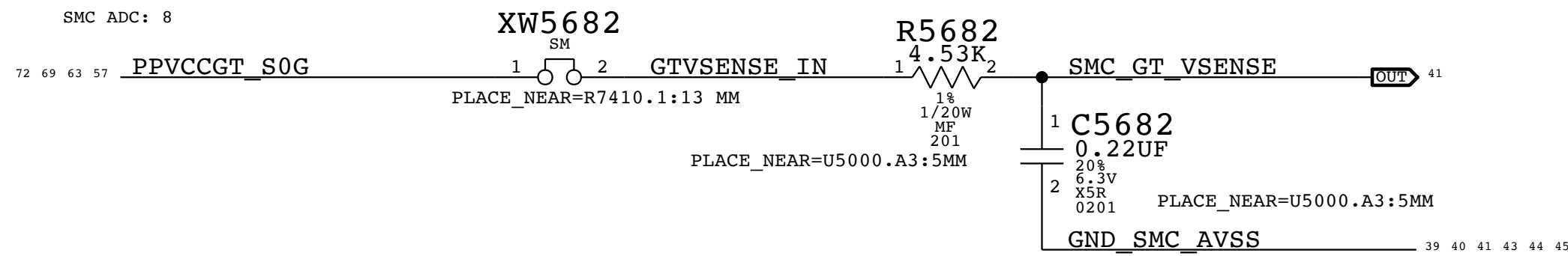
Gain: 1 A / 28.273 mV, Range: 40 A.
SMC ADC: 15



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5605		SNS_I_CPUVCC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5615		SNS_I_CPUVGT:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5631		SNS_I_CPUVSA:NO

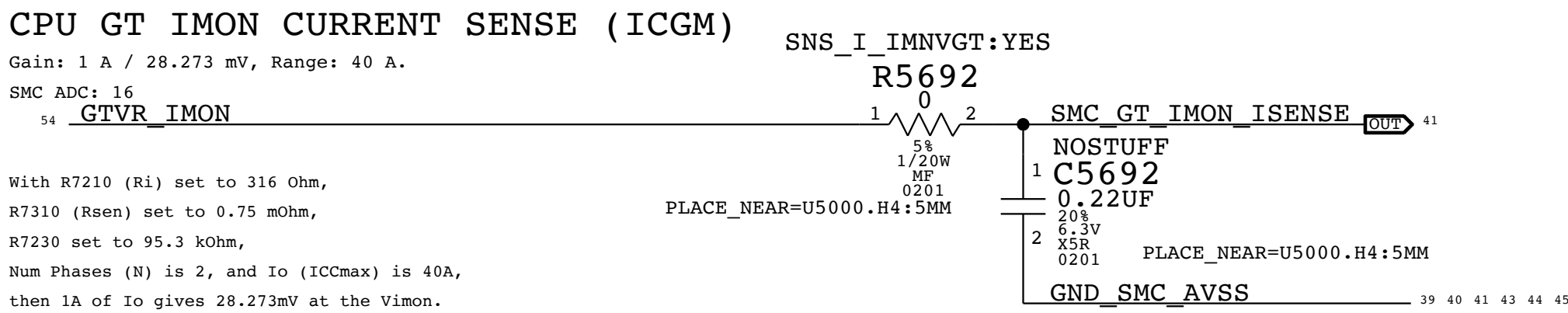
CPU GT VOLTAGE SENSE (VCGC)

SMC ADC: 8



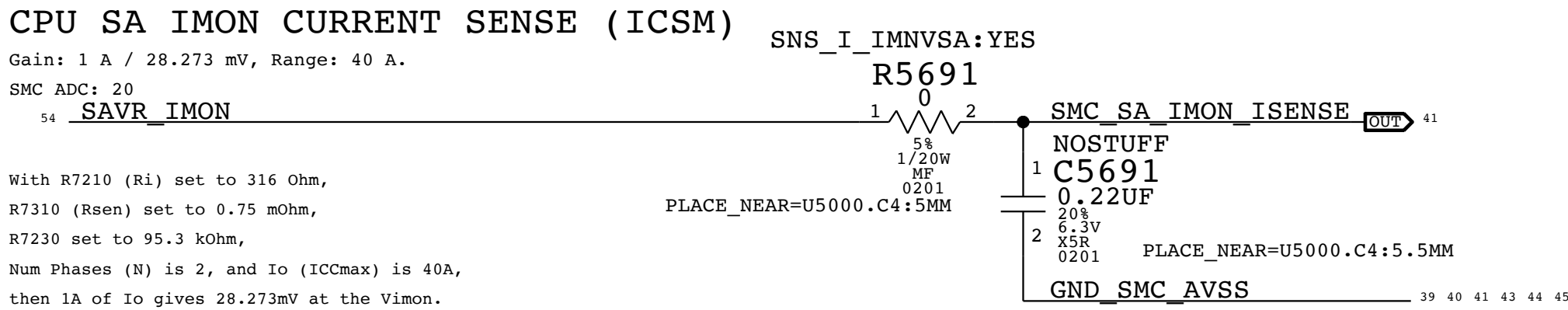
CPU GT IMON CURRENT SENSE (ICGM)

Gain: 1 A / 28.273 mV, Range: 40 A.
SMC ADC: 16



CPU SA IMON CURRENT SENSE (ICSM)

Gain: 1 A / 28.273 mV, Range: 40 A.
SMC ADC: 20



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5649		SNS_I_TBT:NO

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BOM_COST_GROUP=SENSORS

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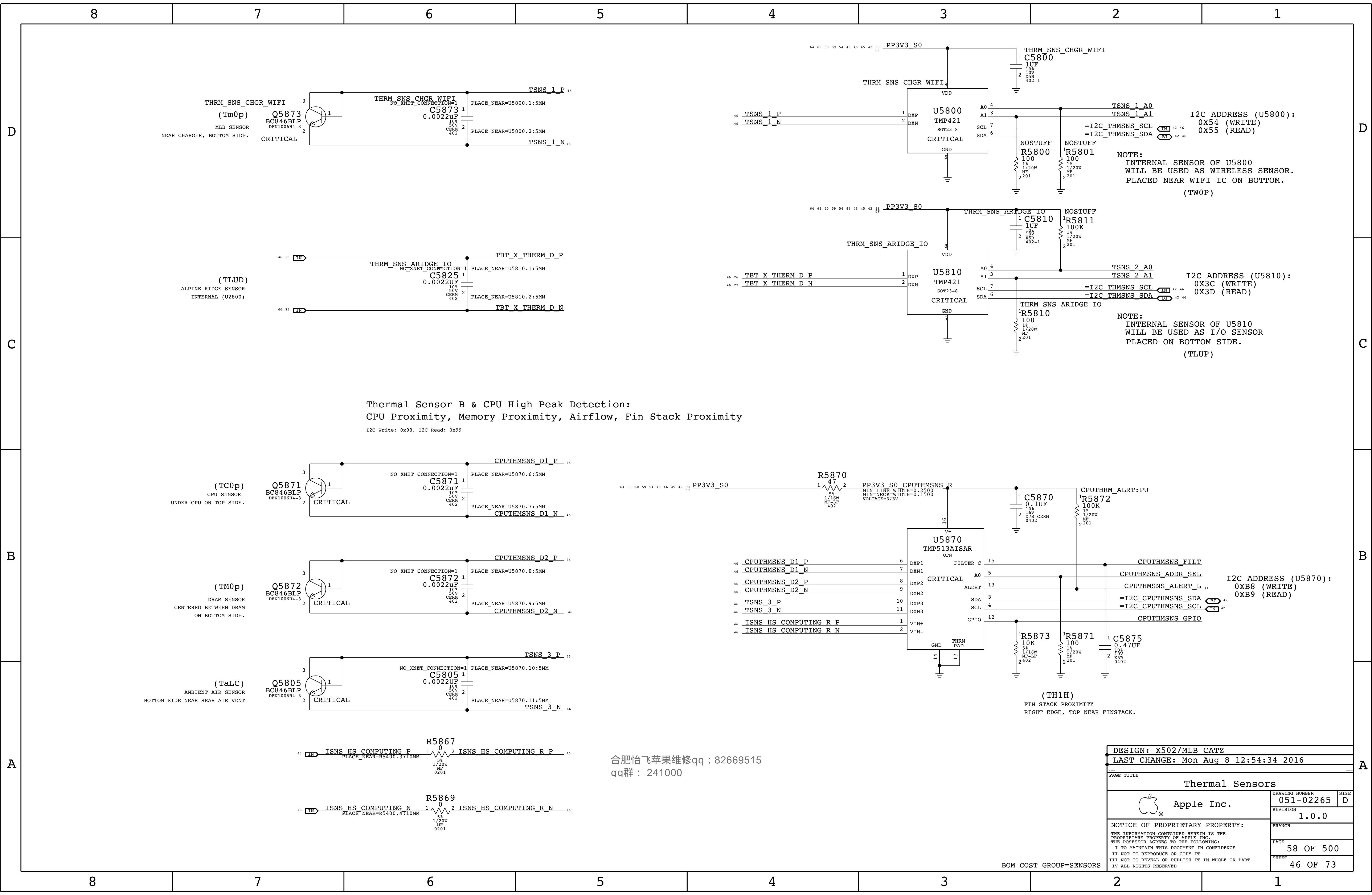
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D

C

B

A

D

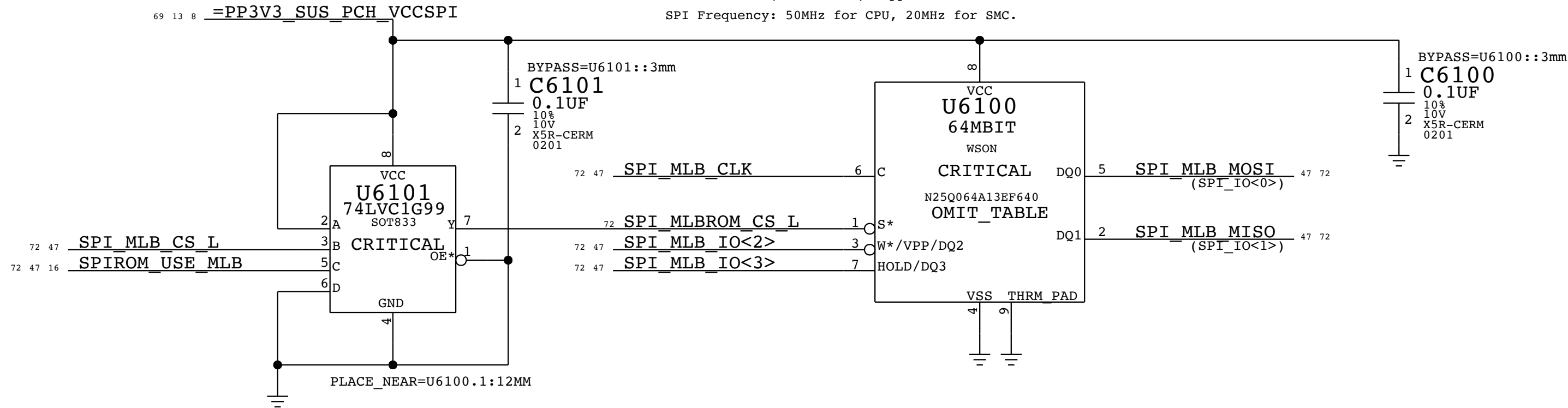
C

B

A

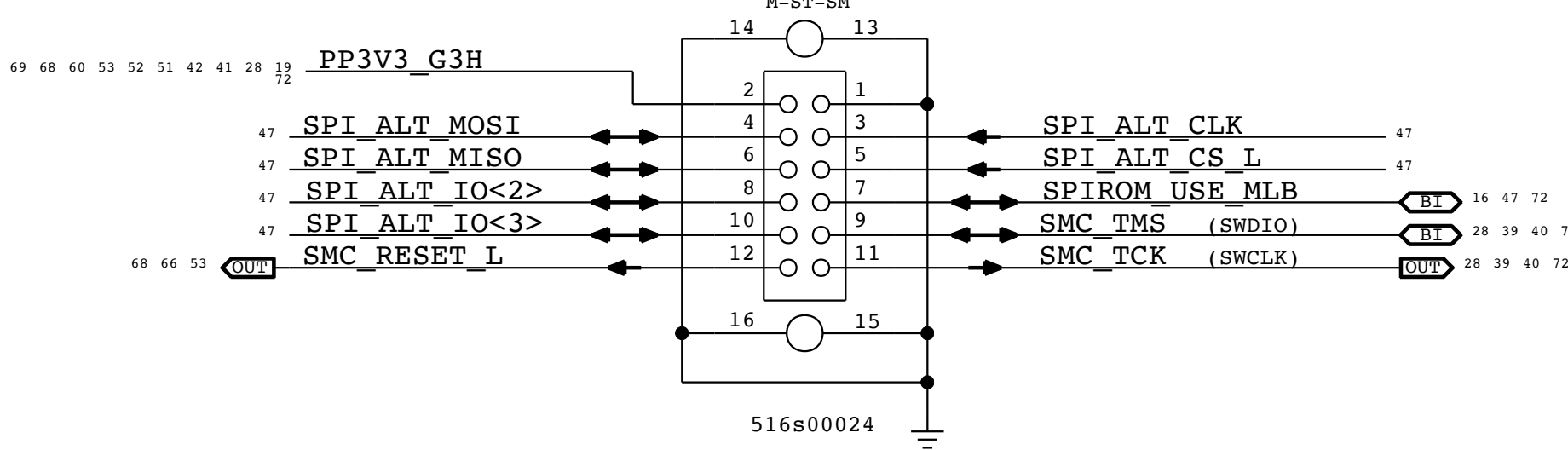
SPI ROM - Combo BGA Footprint (3 vendors)

Quad-IO Mode (Mode 0 & 3) supported.
SPI Frequency: 50MHz for CPU, 20MHz for SMC.



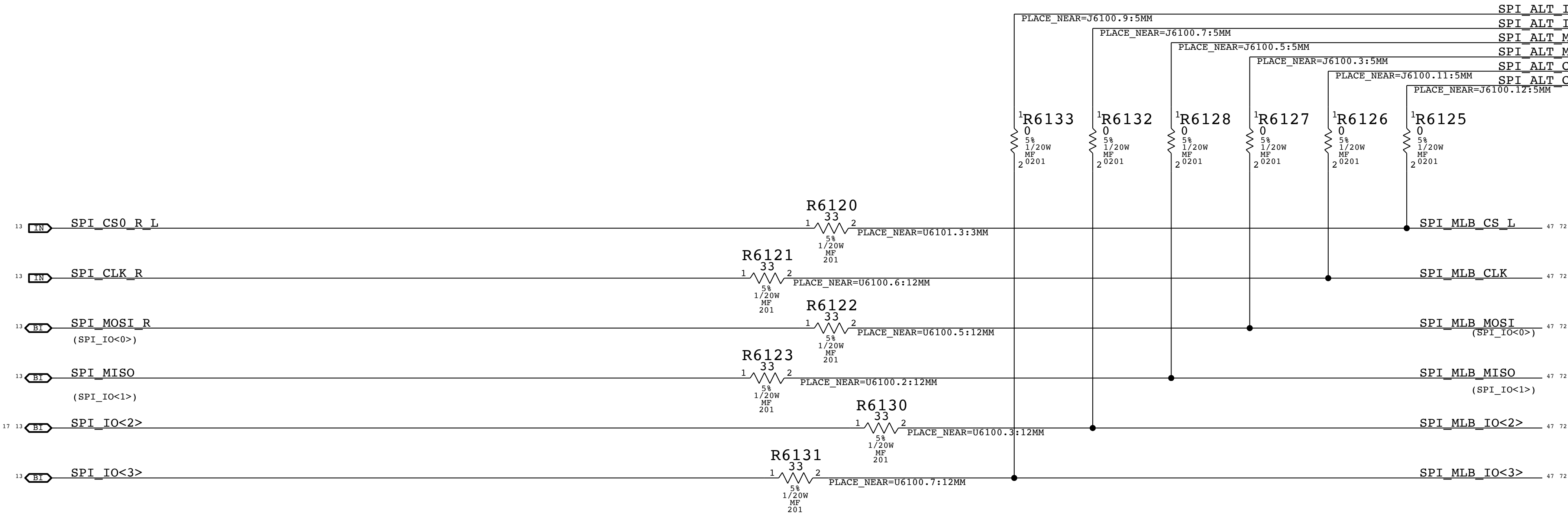
SPI+SWD SAM Connector

CRITICAL
J6100
DF40PC-12DP-0.4V-51
M-SW-SW



BootROM SPI Bus Series Termination

CPU Master




Sam Card ROM Slave

SPI ROM Slave

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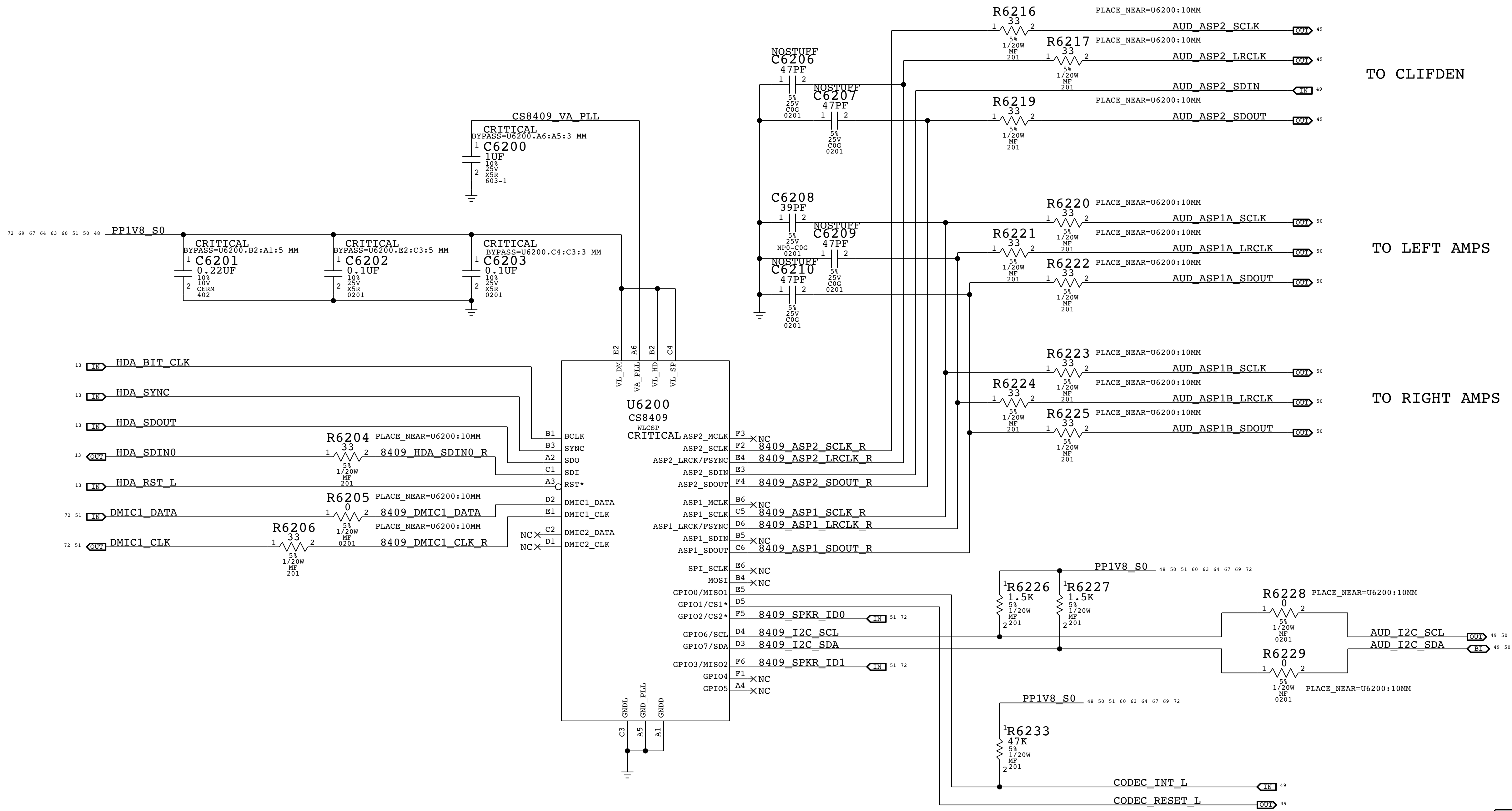
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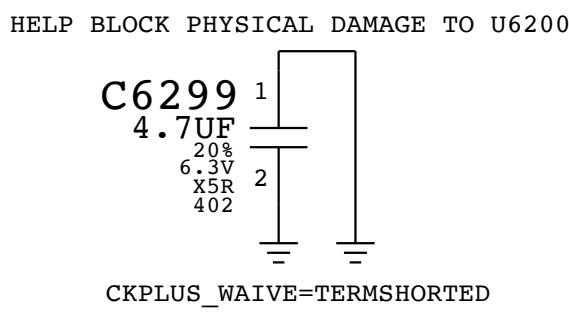
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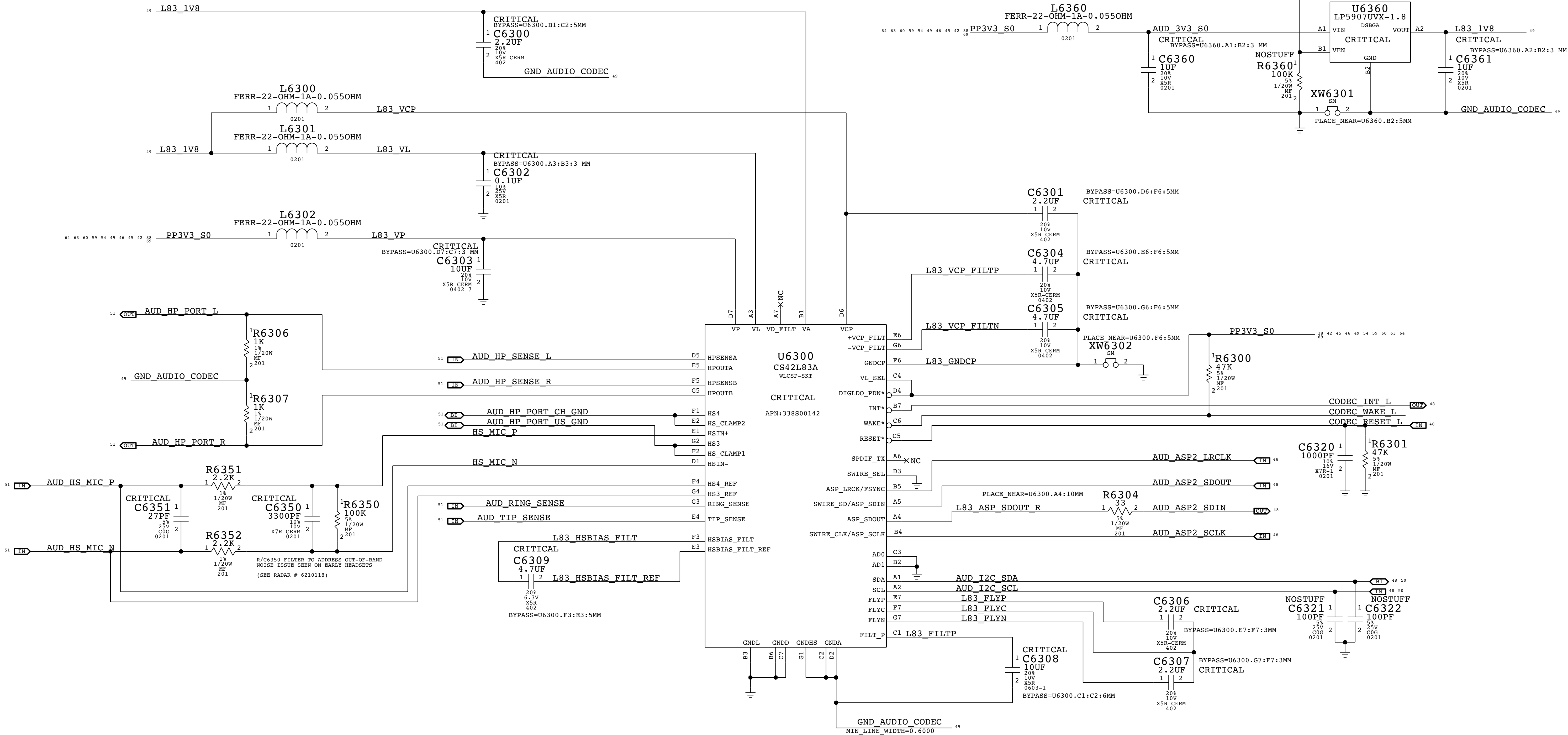
合肥怡飞苹果维修qq : 82669515
qq群 : 241000



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AD1 AD0 I2C ADDR
GND GND 0X48 <--
GND 1.8V 0X49
1.8V GND 0X4A
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4X MONO SPEAKER AMPLIFIERS

APN: 353S00685
GAIN: 0DBFS = 7VRMS

FRONT LEFT AMPLIFIER

FRONT RIGHT AMPLIFIER

REAR LEFT AMPLIFIER

REAR RIGHT AMPLIFIER

LEFT BULK CAPACITANCE

RIGHT BULK CAPACITANCE

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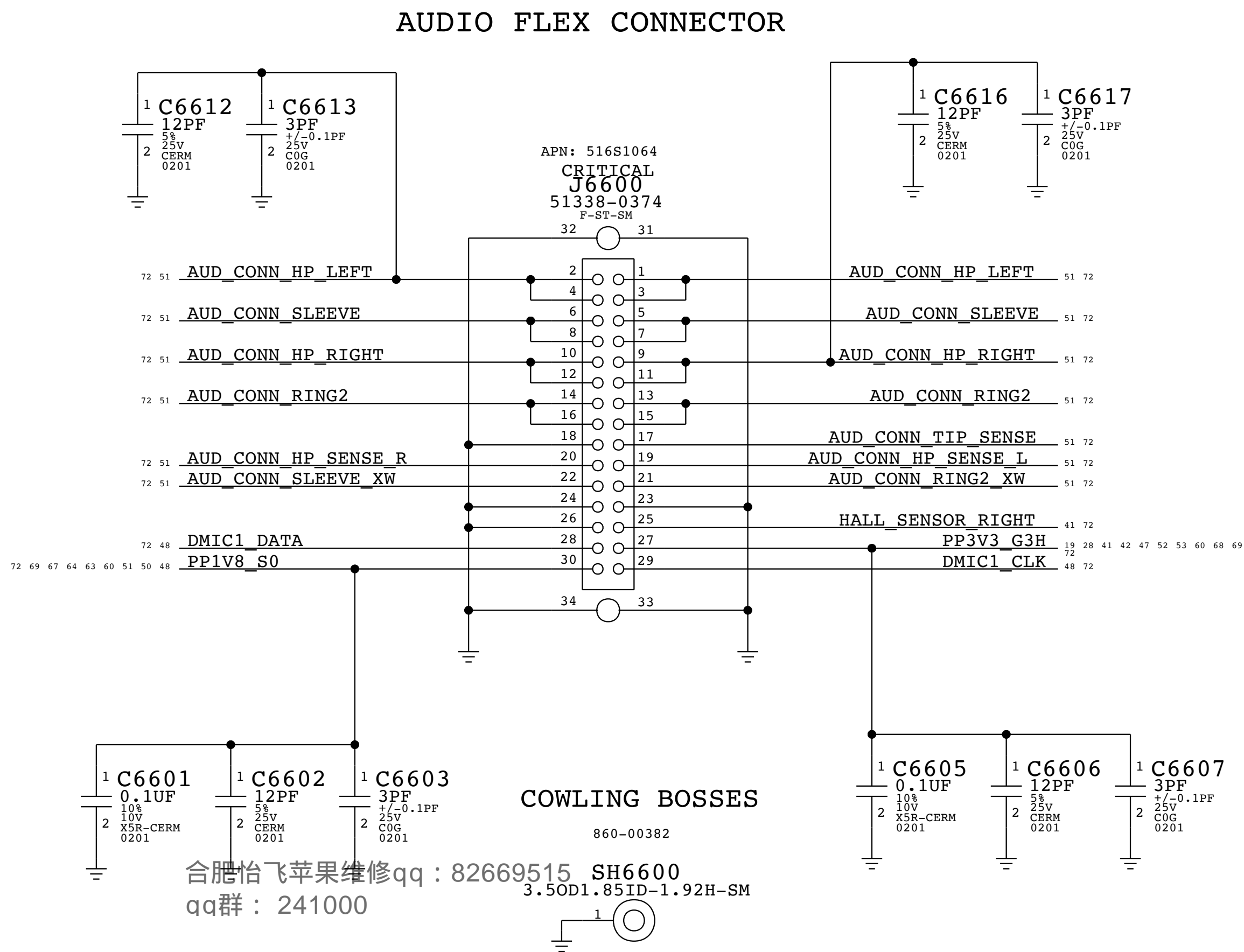
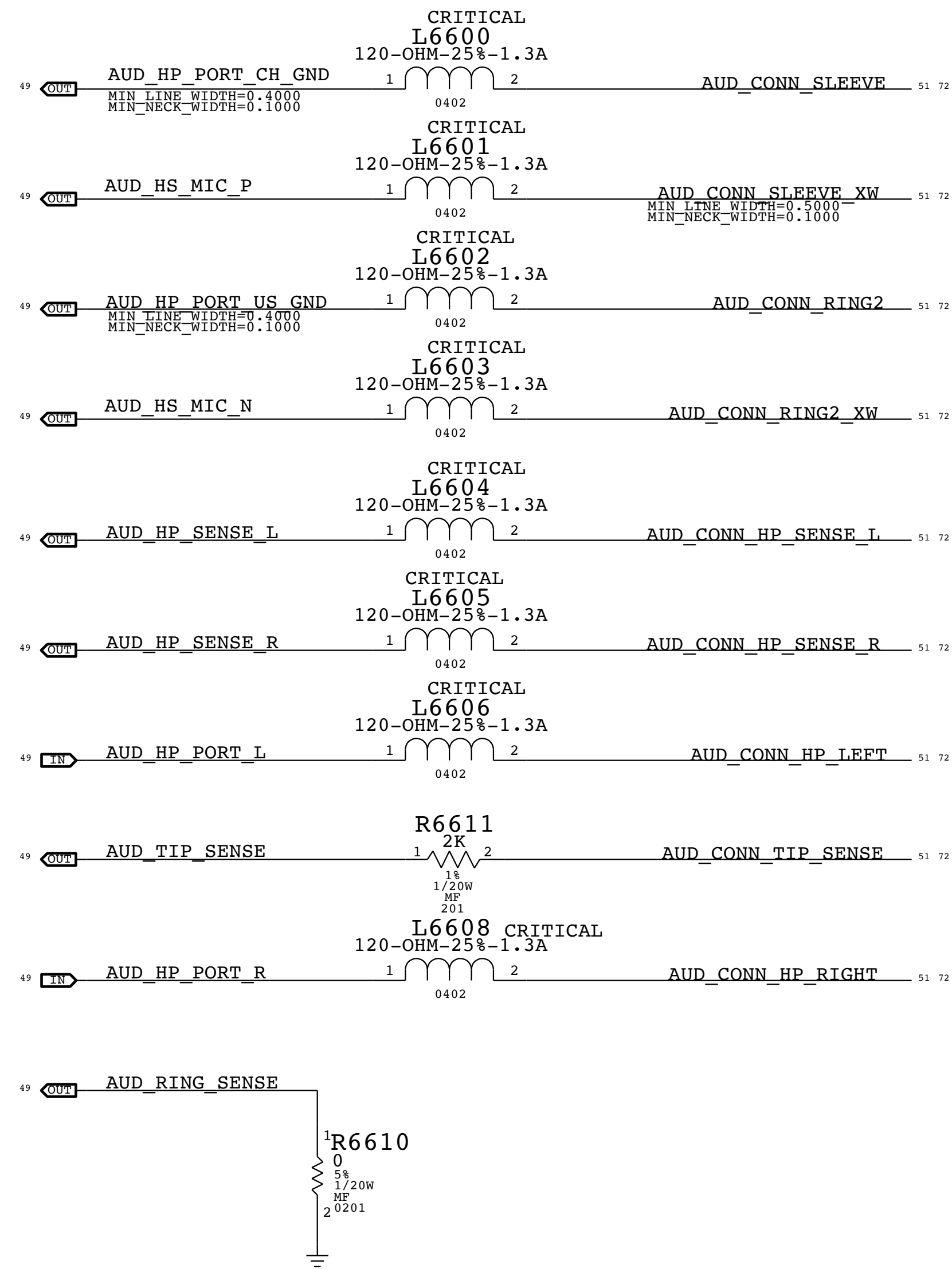
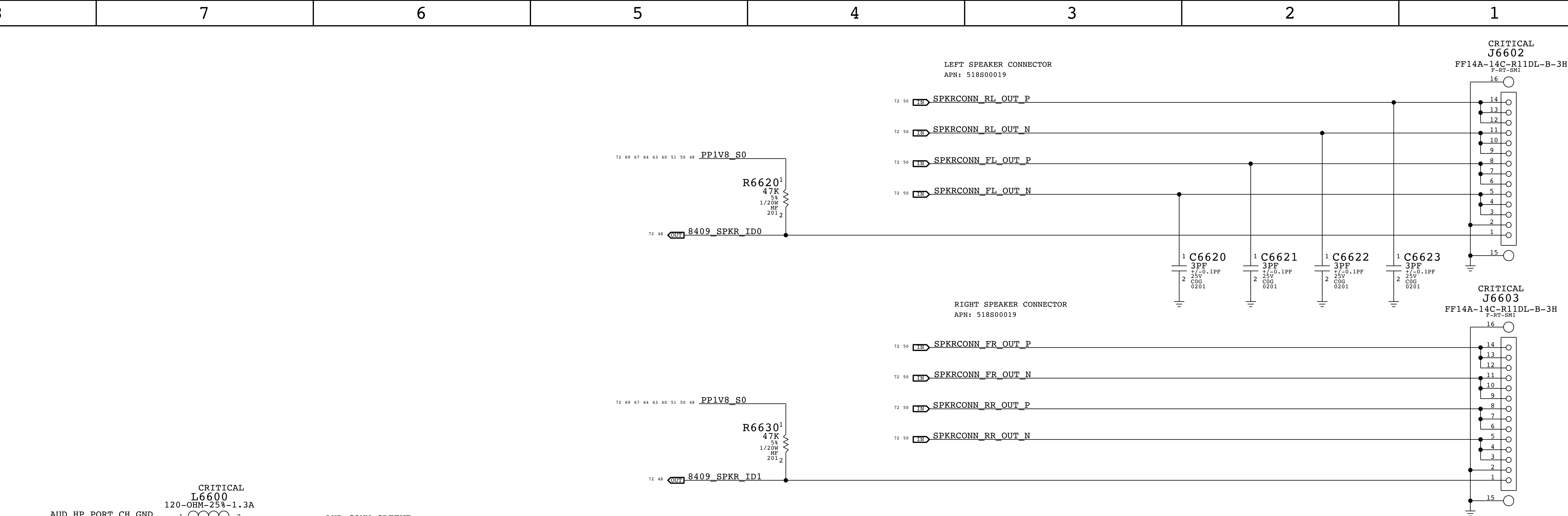
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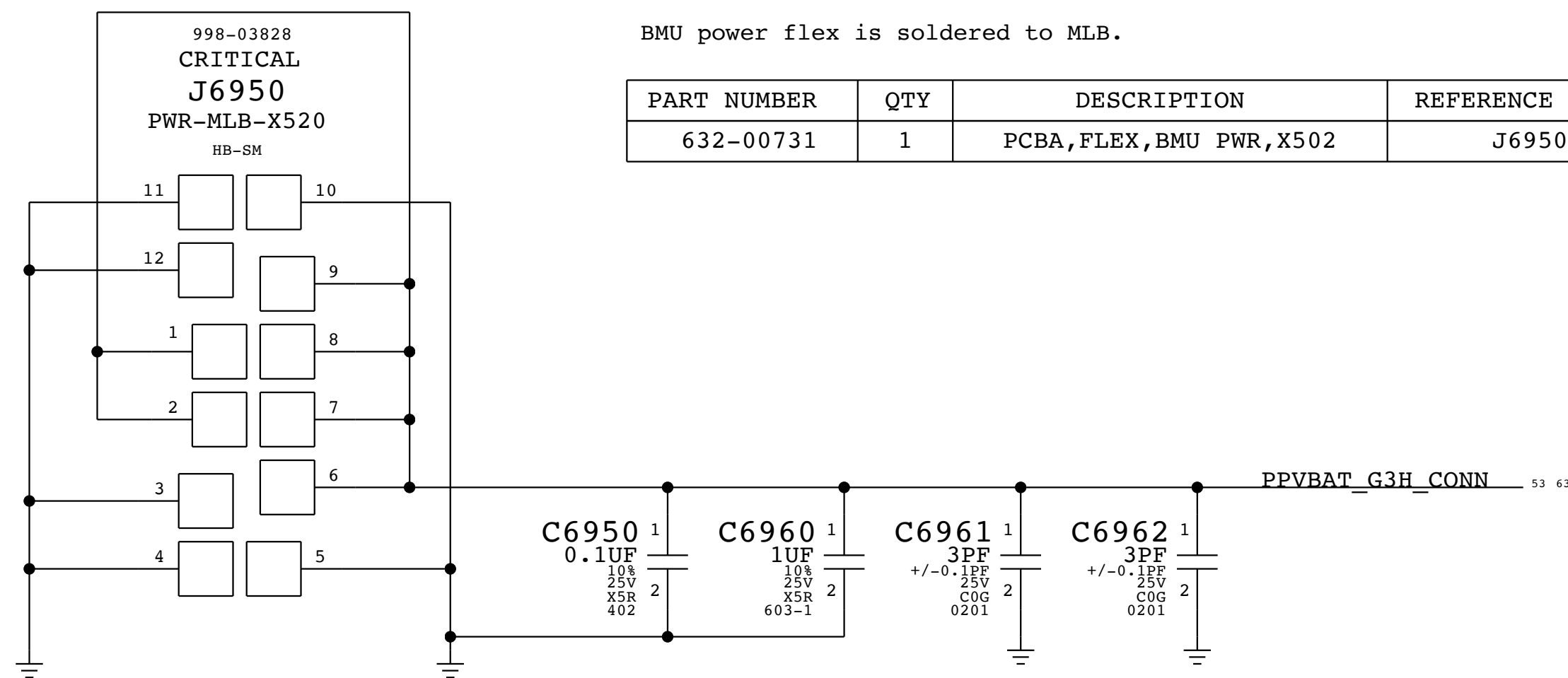
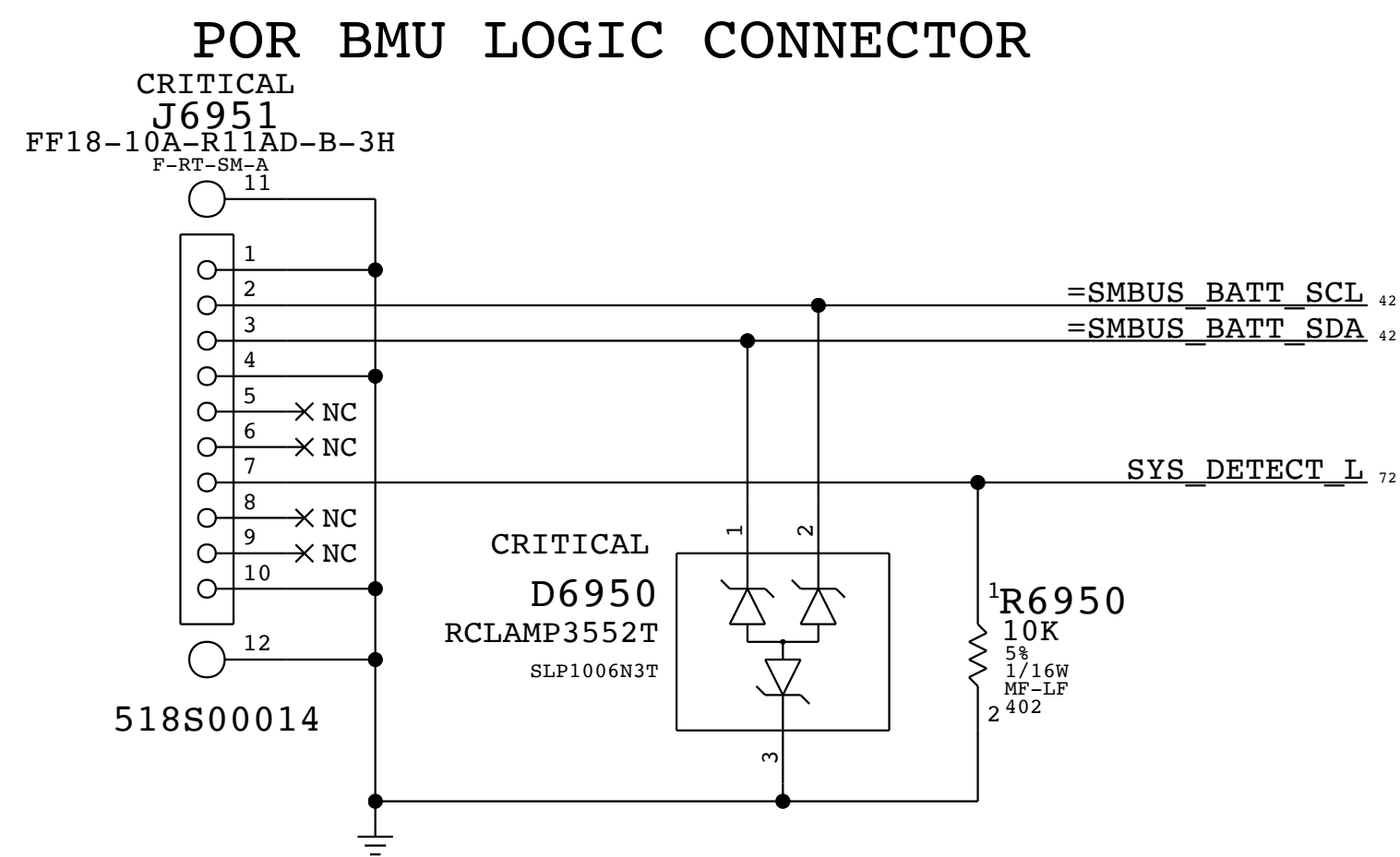
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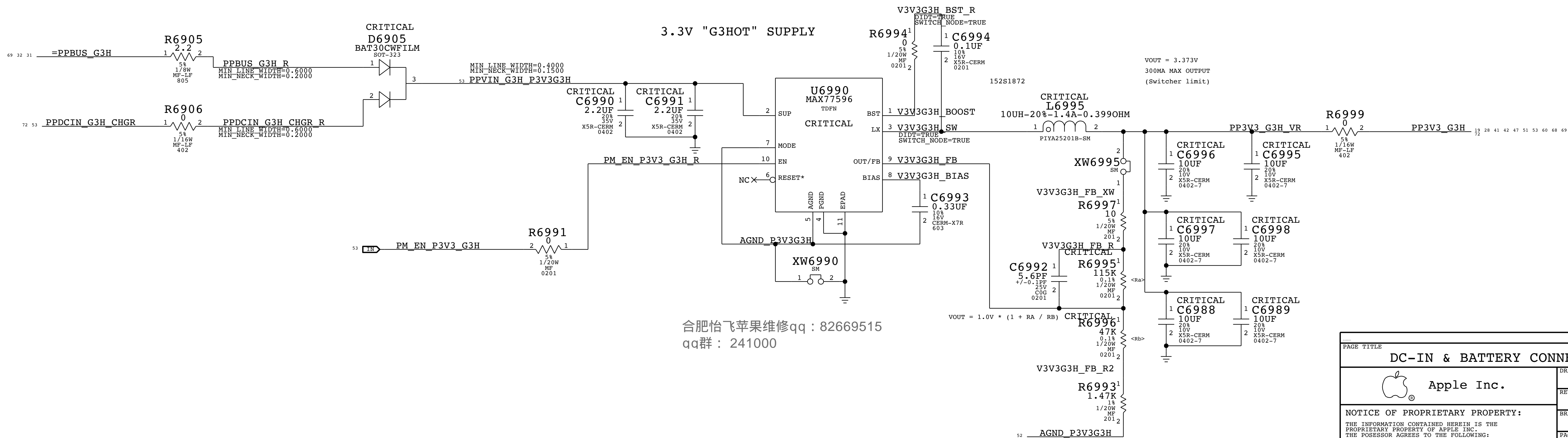
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BOM_COST_GROUP=AUDIO


POR BATTERY (BMU) FLEX SOLDER PADS.



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
632-00731	1	PCBA,FLEX,BMU PWR,X502	J6950	CRITICAL	



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DC-IN & BATTERY CONNECTORS		051-02265		D
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		69 OF 500		
		SHEET		
		52 OF 73		

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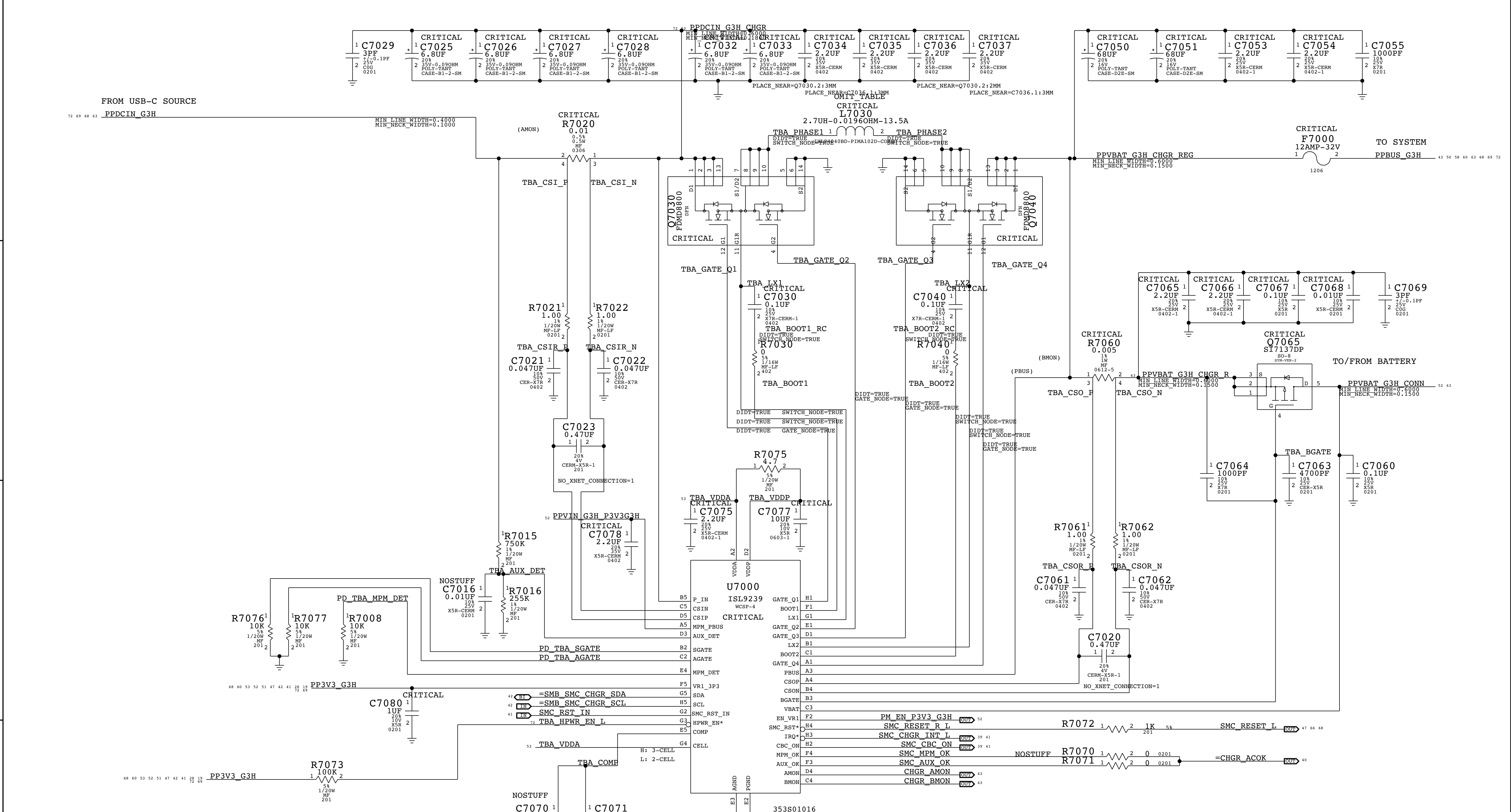
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S00198	1	IND,MLD,2.7UH,19.6MO,12.5A,10.9X10X2.4MM	L7030	CRITICAL	

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PAGE TITLE

SYNCHDATE=06/15/2015

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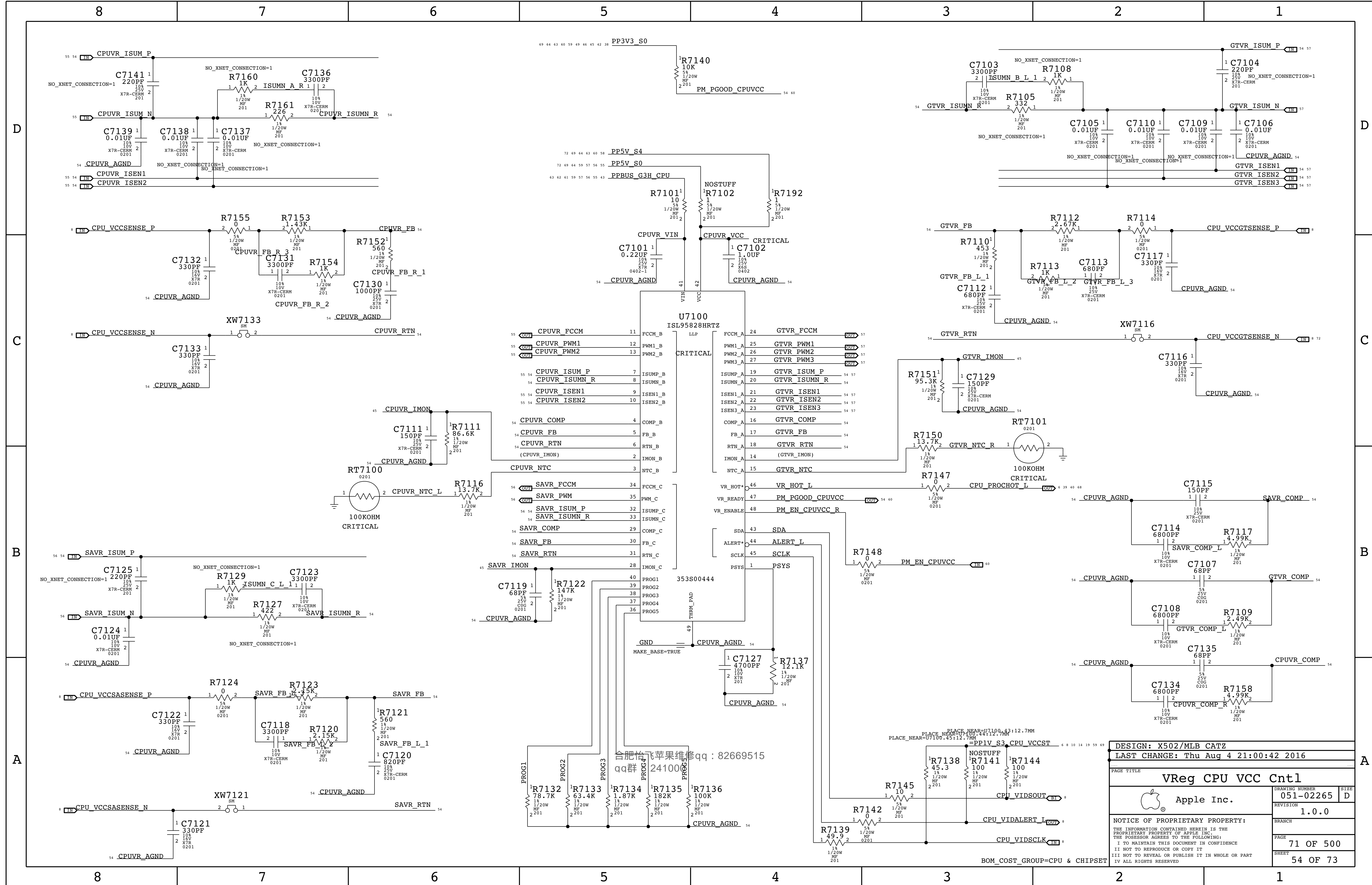
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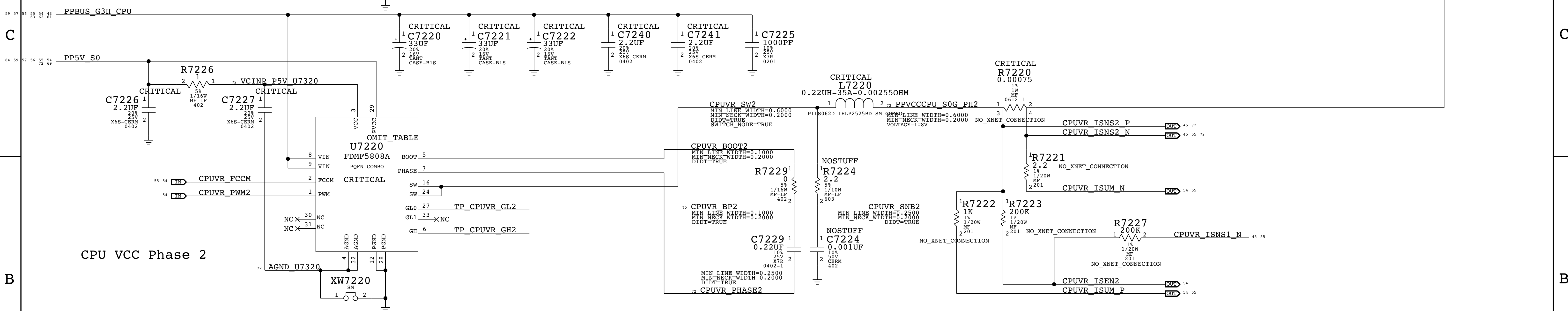
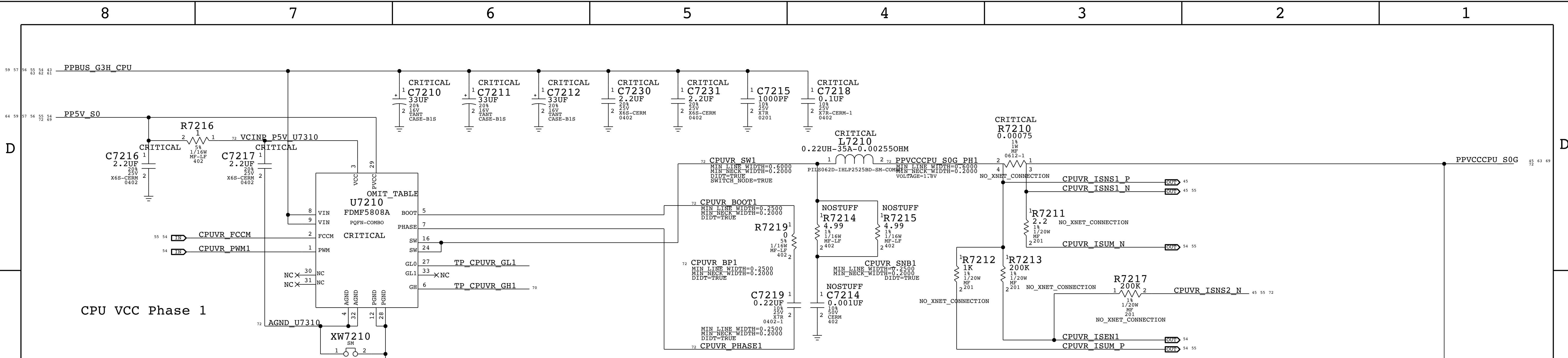
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BOM_COST_GROUP=PLATFORM POWER



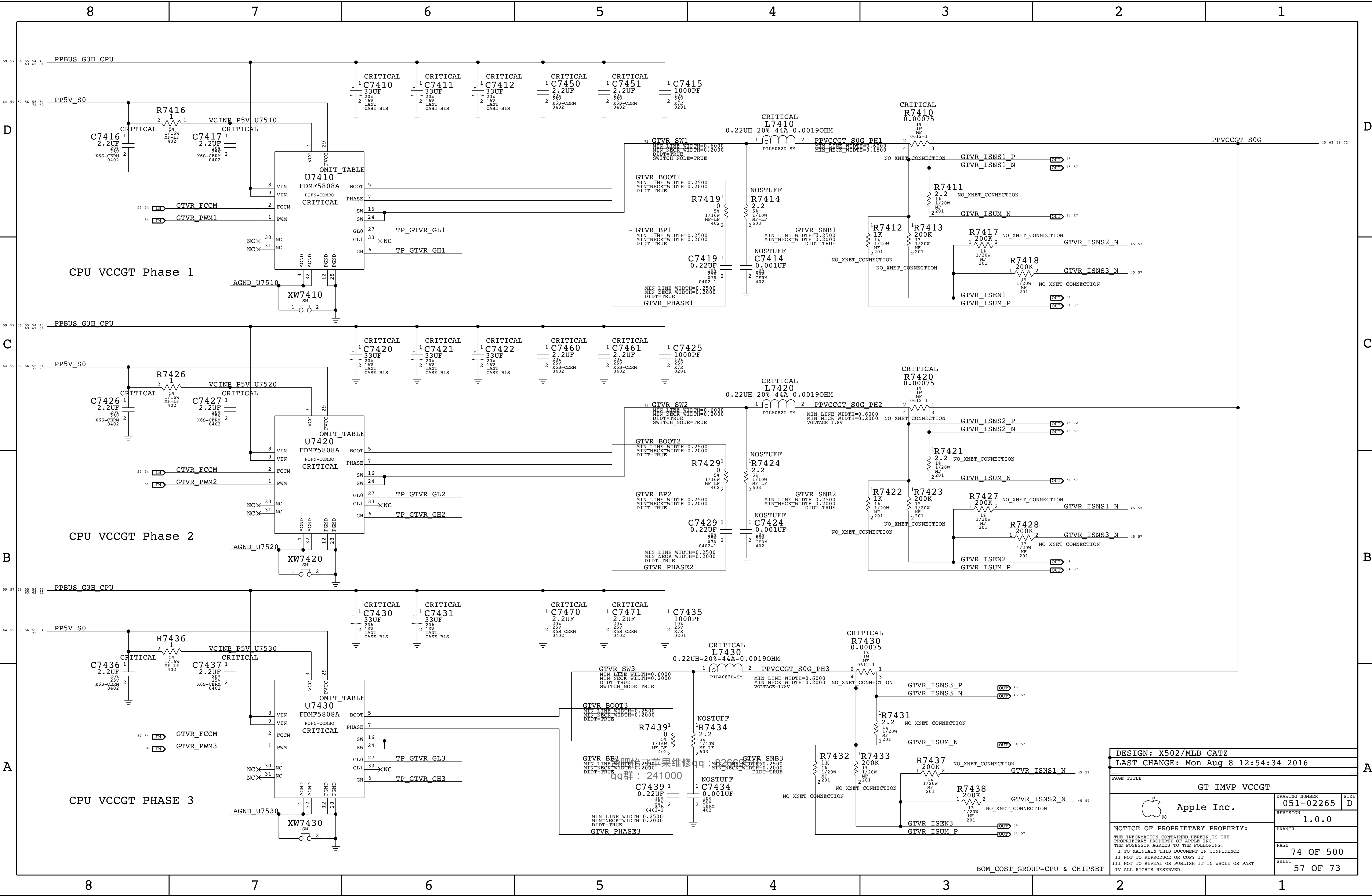



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00497	5	IC, SIC635, DR MOS, IMVP-8, 40A, PQFN31, 5X5	U7210, U7220, U7410, U7420, U7430	CRITICAL	

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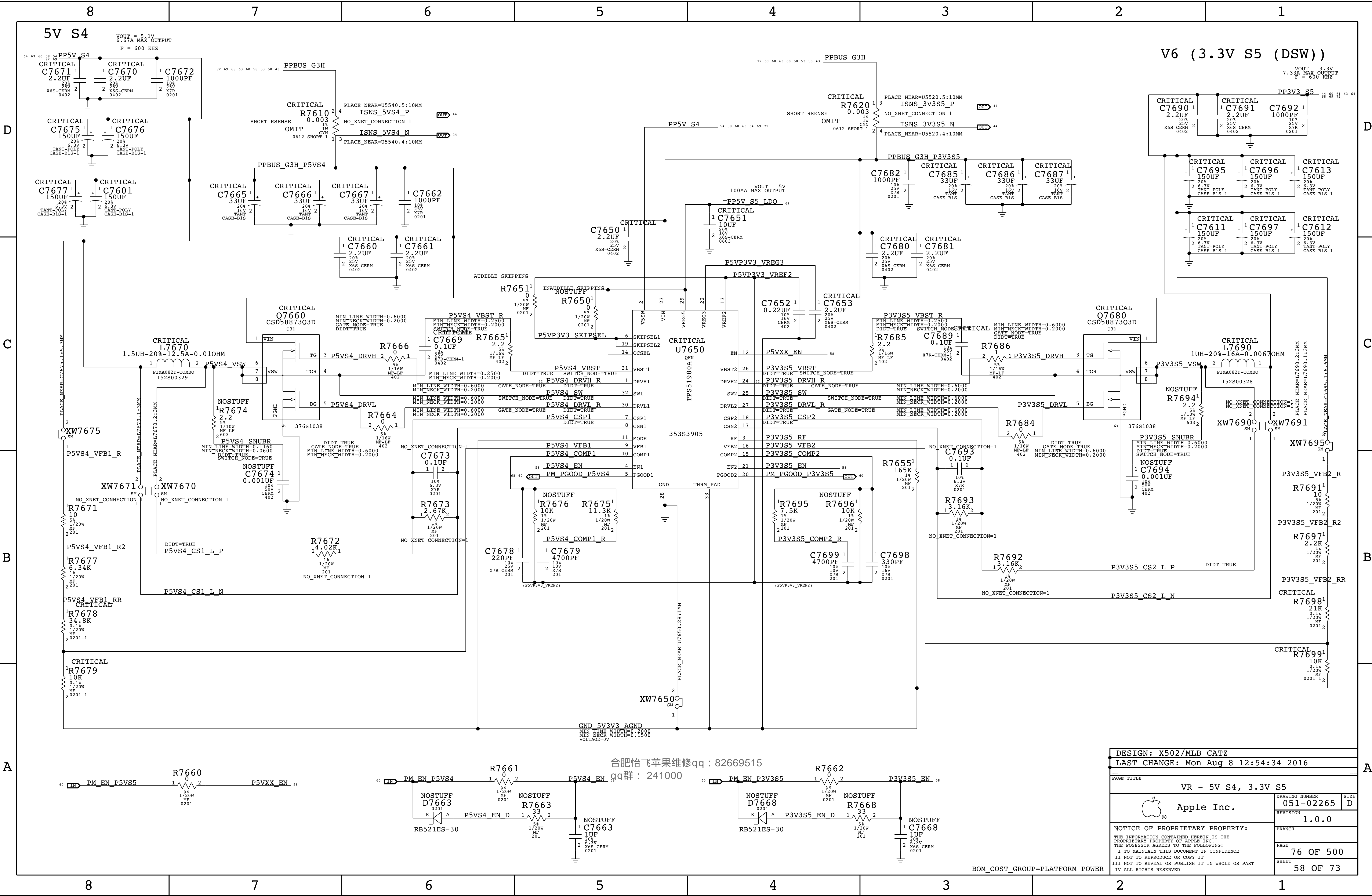
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CPU IMVP VCC & VCCSA			
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		SHEET 55 OF 73	

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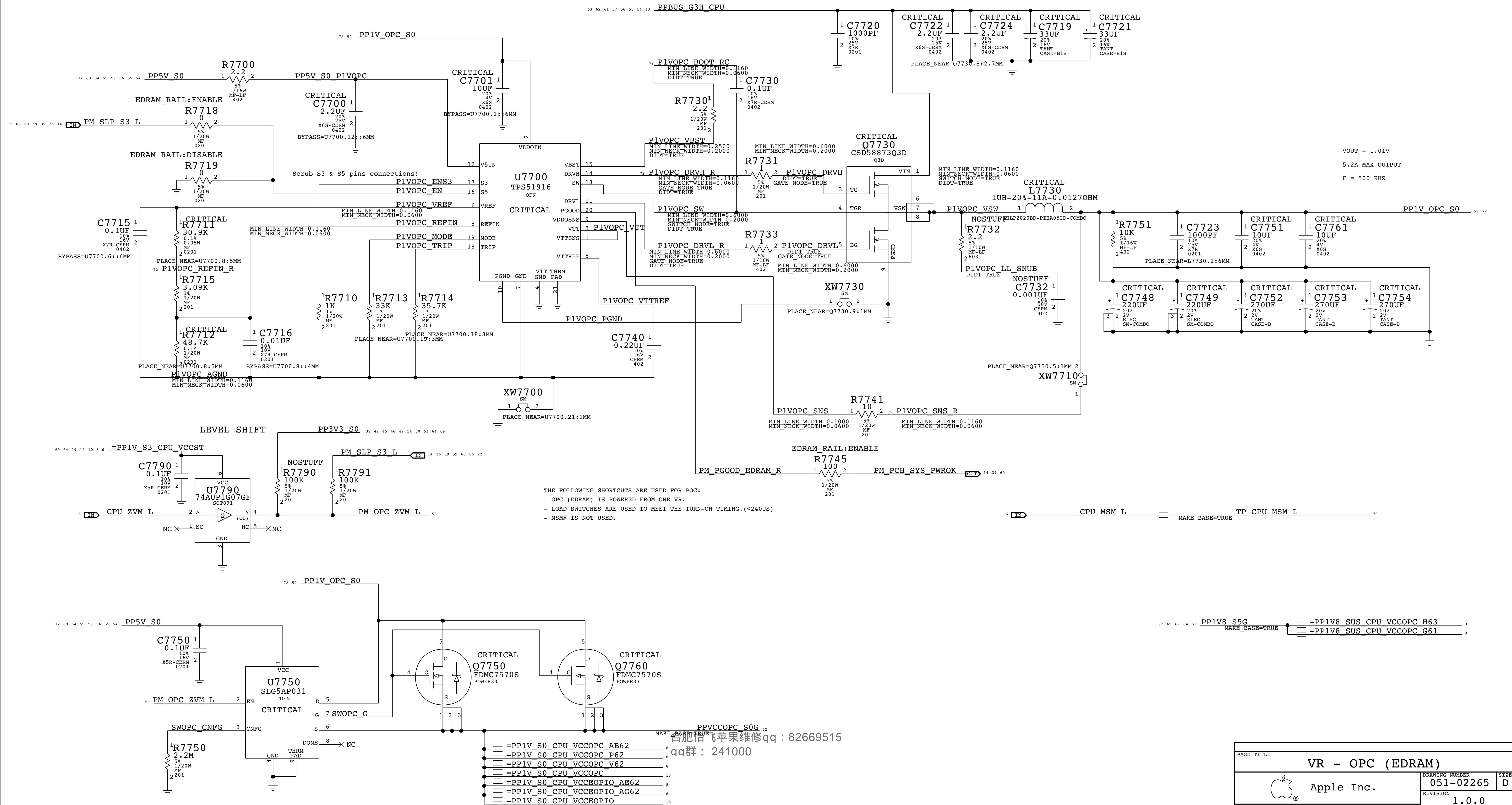


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GT IMVP VCCGT		
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BOM_COST_GROUP=CPU & CHIPSET

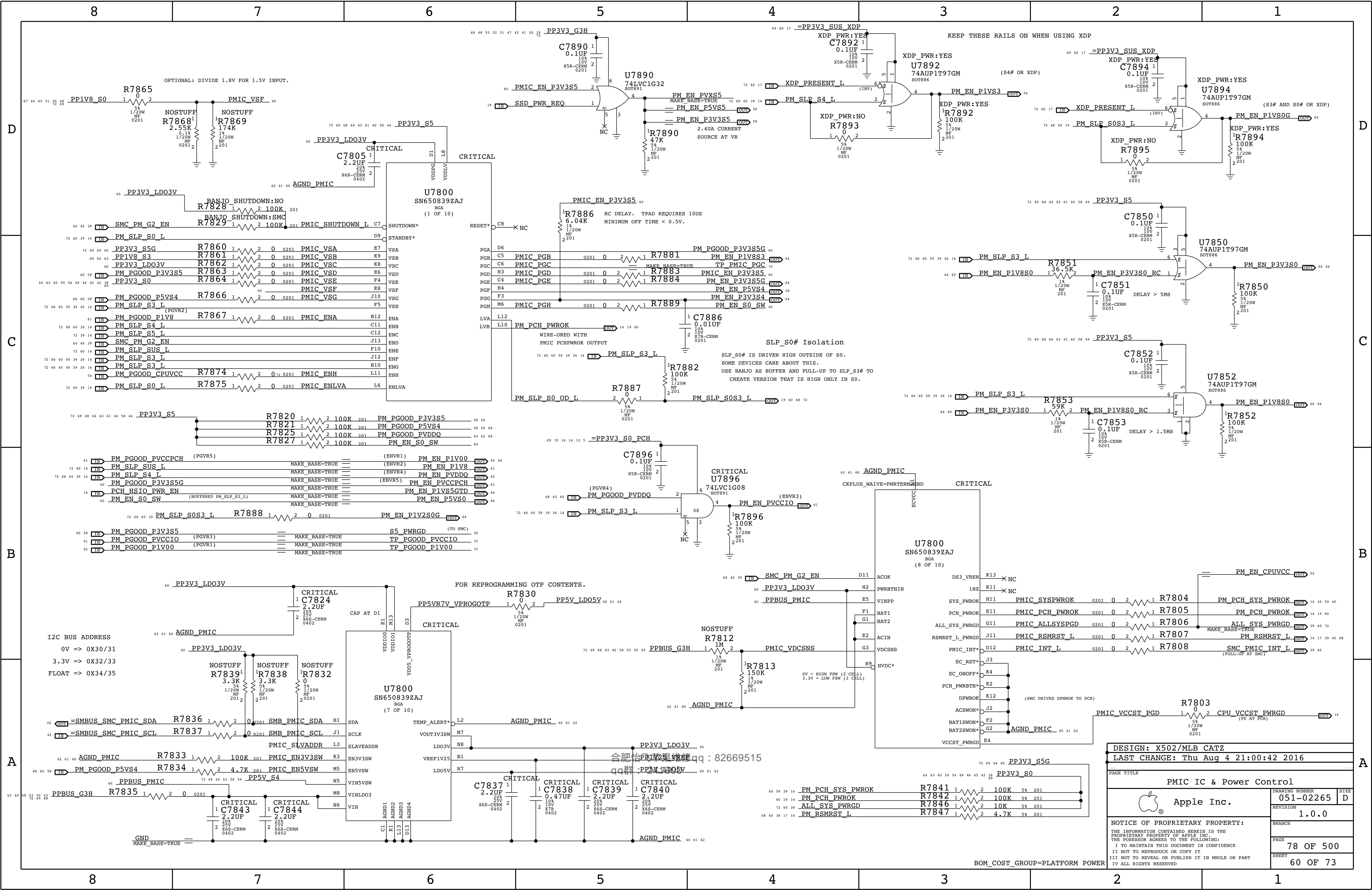


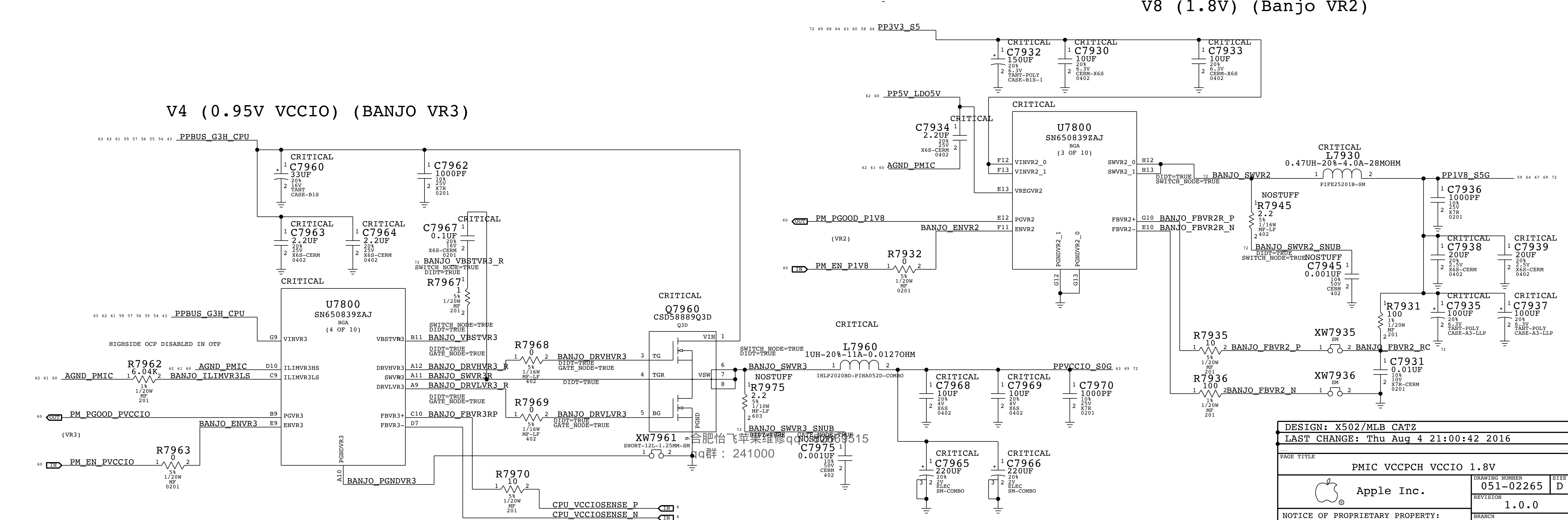
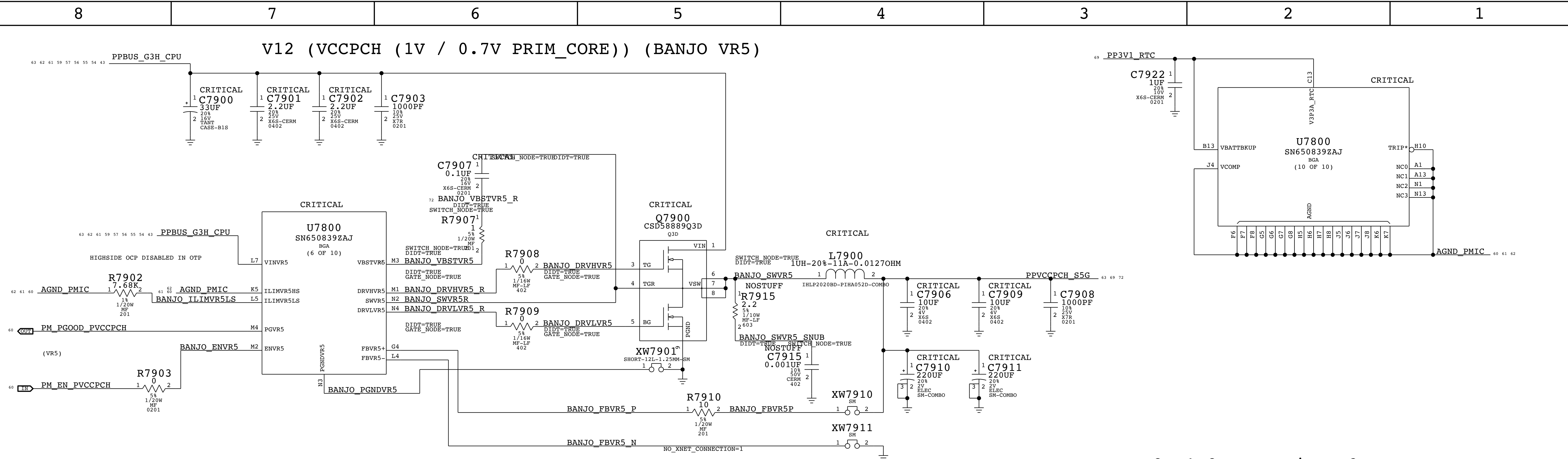
1V S0 REGULATOR FOR EDRAM (ON-PACKAGE CACHE)




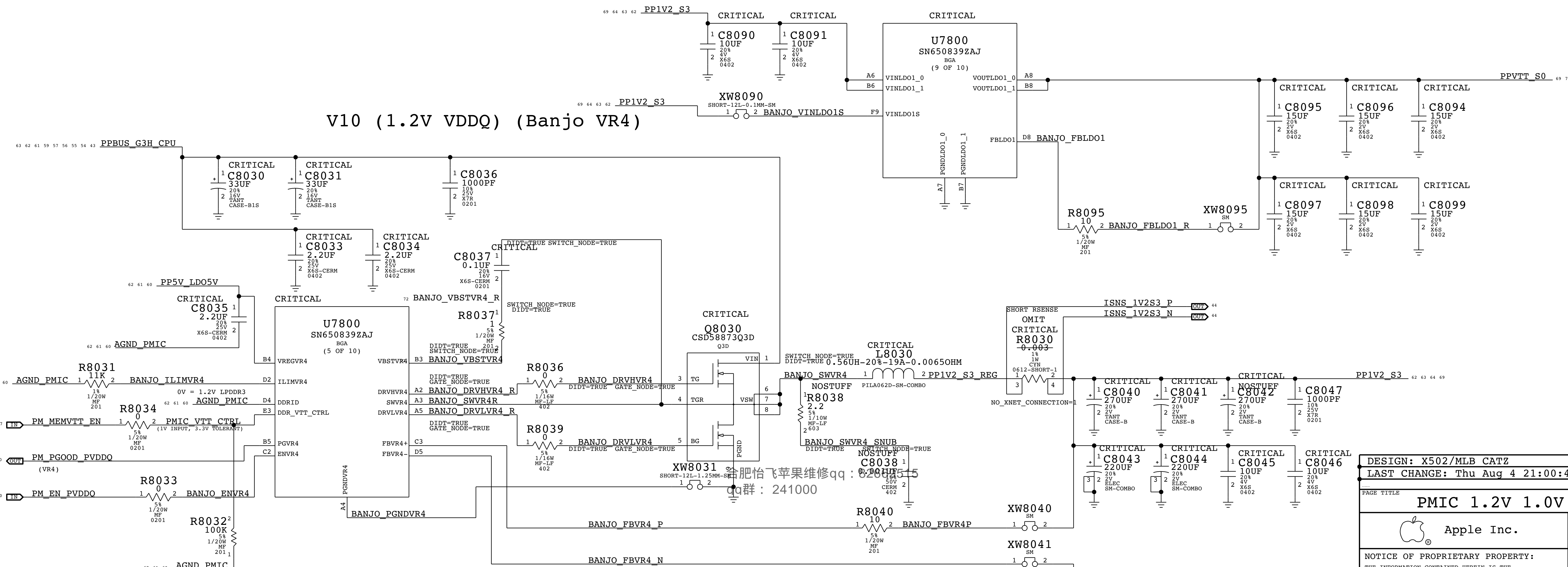
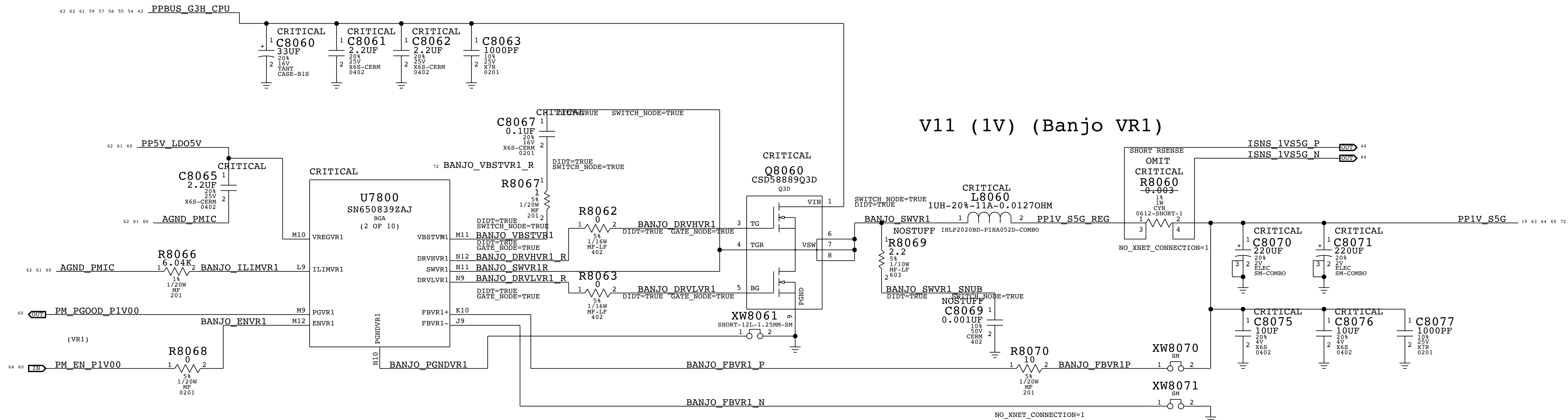
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BOM_COST_GROUP=CPU & CHIPSET

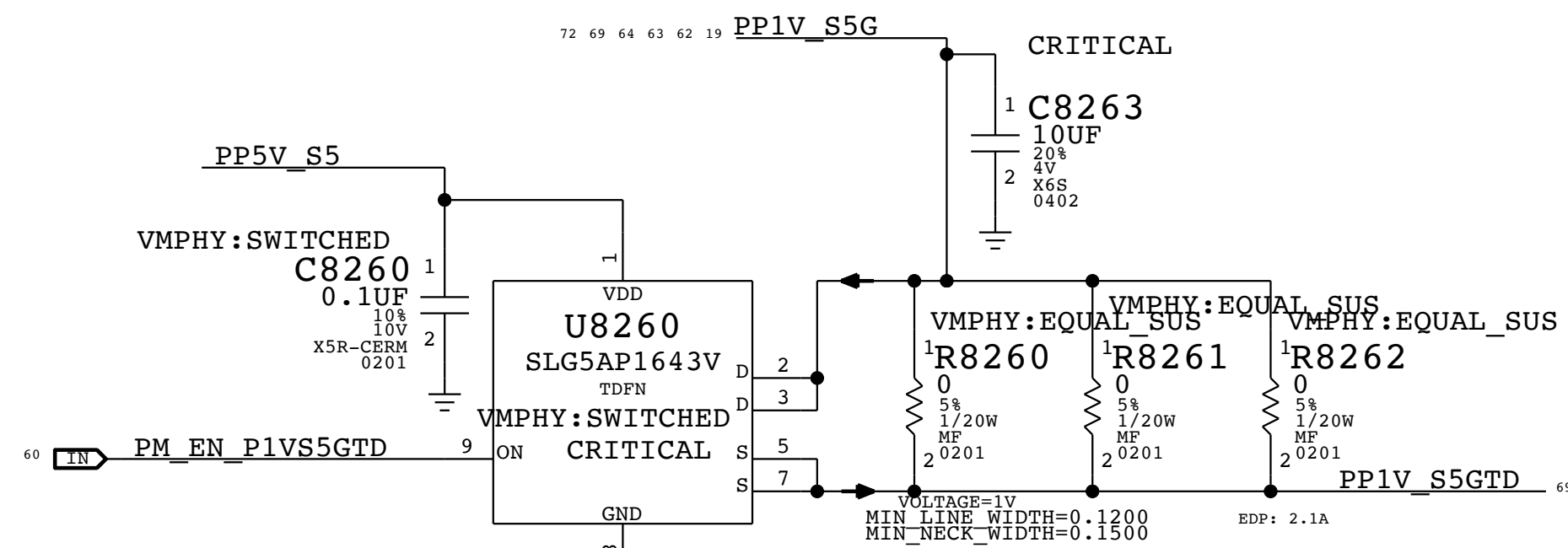




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		SHEET 61 OF 73	

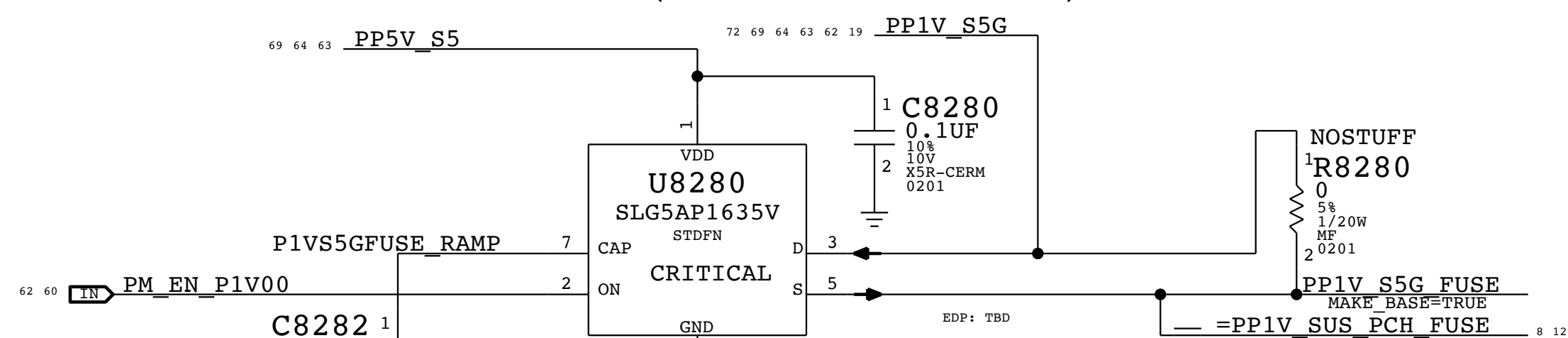


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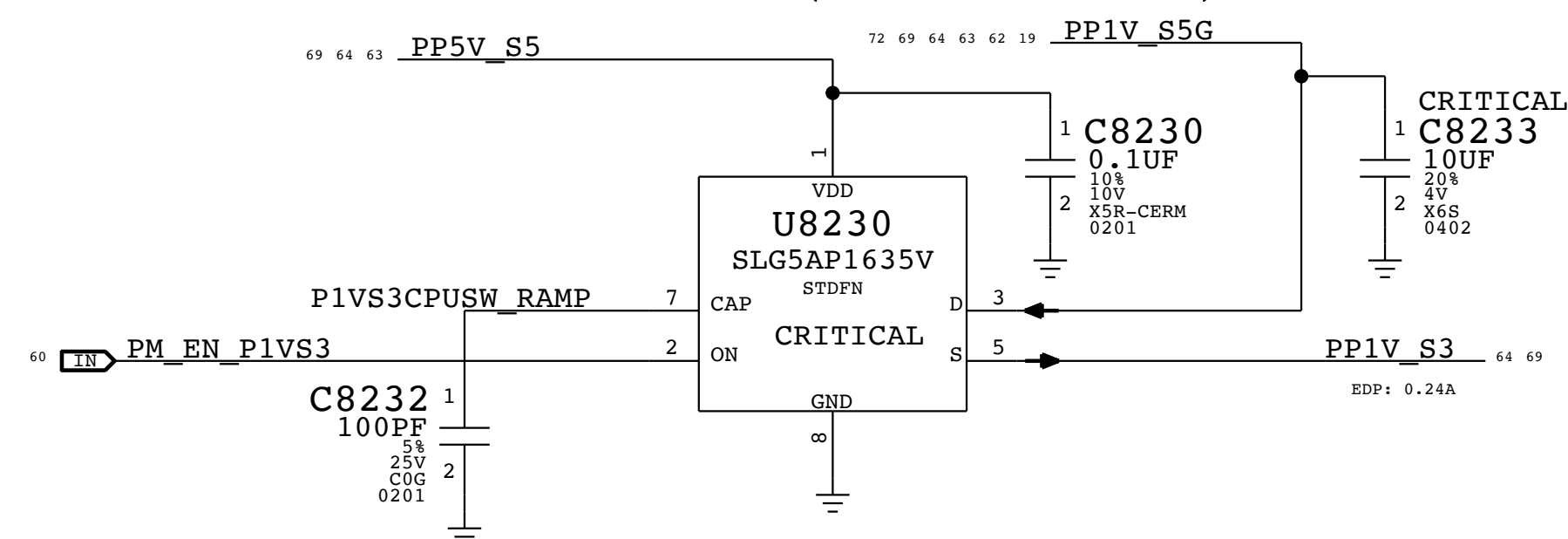
Part	SLG5AP1643V
Type	Load Switch
R(on) @ 25C	7.4 MOHM TYP
R(on) @ 70C	10.6 MOHM MAX
Current	6A MAX
TON-TOTAL	65US MAX @ 1V

1V S5G FUSE (FOR FAST TURN OFF)



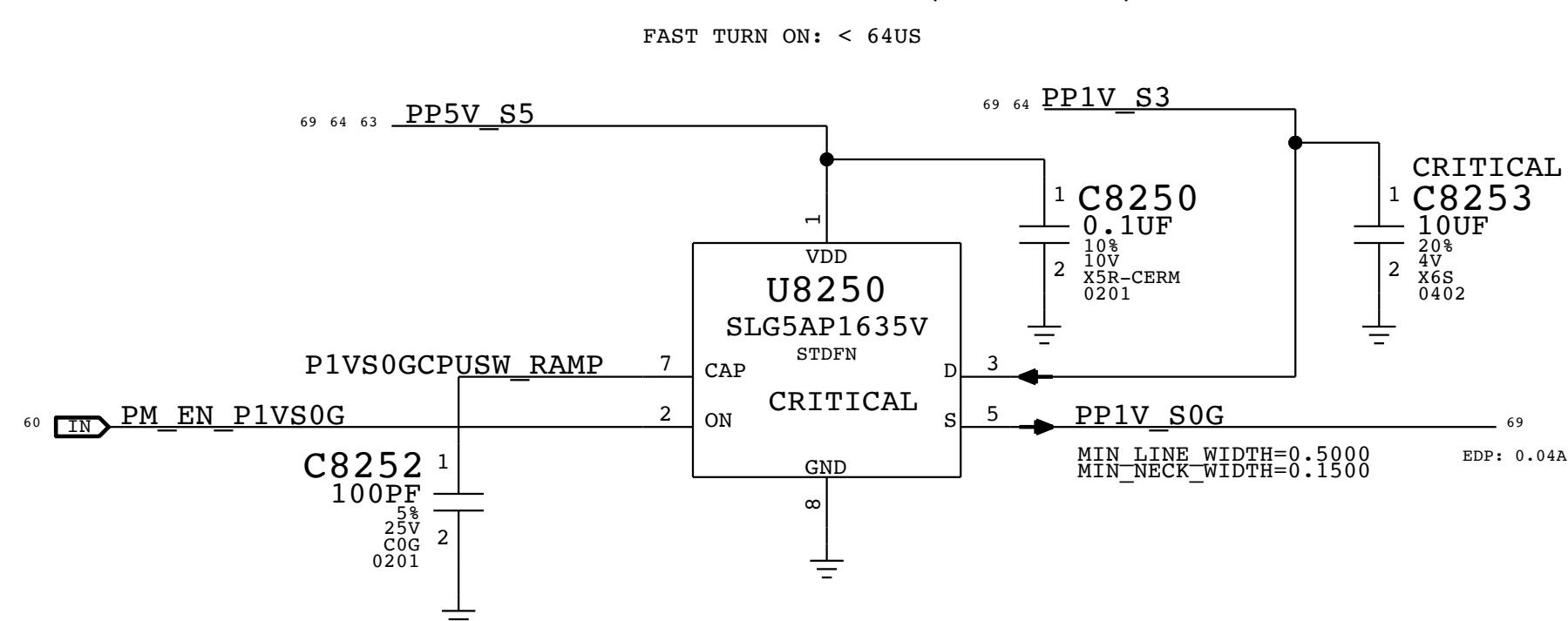
Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 MOHM TYP 28 MOHM MAX
Current	2.5A MAX
TON-TOTAL	39US MAX @ 1V

1V S3 SWITCH (VCCST, VCCPLL)



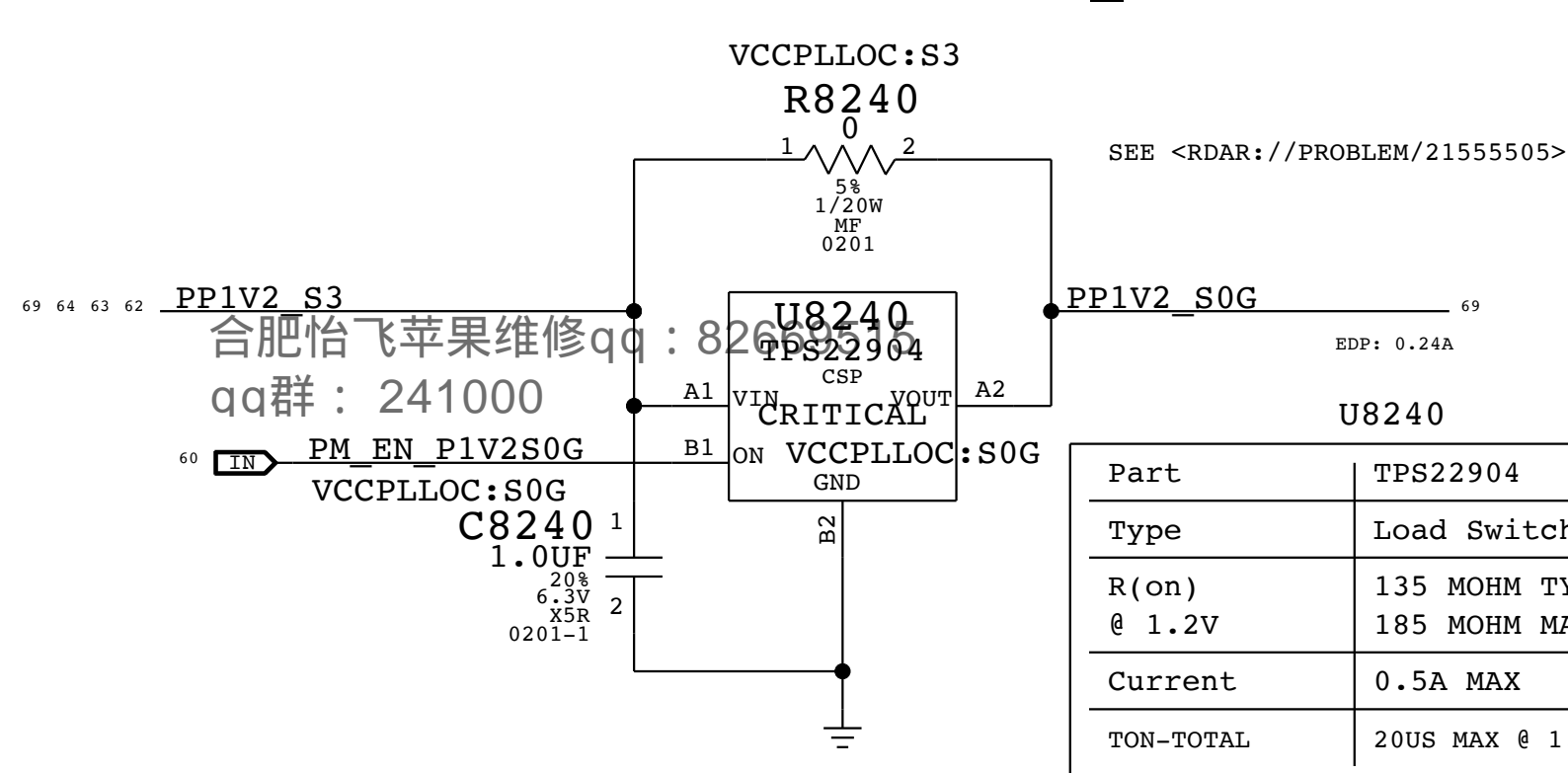
Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 MOHM TYP 28 MOHM MAX
Current	2.5A MAX
TON-TOTAL	39US MAX @ 1V

1V S0G CPU SWITCH (VCCSTG)

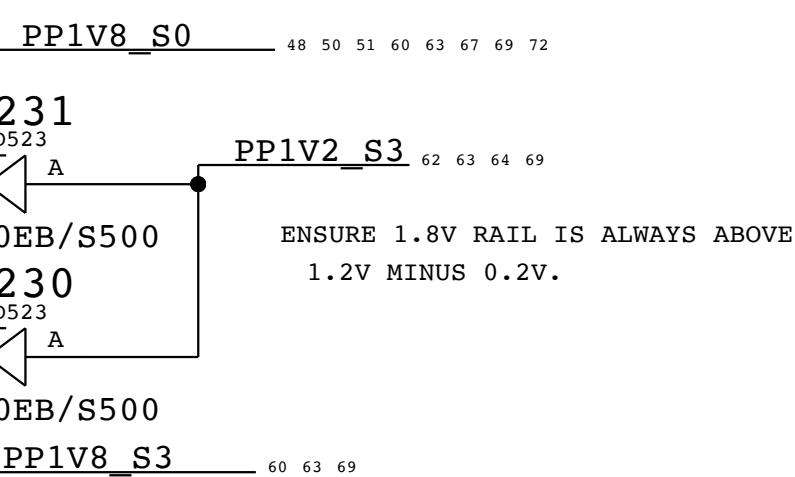


Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 MOHM TYP 28 MOHM MAX
Current	2.5A MAX
TON-TOTAL	39US MAX @ 1V

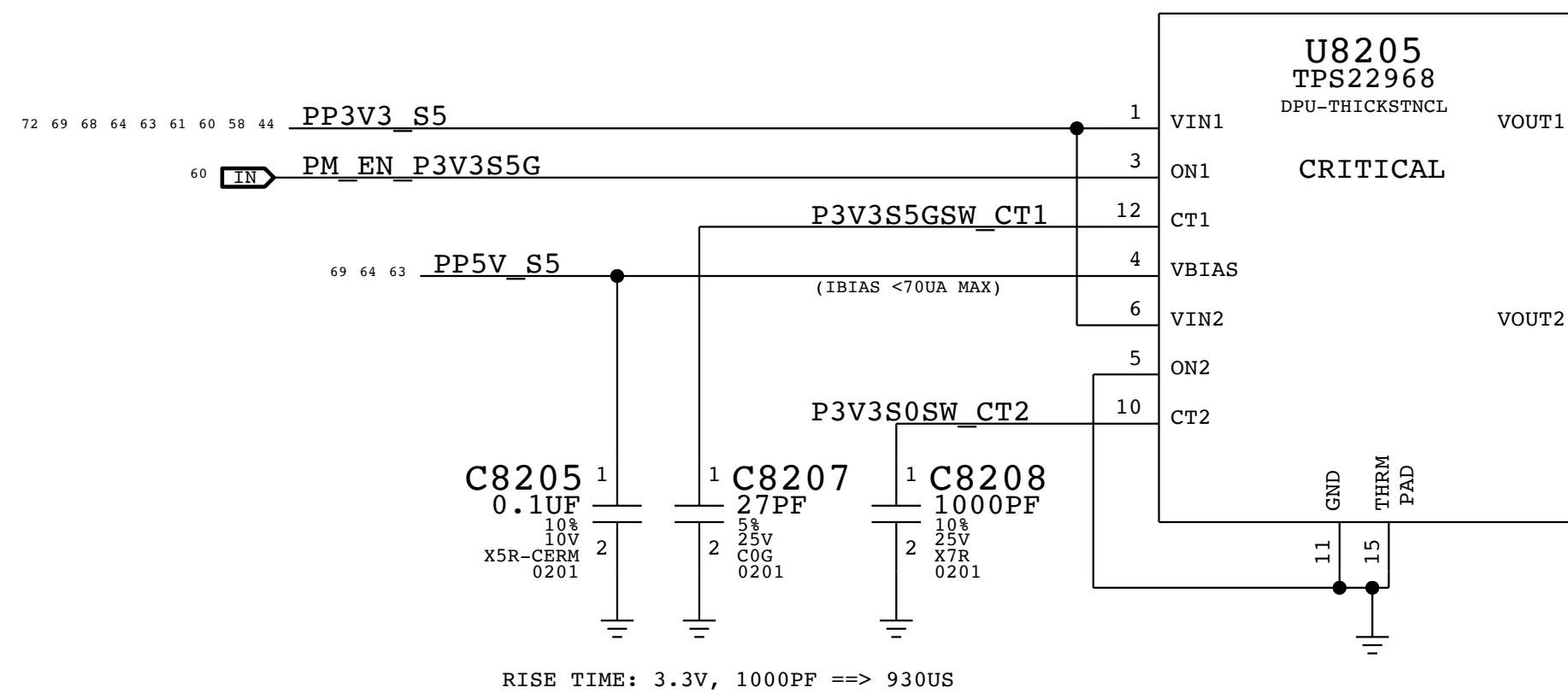
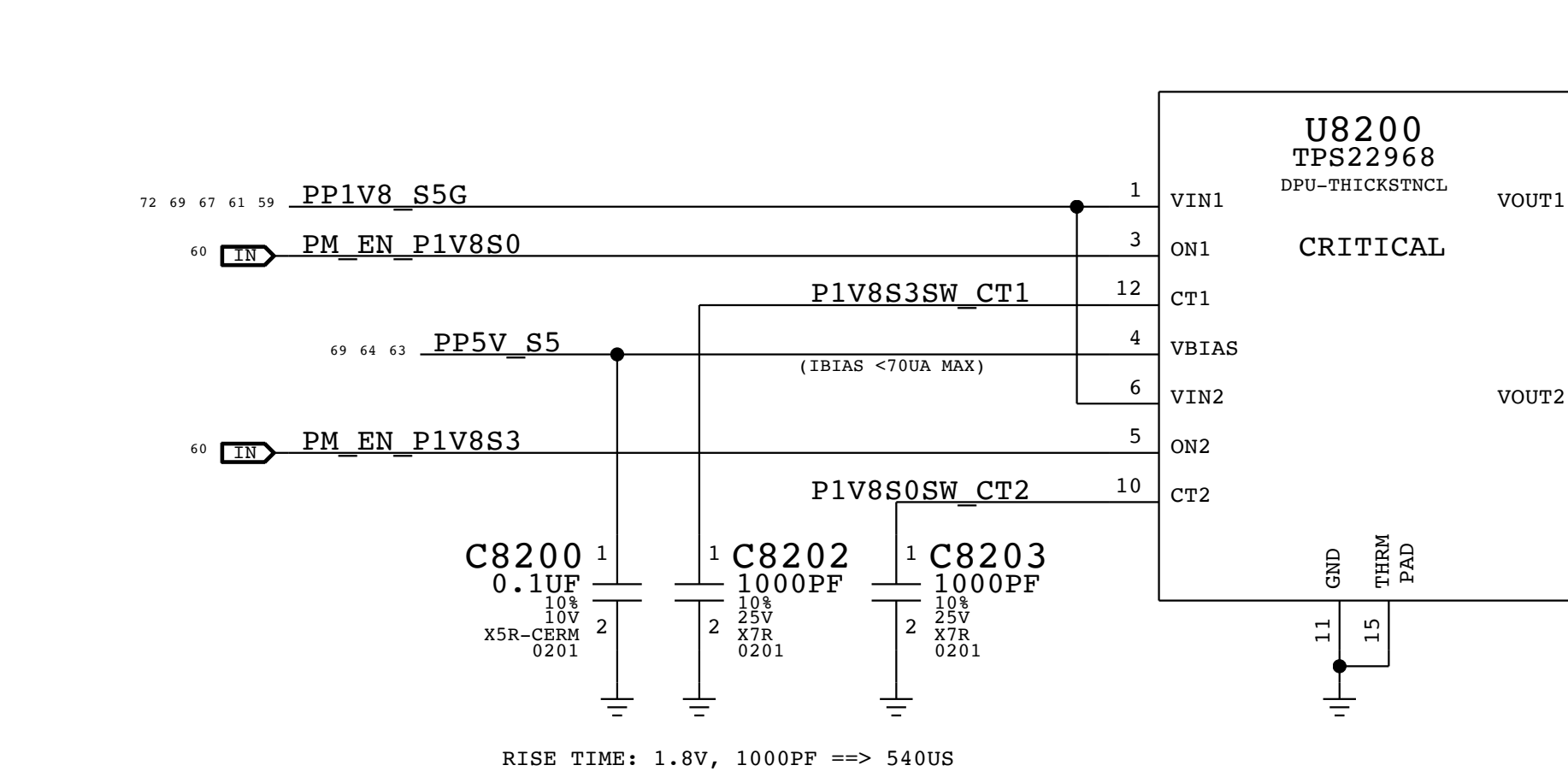
1V2 S0G SWITCH (VCCPLL_OC)



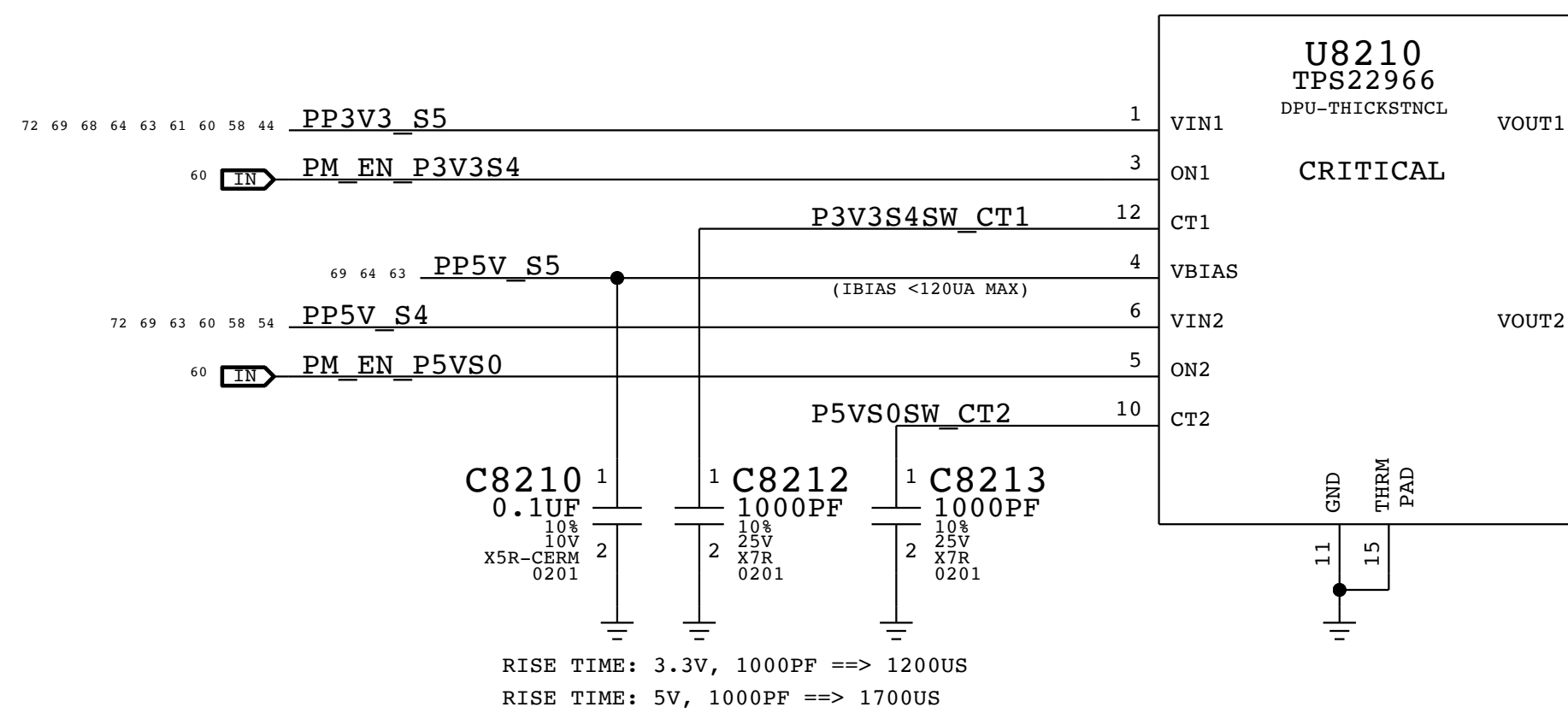
U8240	
Part	TPS22904
Type	Load Switch
R(on) @ 1.2V	135 MOHM TYP 185 MOHM MAX
Current	0.5A MAX
TON-TOTAL	20US MAX @ 1.2V



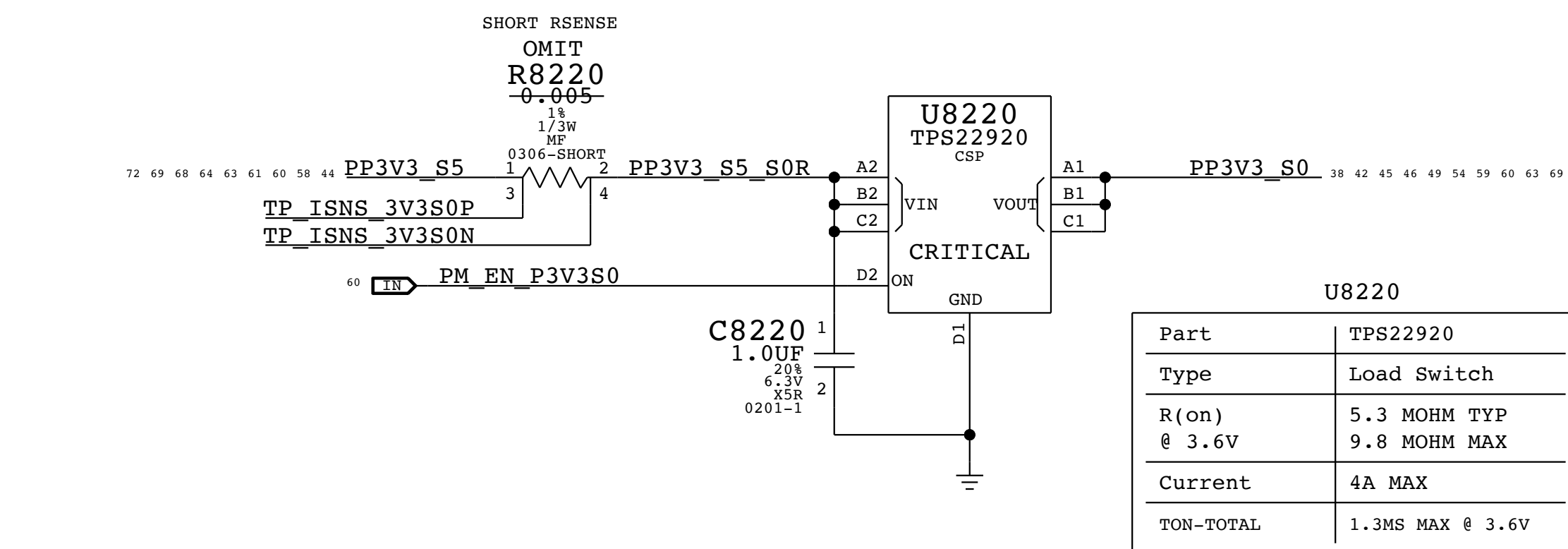
U8200	
Part	TPS22968
Type	LOAD SWITCH - DUAL
R(on) @ 5V VBIAS	25 MOHM TYP 38 MOHM MAX
Current	4A MAX
TON-TOTAL	1MS MAX @ 1.8V



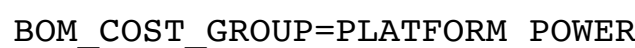
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Part	TPS22968
Type	LOAD SWITCH - DUAL
R(on) @ 5V VBIAS	25 MOHM TYP 38 MOHM MAX
Current	4A MAX
TON-TOTAL	1.4MS MAX @ 3.3V




U8210	
Part	TPS22966
Type	LOAD SWITCH - DUAL
R(on) @ 5V VBIAS	18 MOHM TYP 27 MOHM MAX
Current	6A MAX
TON-TOTAL	1.7MS MAX @ 3,3V 2.4MS MAX @ 5V



U8220	
Part	TPS22920
Type	Load Switch
R(on) @ 3.6V	5.3 MOHM TYP 9.8 MOHM MAX
Current	4A MAX
TON-TOTAL	1.3MS MAX @ 3.6V



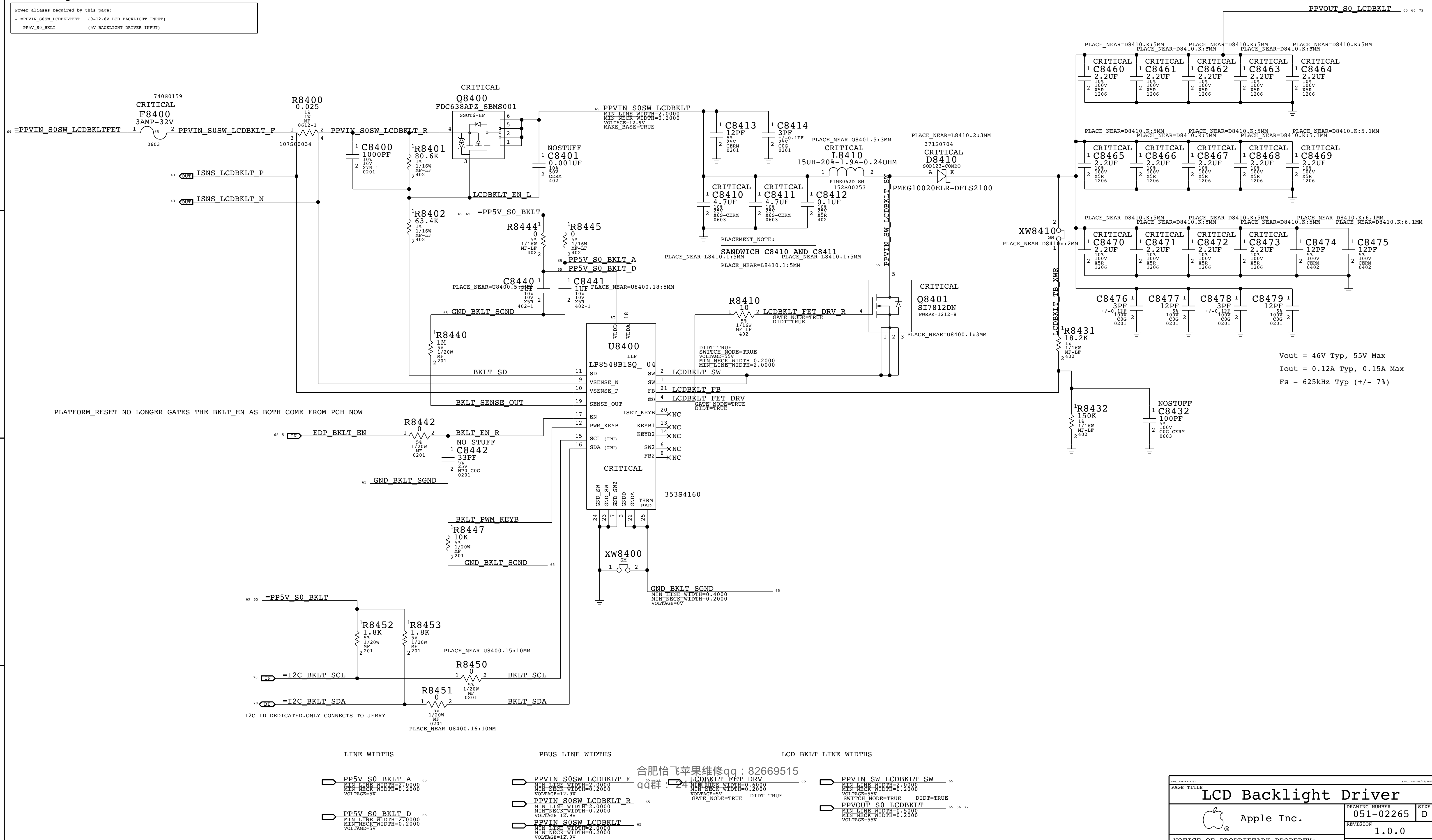
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Page Notes


Power aliases required by this page:

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- =PPVIN_S0SW_LCDBKLTPTET (9-12.6V LCD BACKLIGHT INPUT
```

- =PP5V_S0_BKLT (5V BACKLIGHT DRIVER INPUT)



BOM_COST_GROUP=DISPLAY

FORM 100 (01/01/2017)		FORM 100 (01/01/2017)	
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LCD Backlight		Driver	
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		65 OF 73	

LCD PANEL INTERFACE (eDP) + Camera (MIPI)

LCD Panel HPD & AUX strapping

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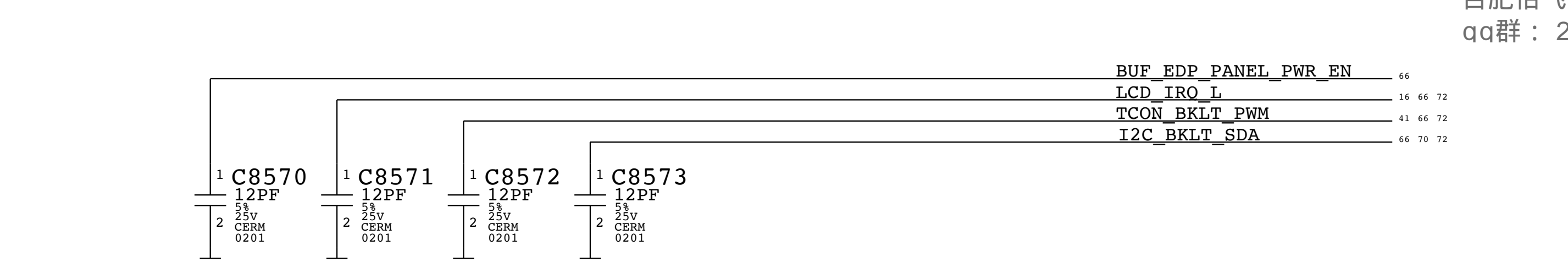
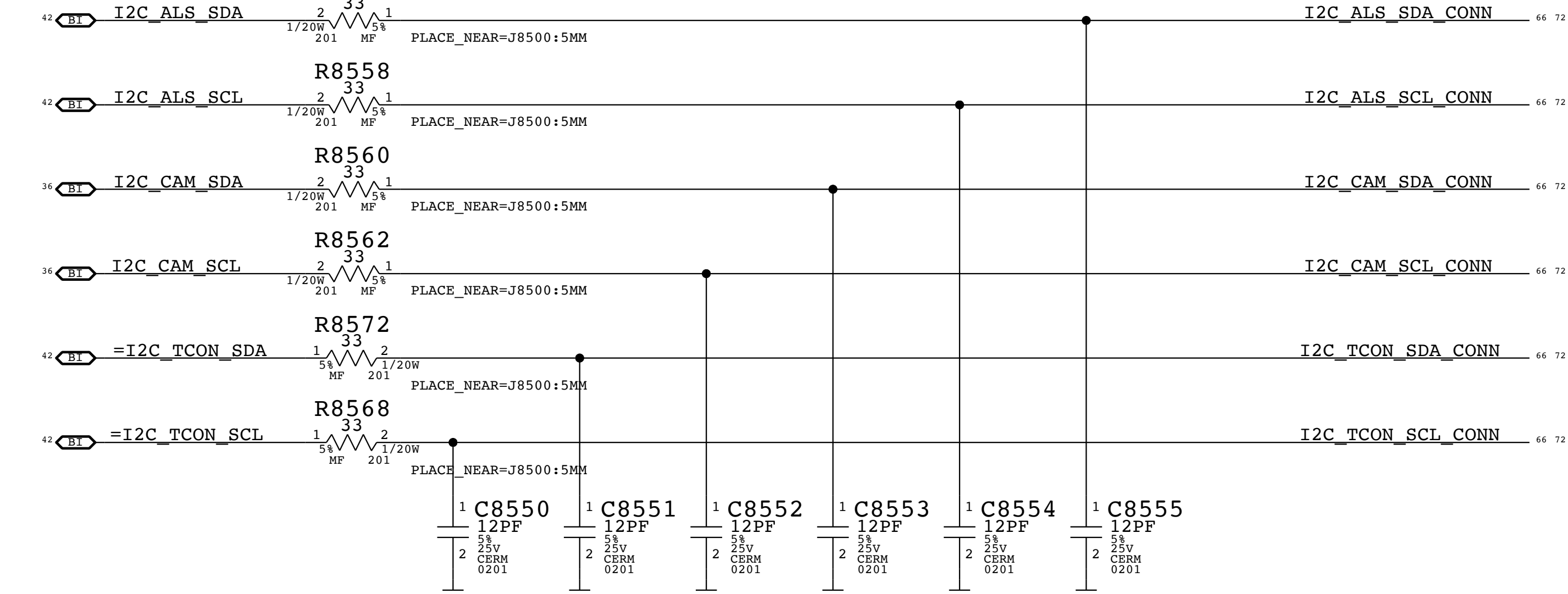
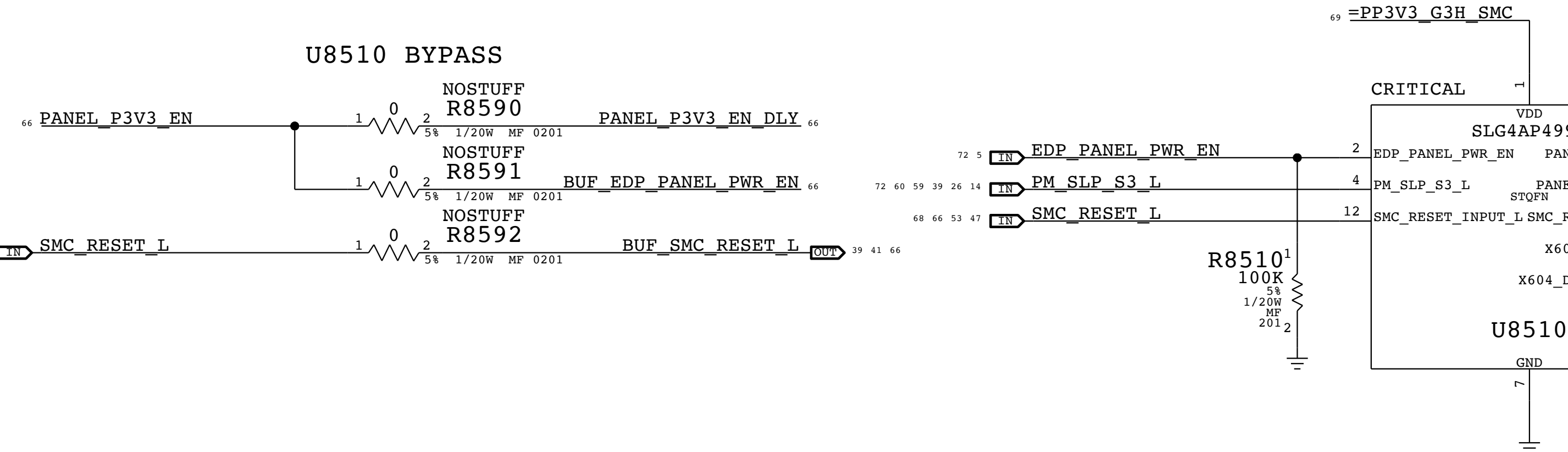
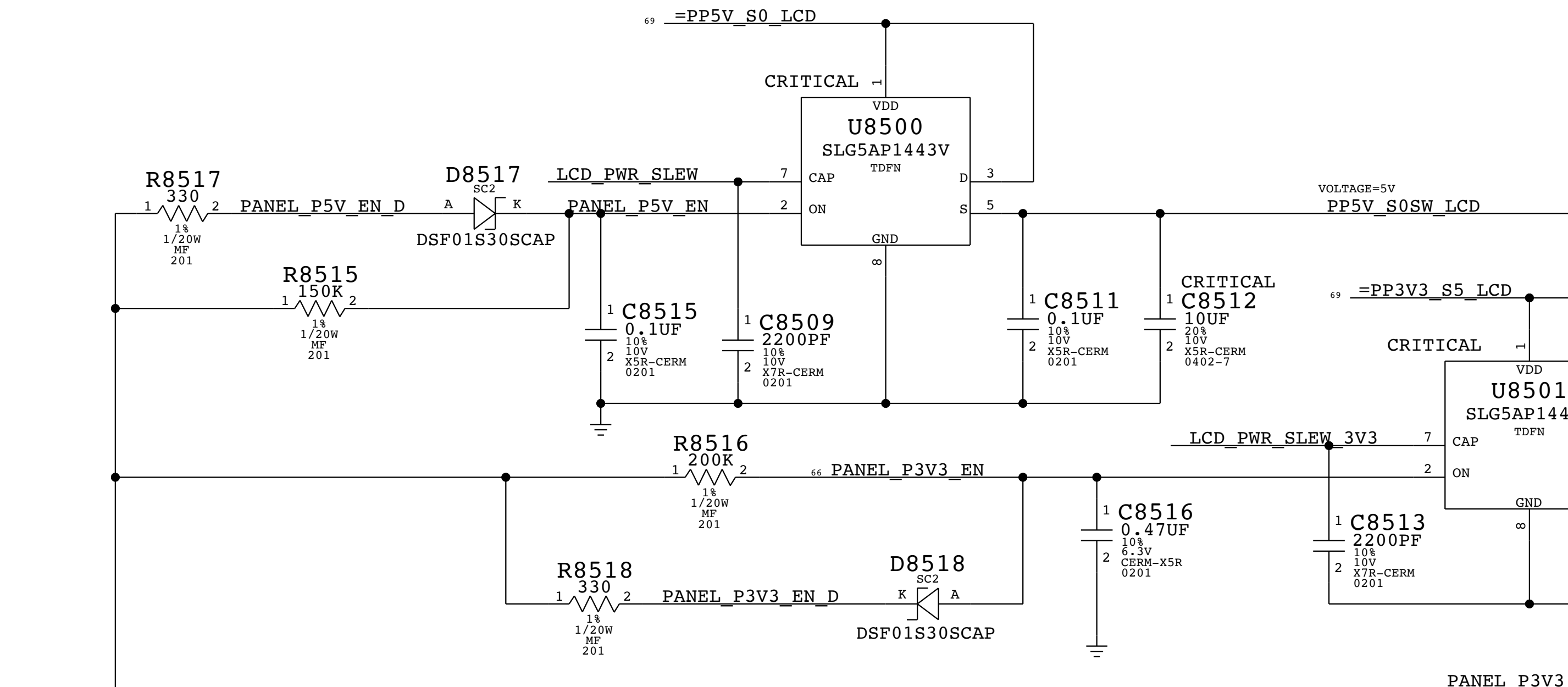
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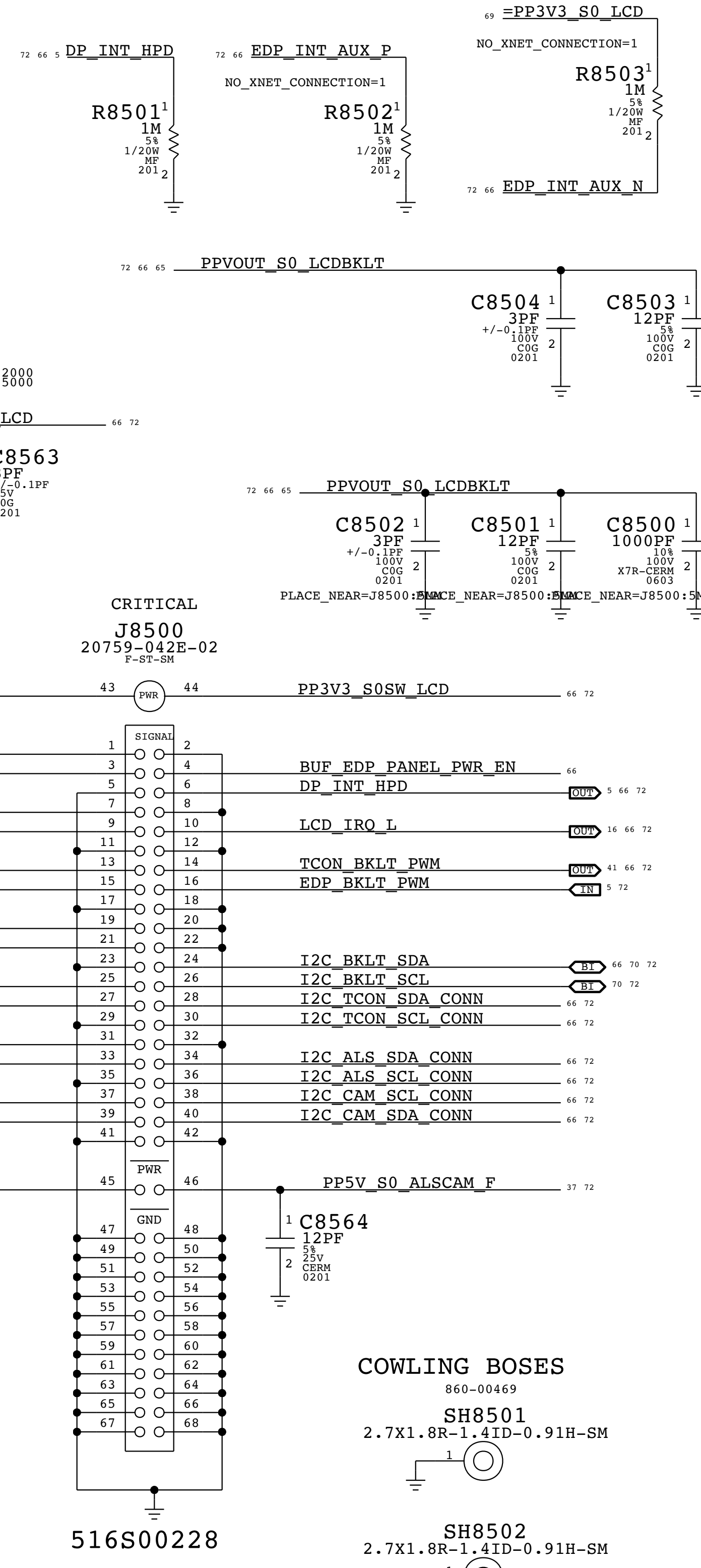
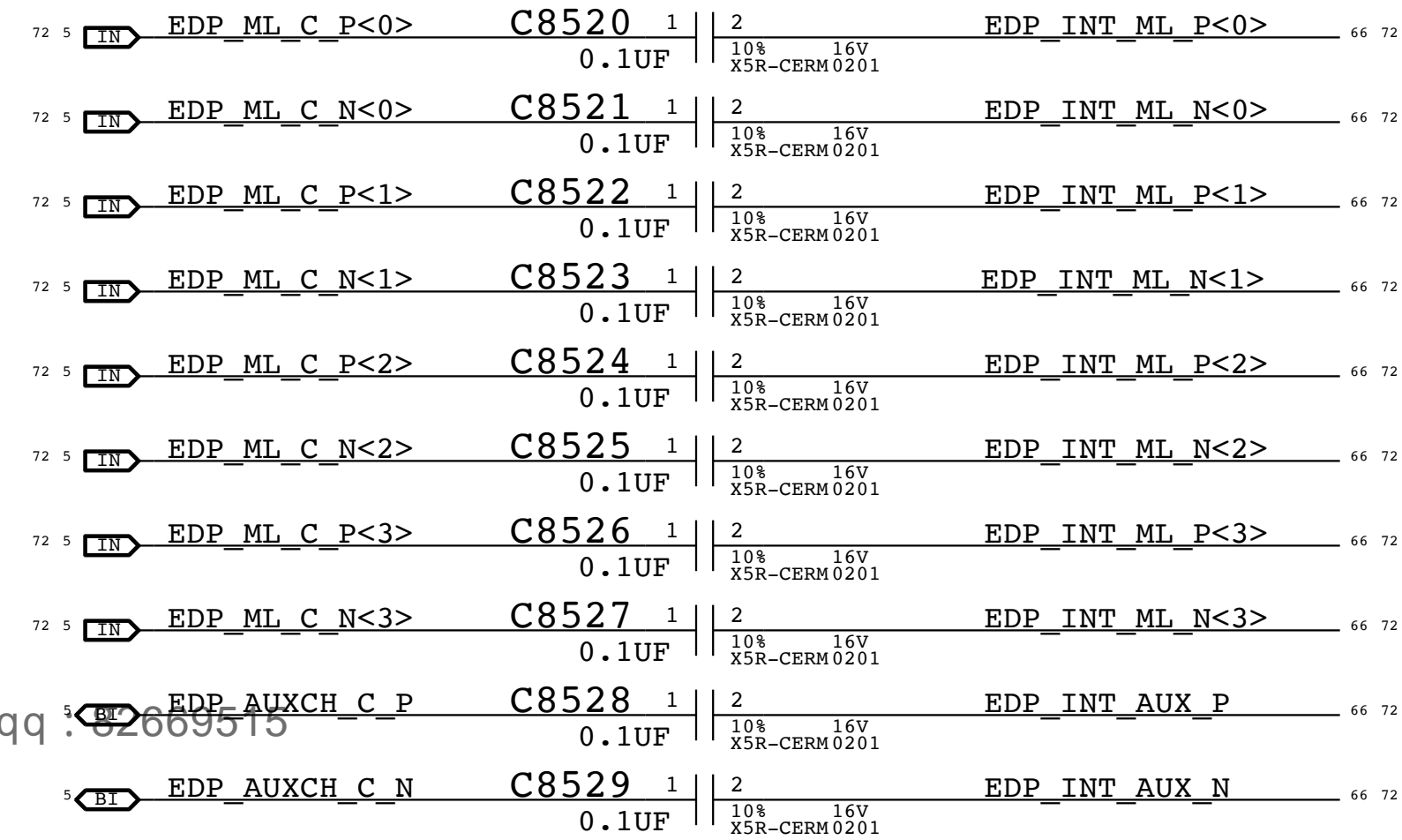
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BOM_COST_GROUP=DISPLAY

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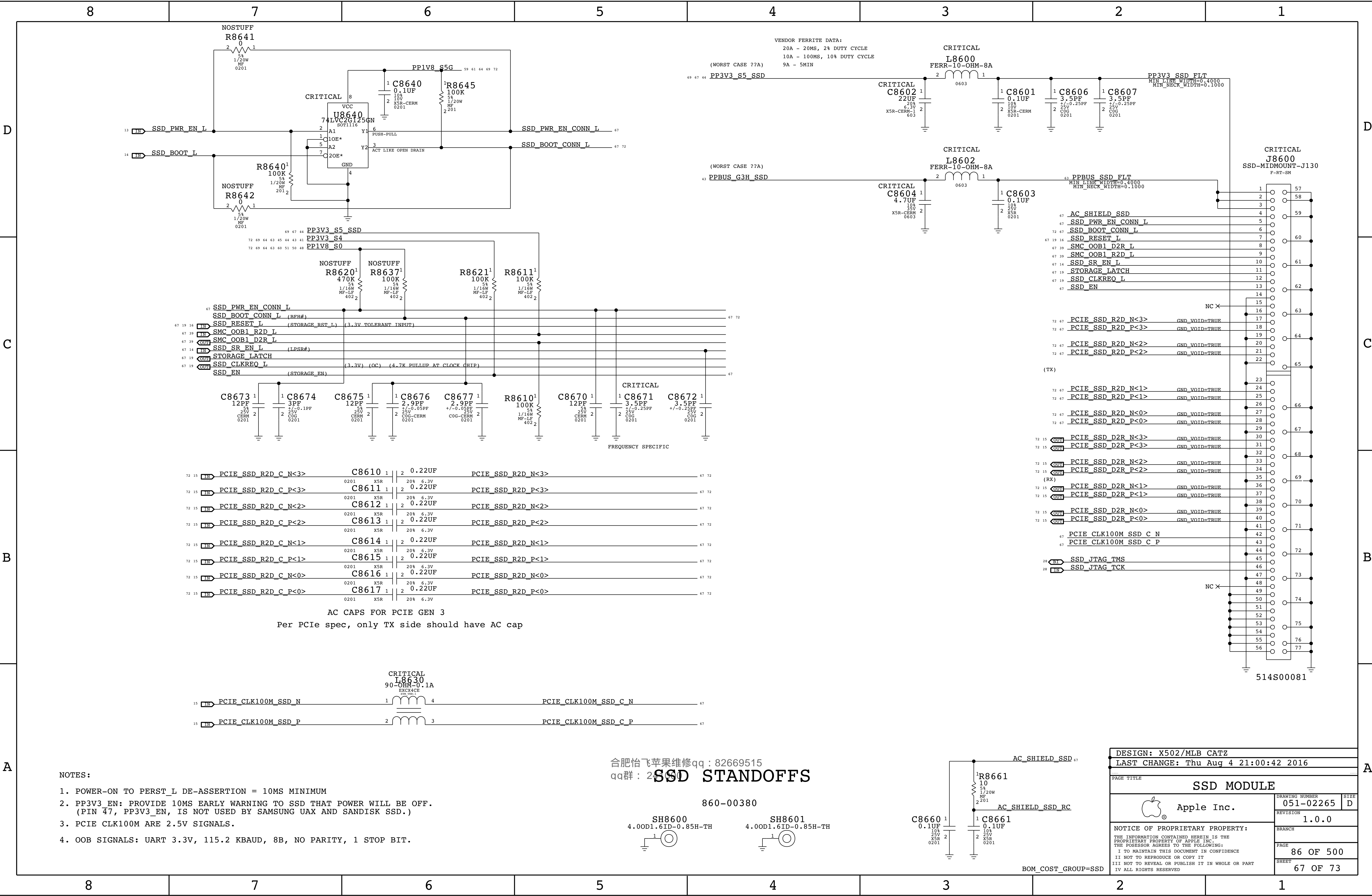
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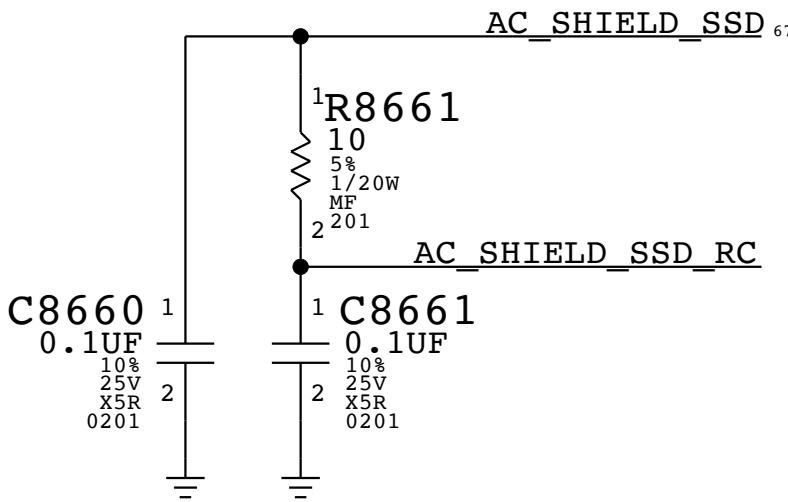
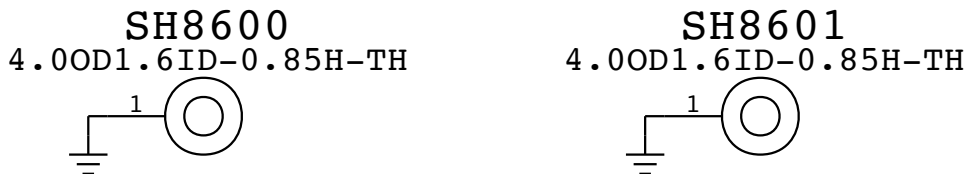


- NOTES:
- POWER-ON TO PERST_L DE-ASSERTION = 10MS MINIMUM
 - PP3V3_EN: PROVIDE 10MS EARLY WARNING TO SSD THAT POWER WILL BE OFF. (PIN 47, PP3V3_EN, IS NOT USED BY SAMSUNG UAX AND SANDISK SSD.)
 - PCIE CLK100M ARE 2.5V SIGNALS.
 - OOB SIGNALS: UART 3.3V, 115.2 KBAUD, 8B, NO PARITY, 1 STOP BIT.


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qq群 : 245555555

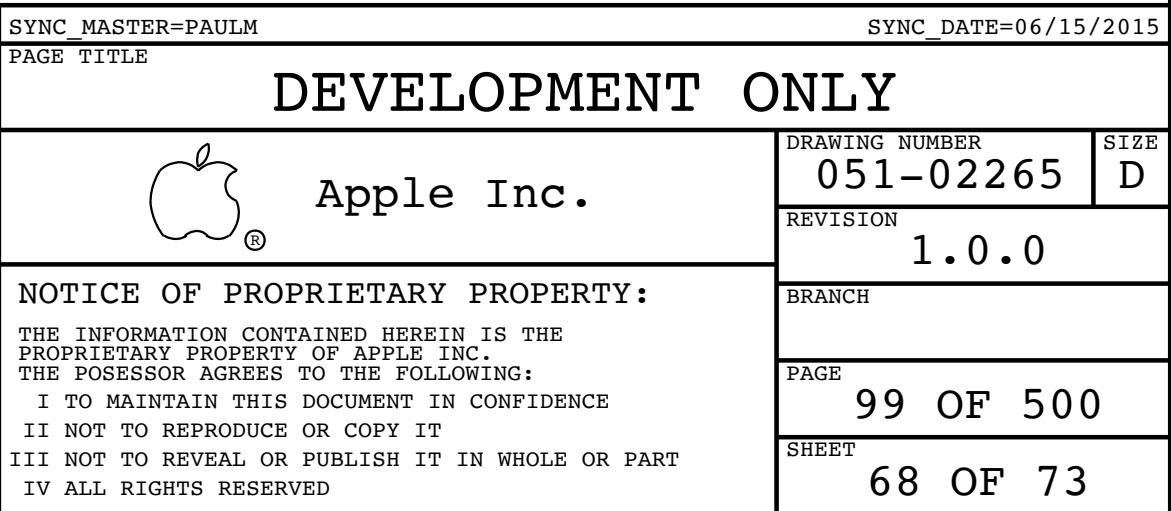
SSD STANDOFFS

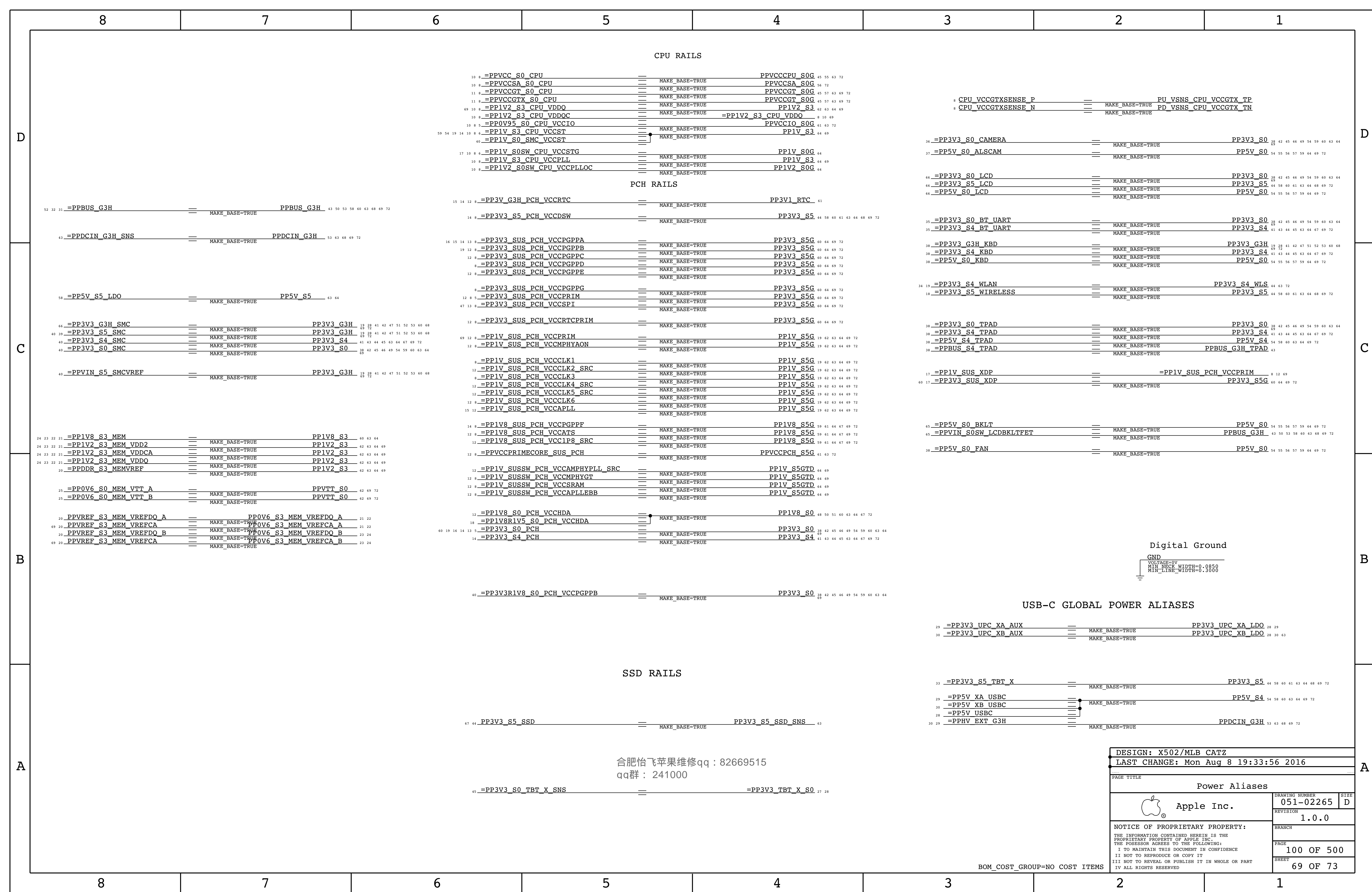
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D	Memory Bit/Byte Swizzle														D											
	CPU							DRAM																		
	MAKE_BASE							MAKE_BASE																		
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