

BOM Groups

BOM GROUP	BOM OPTIONS
J44_COMMON	ALTERNATE,COMMON,J44_COMMON1,J44_COMMON2,J44_COMMON3,J44_COMMON4,J44_PROGPARTS
J44_COMMON1	TBTHV:P15V,SKIP_5V3V3:AUDIBLE,SPI:DUAL_IO
J44_COMMON2	EDP,EDP_LS_CAP,CAMERA_3V3:S0,CAM_WAKE:NO,CAM_XTAL:NO,MEM_ODT:PU,VCORE_FETS
J44_COMMON3	XDP,LPCPLUS,BKLT:PROD,CPUHRM:ALRT,LOADRC:NO,OTHERRC:NO,DDRRC:NO,TBTRC:NO,BMONRC:NO
J44_PROGPARTS	SMC_PROG:PVT,BOOTROM:PVT,TBTROM:PVT,TPAD_PSOC:PROG
ENGISMS	LOADISMS,OTHERISMS,DDRISMS,TBTISMS,BMONISMS

Programmables (All Builds)

TBT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S3918	1	EPROM,FALCON RIDGE (V13.7) J44	U2890	CRITICAL	TBTROM:PVT

SMC

341S3922	1	IC,SMC-B1,EXT(V2.16F39),PVT,J44	U5000	CRITICAL	SMC_PROG:PVT
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EFI ROM

341S3924	1	IC,EFI ROM (V0116),PVT,J44	U6100	CRITICAL	BOOTROM:PVT
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PSOC

341S3862	1	IC,TRKPD/KYBD PSOC,CU ONLY(V224) J44	U4801	CRITICAL	TPAD_PSOC:PROG
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Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4596	1	HSWULT,SR18A,PRQ,C0,2,4,28W,2+3,3M,BGA	U0500	CRITICAL	CPU_HSW:2.4G
337S4597	1	HSWULT,SR189,PRQ,C0,2,6,28W,2+3,3M,BGA	U0500	CRITICAL	CPU_HSW:2.6G
338S4598	1	HSWULT,SR188,PRQ,C0,2,8,28W,2+3,4H,BGA	U0500	CRITICAL	CPU_HSW:2.8G
338S1247	1	IC,TBT,FR-4C,A0,PRQ,CIO,SR13JC,FCBGA288	U2800	CRITICAL	
338S1186	1	IC,BCM15700A2,S2 PCIE CAMERA PROCESSOR	U3900	CRITICAL	
376S1194	2	MOSFET,N-CH,30V,15.3A,12M,8P 3.3X3.3 DFN	Q7310,Q7320	CRITICAL	VCORE_FET:VSHY
376S1193	2	MOSFET,N-CH,30V,22A,6.0M,8P 3.3X3.3 DFN	Q7311,Q7321	CRITICAL	VCORE_FET:VSHY
376S0964	2	MOSFET,N-CH,25V,30A,9.6M,8P 3.3X3.3 DFN	Q7310,Q7320	CRITICAL	VCORE_FET:REN
376S1104	2	MOSFET,N-CH,25V,30A,6.1M,8P 3.3X3.3 DFN	Q7311,Q7321	CRITICAL	VCORE_FET:REN

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1053	376S0604		ALL	
128S0311	128S0329		ALL	
138S0739	138S0706		ALL	
197S0481	197S0480		ALL	
152S0461	152S1645		ALL	
376S1080	376S0820		ALL	
155S0667	155S0583		ALL	
138S0725	138S0724		ALL	
376S1032	376S0855		ALL	
376S1129	376S0855		ALL	
376S1089	376S1128		ALL	
353S3452	353S1286		ALL	
376S1180	376S0761		ALL	
128S0364	128S0264		ALL	
107S0254	107S0241		ALL	
138S0843	138S0674		ALL	
138S0803	138S0639		ALL	
138S0846	138S0811		ALL	
197S0542	197S0544		ALL	
197S0545	197S0544		ALL	
152S1876	152S1804		ALL	
107S0255	107S0240		ALL	
107S0250	107S0248		ALL	
127S0164	127S0162		ALL	
353S4070	353S4069		ALL	
353S4068	353S4069		ALL	
353S3814	353S3812		ALL	
311S0649	311S0541		ALL	
128S0436	128S0392		ALL	

Diodes alt to Fairchild
NEC alt to Sanyo
Samsung alt to Murata
Epson alt to NDK
Cyntec alt to Vishay
Diodes alt to On Semi
Panasonic alt to TDK
Samsung alt to Murata
Toshiba alt for Diodes Dual
NXP Alt for Diodes Dual
NXP Alt for Diodes Single
Maxim alt to Microchip
Renesas alt to Vishay
Sanyo 2nd Factory alt
Cyntec alt to TFT
Samsung alt to Murata (BKLT)
Samsung alt to Murata (BKLT)
Samsung alt to Murata (BKLT)
NDK alt to TXC
Epson alt to TXC
TDK alt to Toko
Cyntec alt to TFT
Cyntec alt to TFT
Rohm alt to Vishay
Pericom alt to TI DP Mux U9750
NXP alt to TI DP Mux U9750
TI alt to NXP
ONsemi alt to Toshiba
Kemet alt to Sanyo

STYC MASTER=214		STYC DATE=08/28/2011					
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		SHEET	2 OF 78				

DRAM SPD Straps

BOM GROUP	BOM OPTIONS
CAMDRAM:HYNIX_H	CAMDRAM_TYPE:HYNIX_H
CAMDRAM:ELPIDA	CAMDRAM_TYPE:ELPIDA
CAMDRAM:MICRON	CAMDRAM_TYPE:MICRON

DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0700	1	1C,SDRAM,4GBIT,DDR3L-1600,HUMA,96B FBGA	U4000	CRITICAL	CAMDRAM_TYPE:HYNIX_H
333S0704	1	1C,SDRAM,4GBIT,DDR3L-1600,DIE F,96B FBGA	U4000	CRITICAL	CAMDRAM_TYPE:ELPIDA
333S0698	1	1C,SDRAM,4GBIT,DDR3L-1600,REV E,96B FBGA	U4000	CRITICAL	CAMDRAM_TYPE:MICRON

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SYNC DATE=01/03/2013

BOM Configuration

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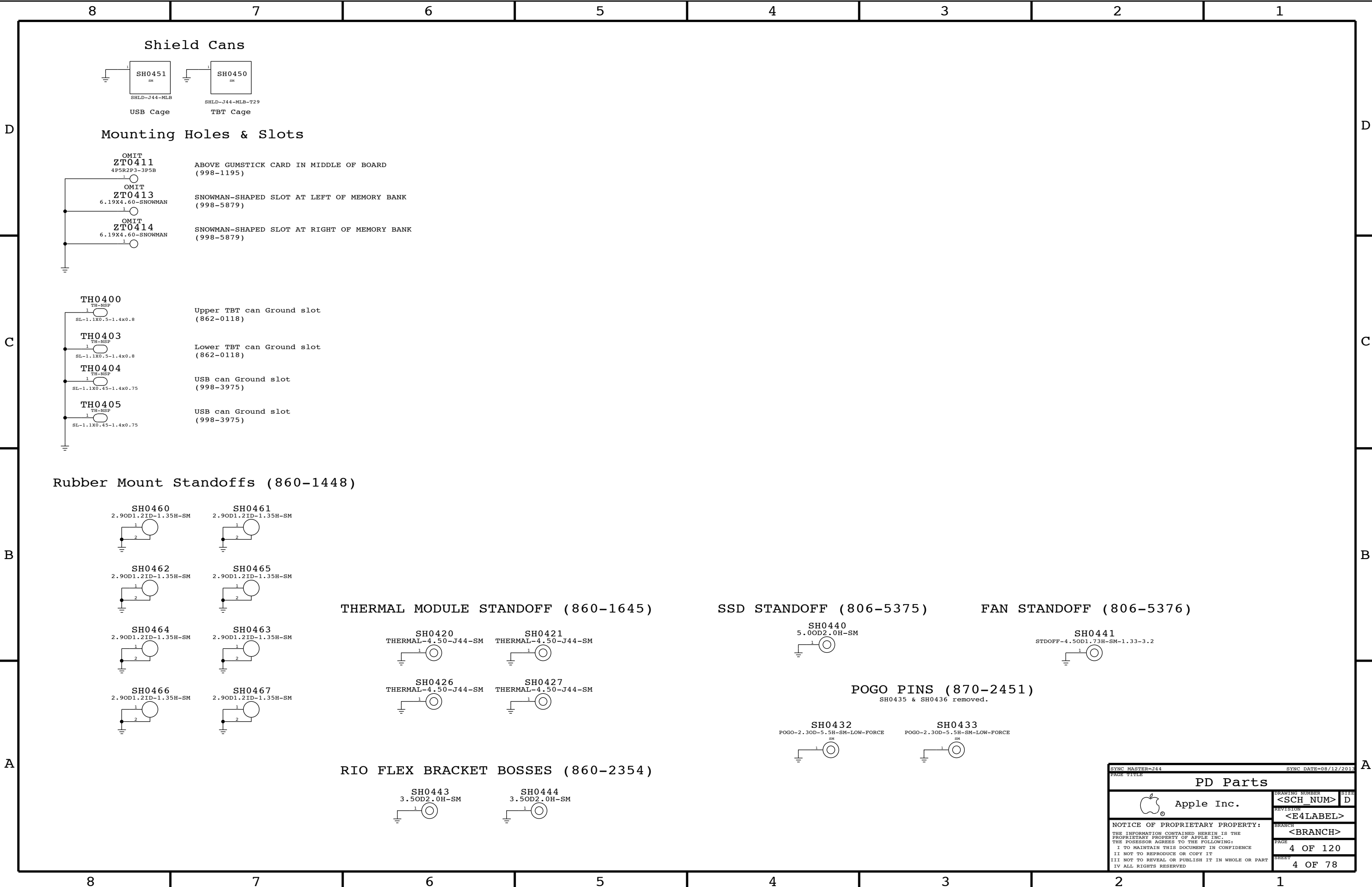
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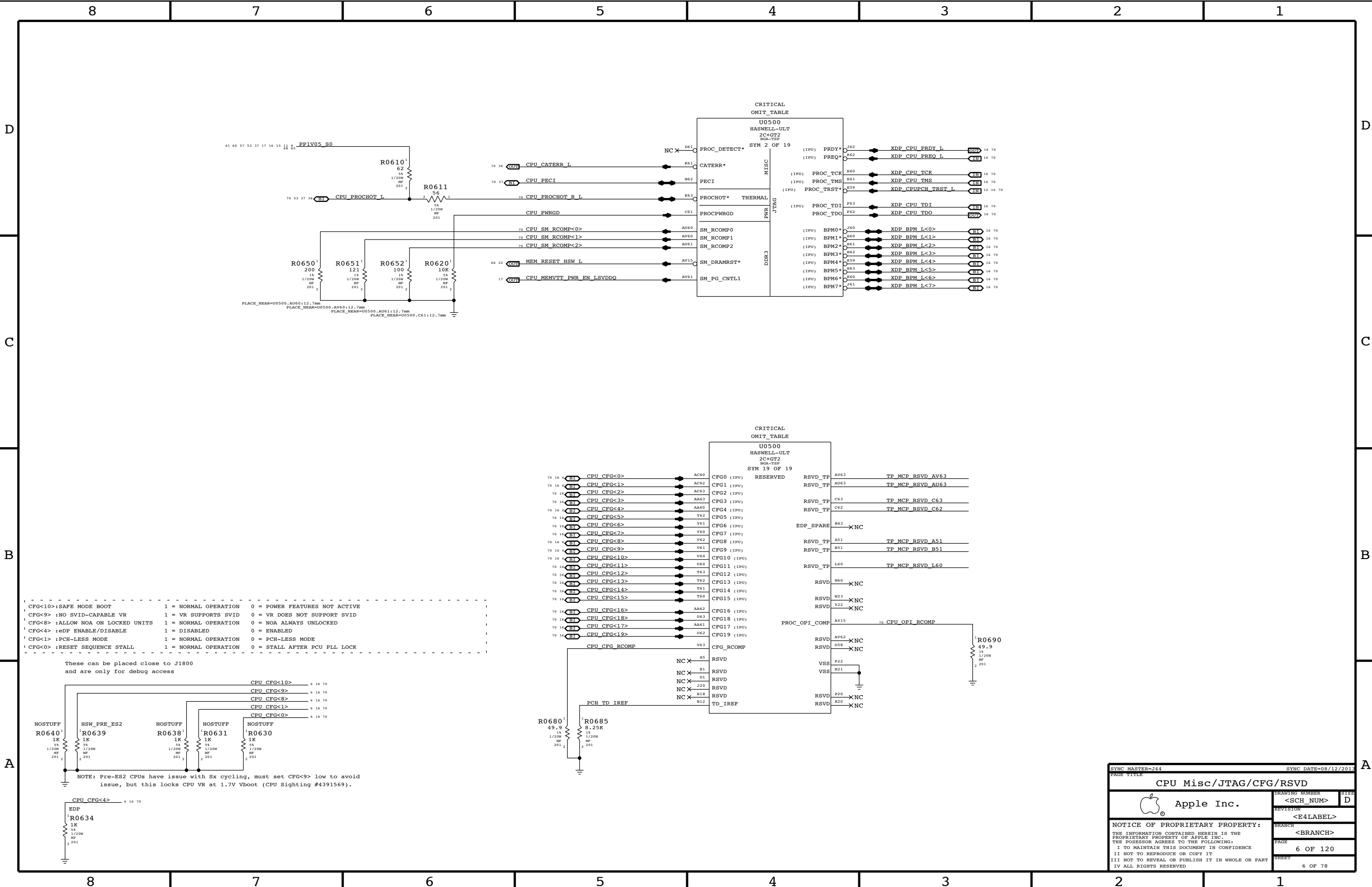
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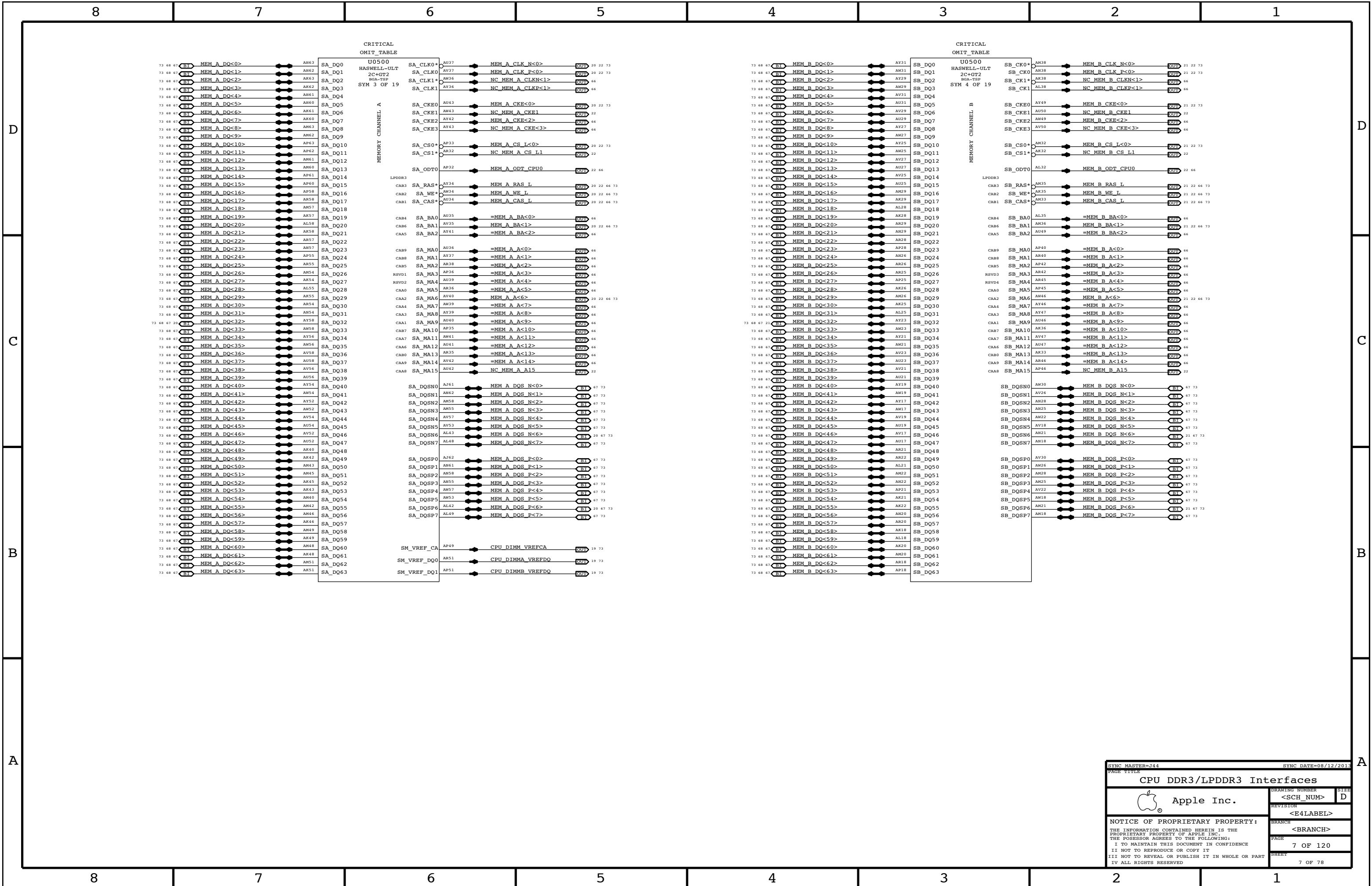
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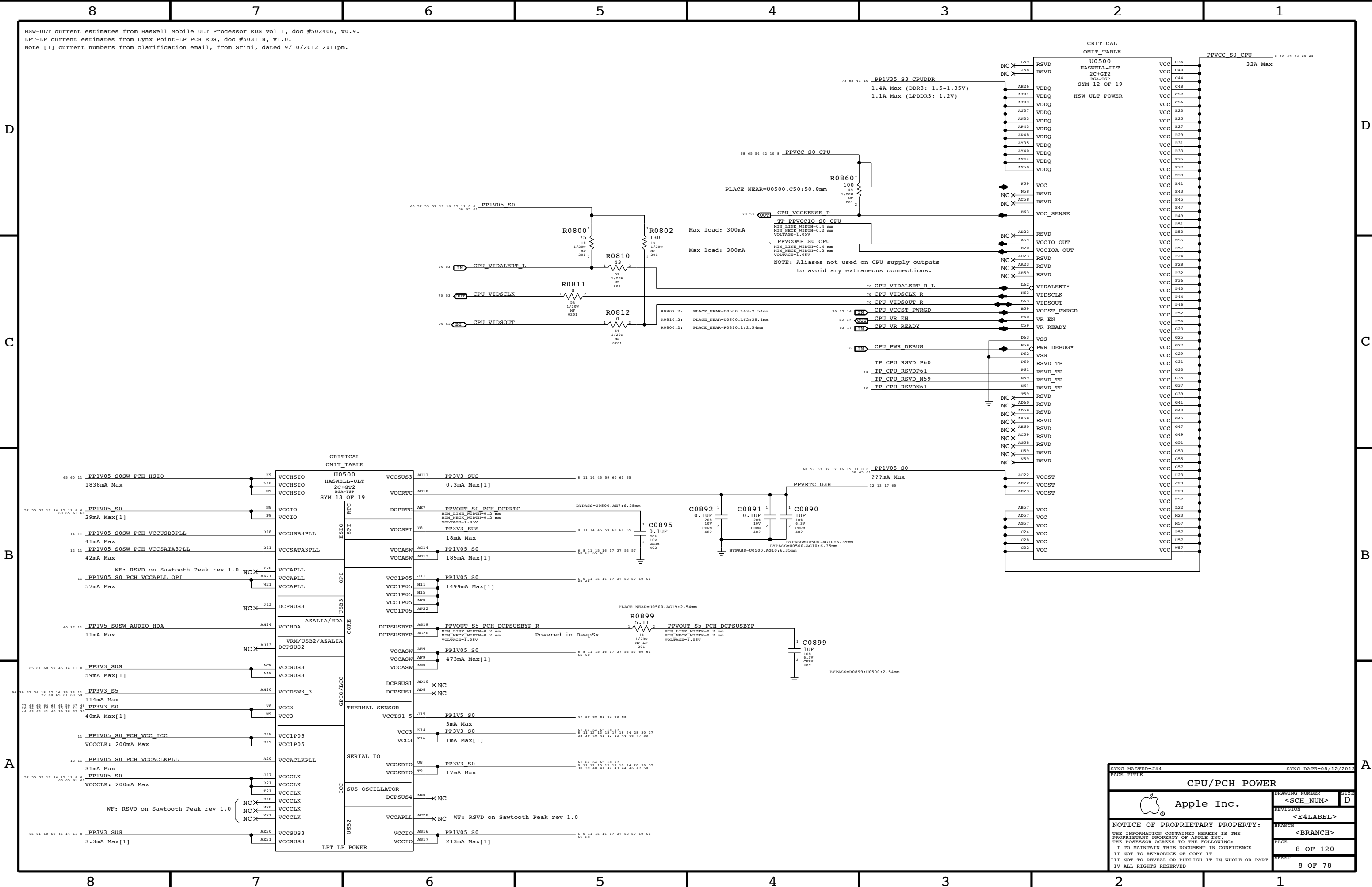
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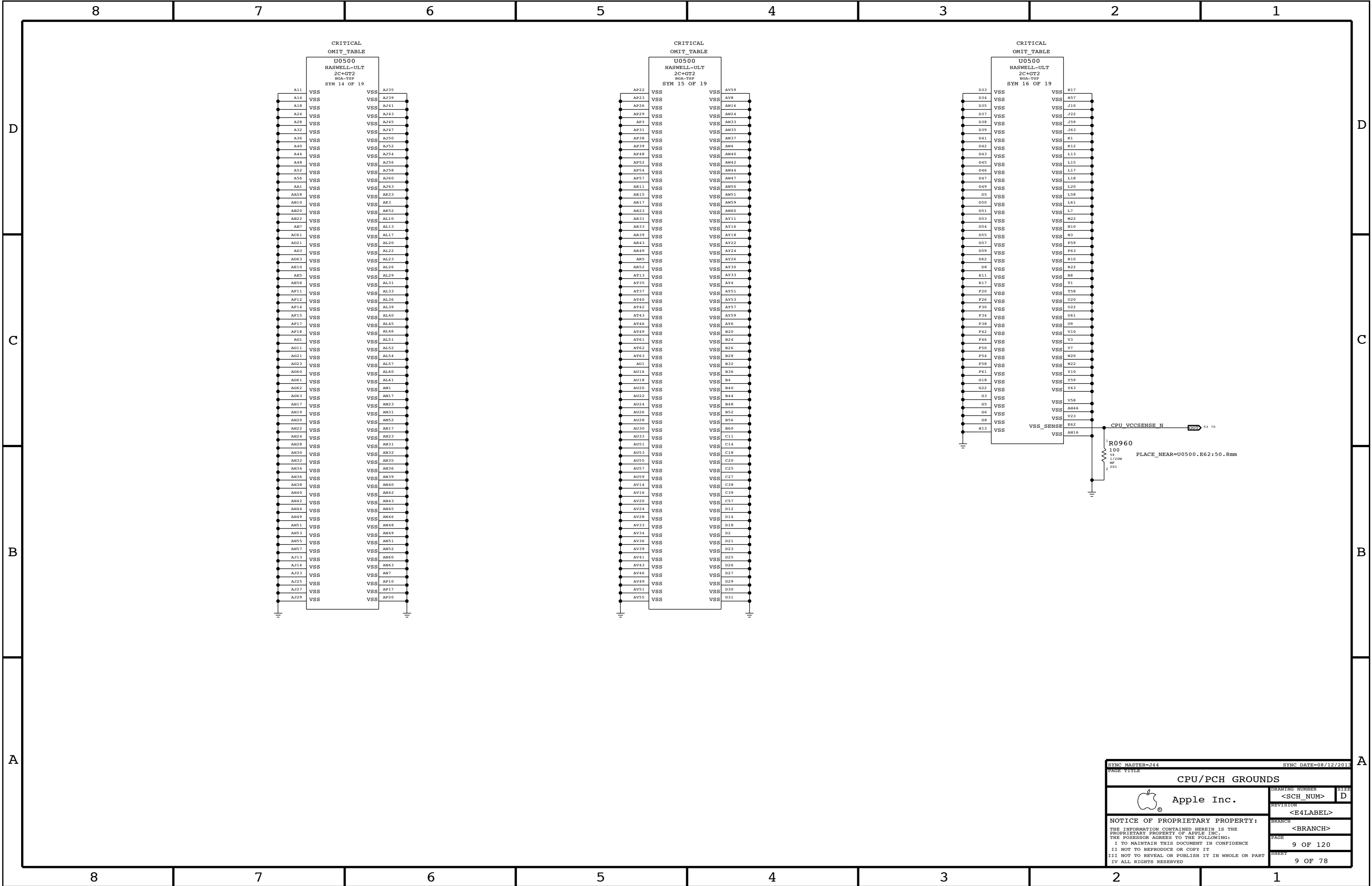


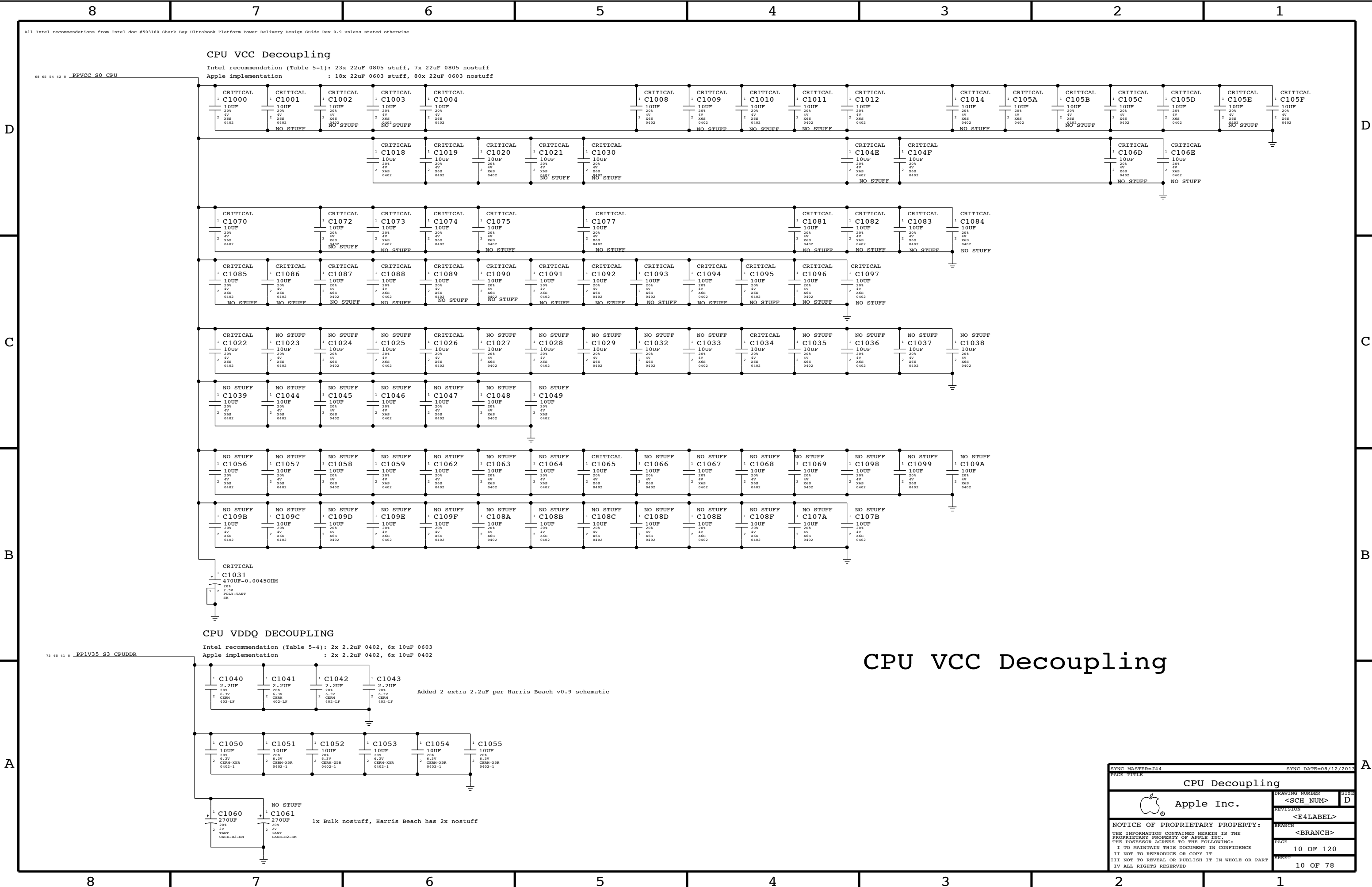
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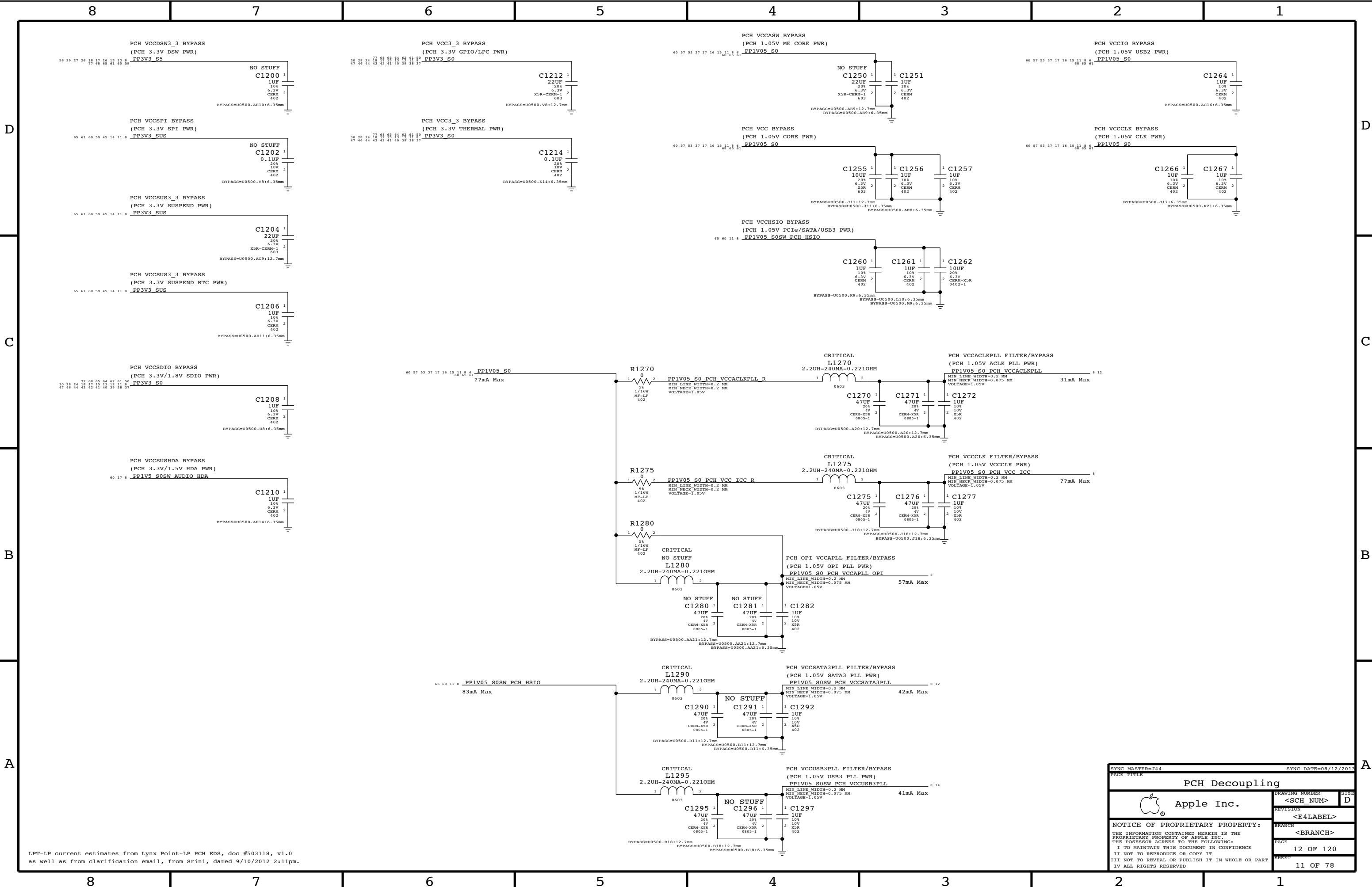






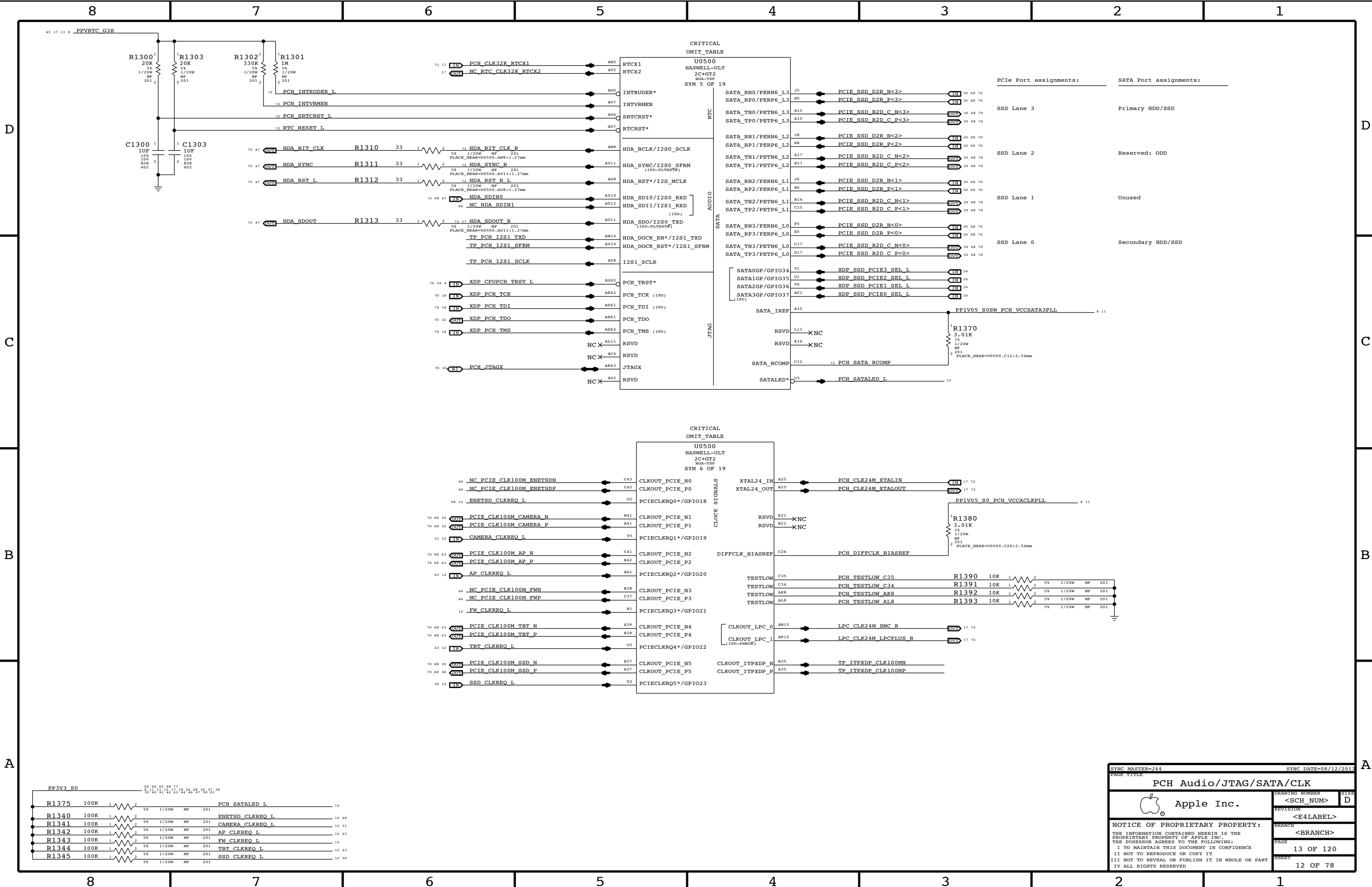


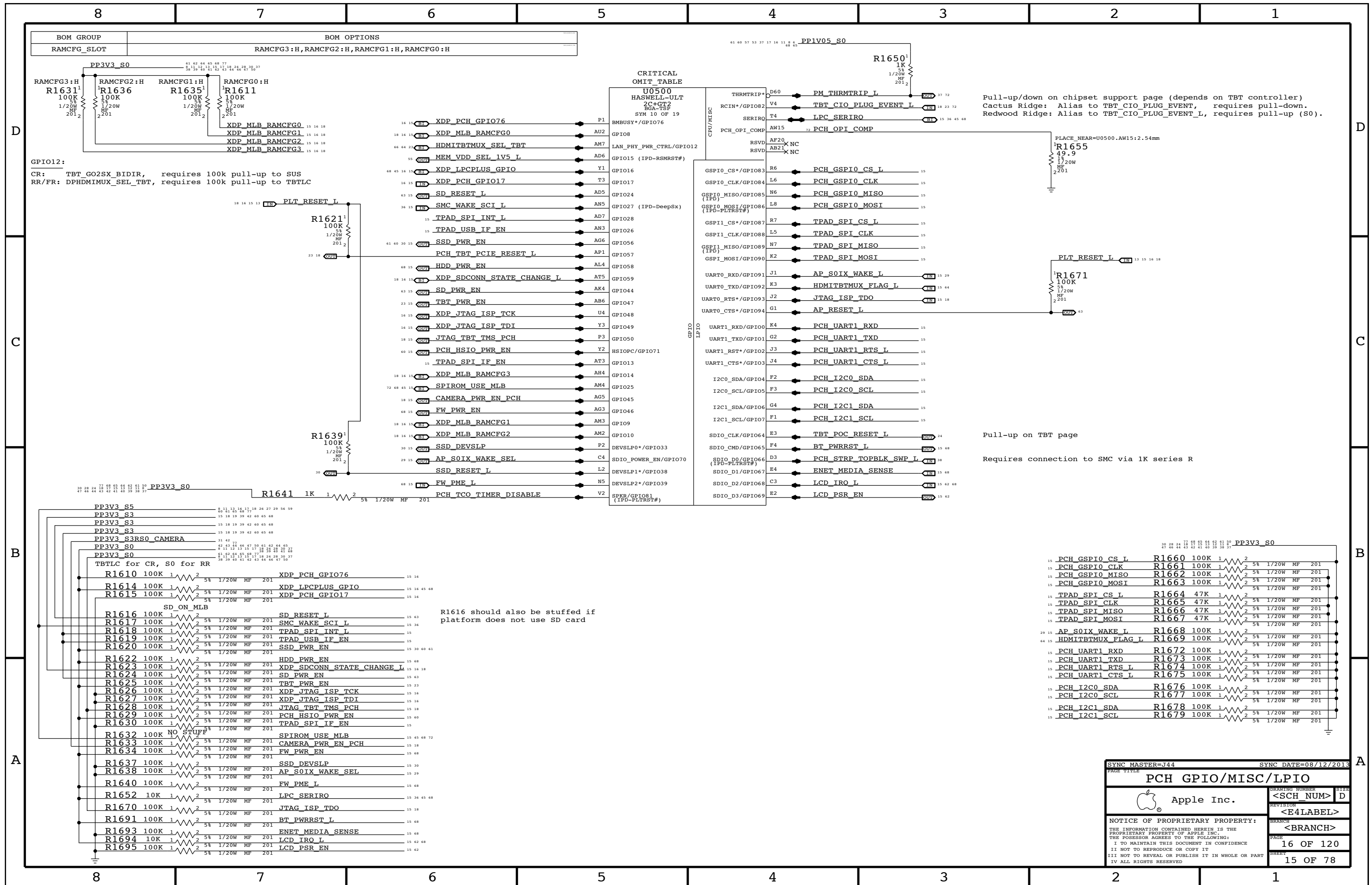
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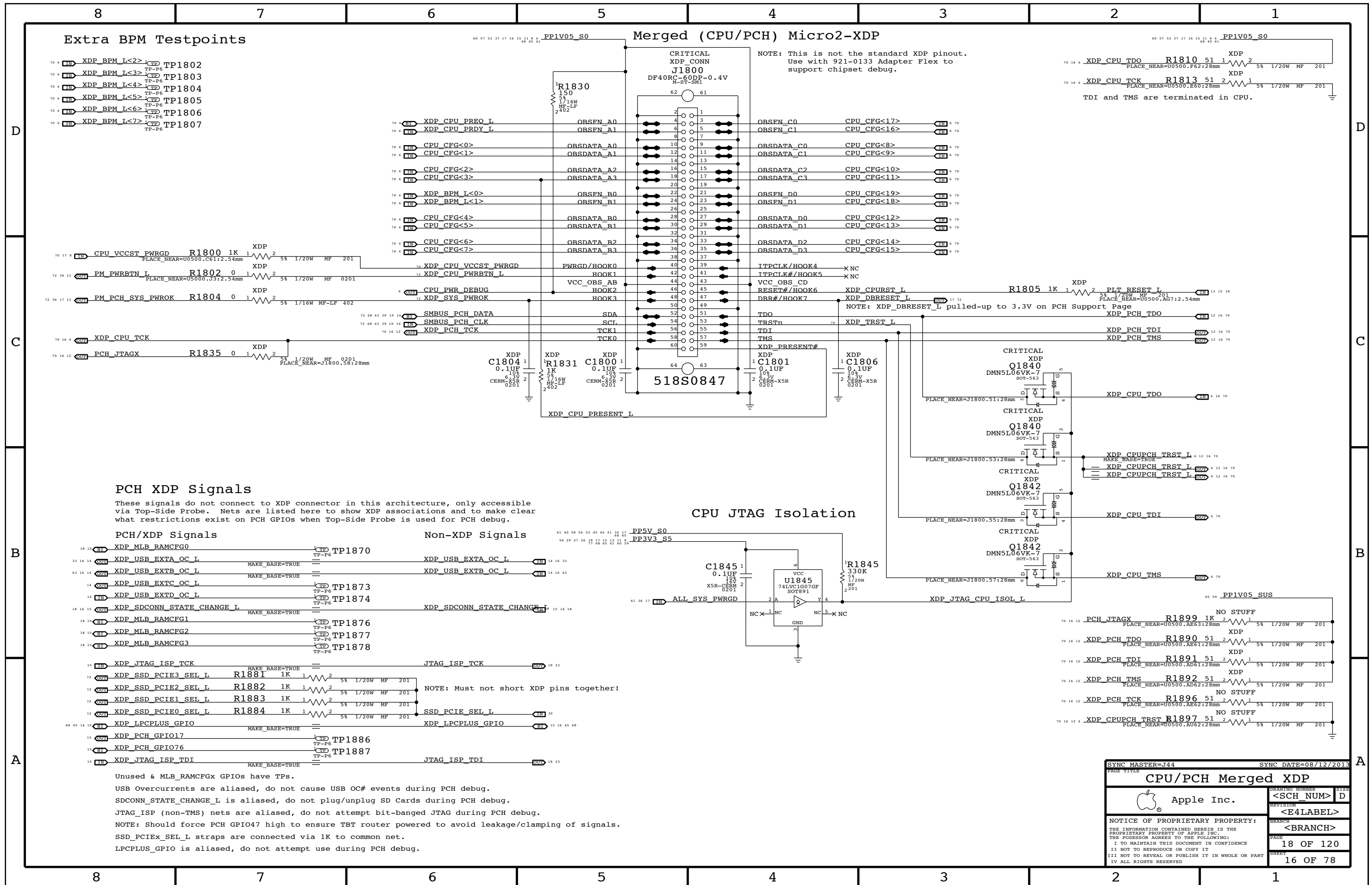


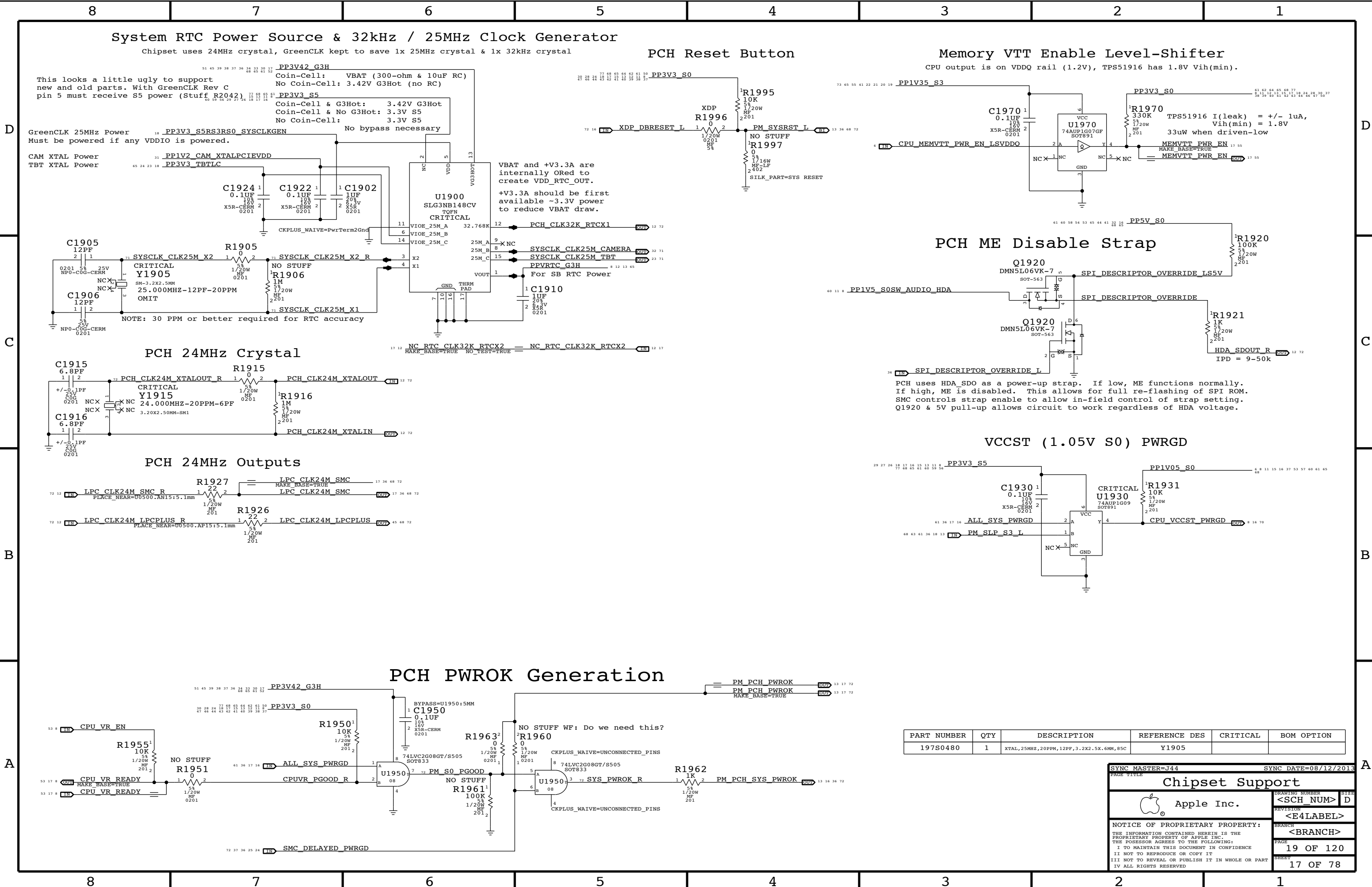
LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0
as well as from clarification email, from Sрни, dated 9/10/2012 2:11pm.

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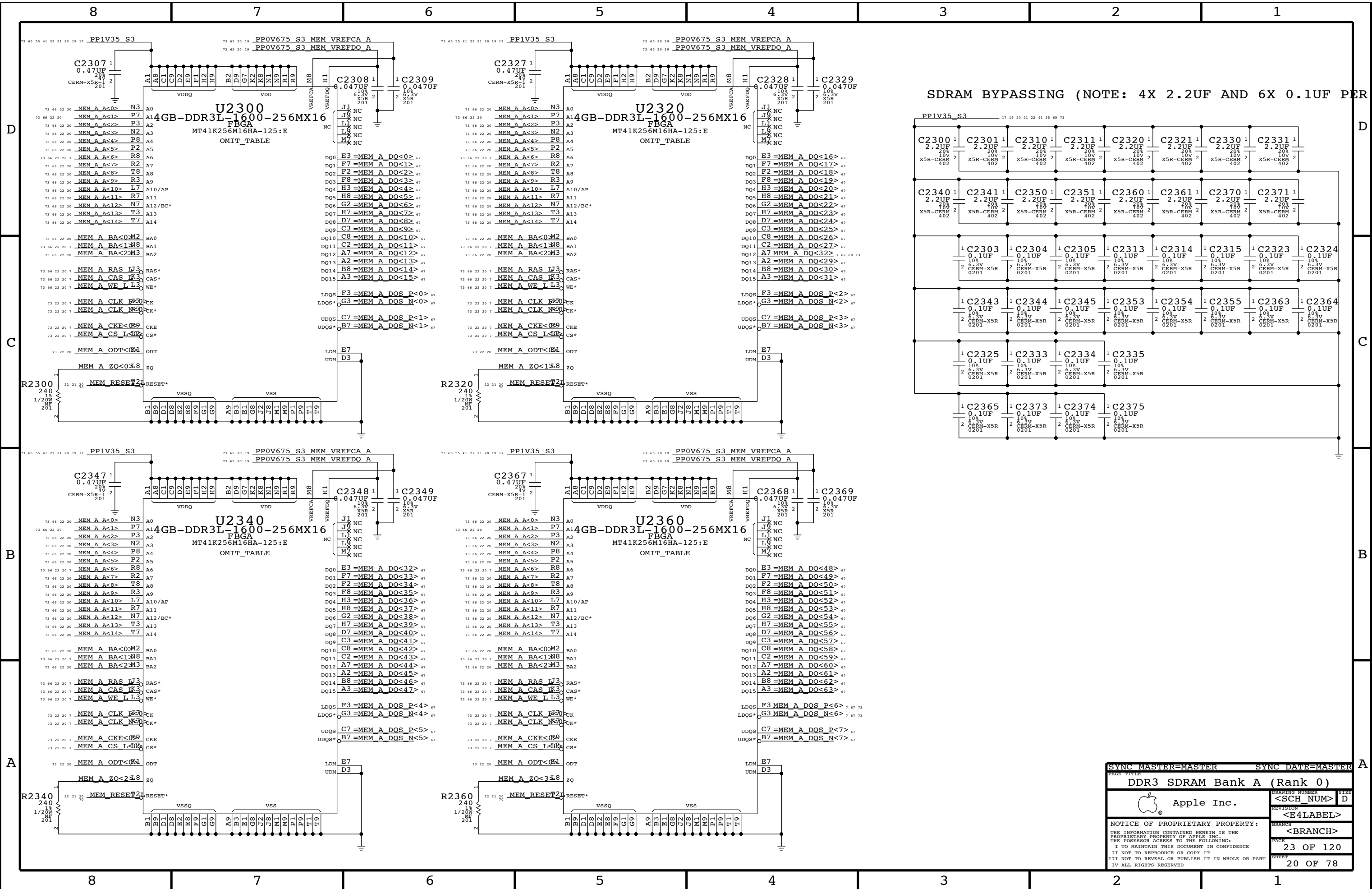





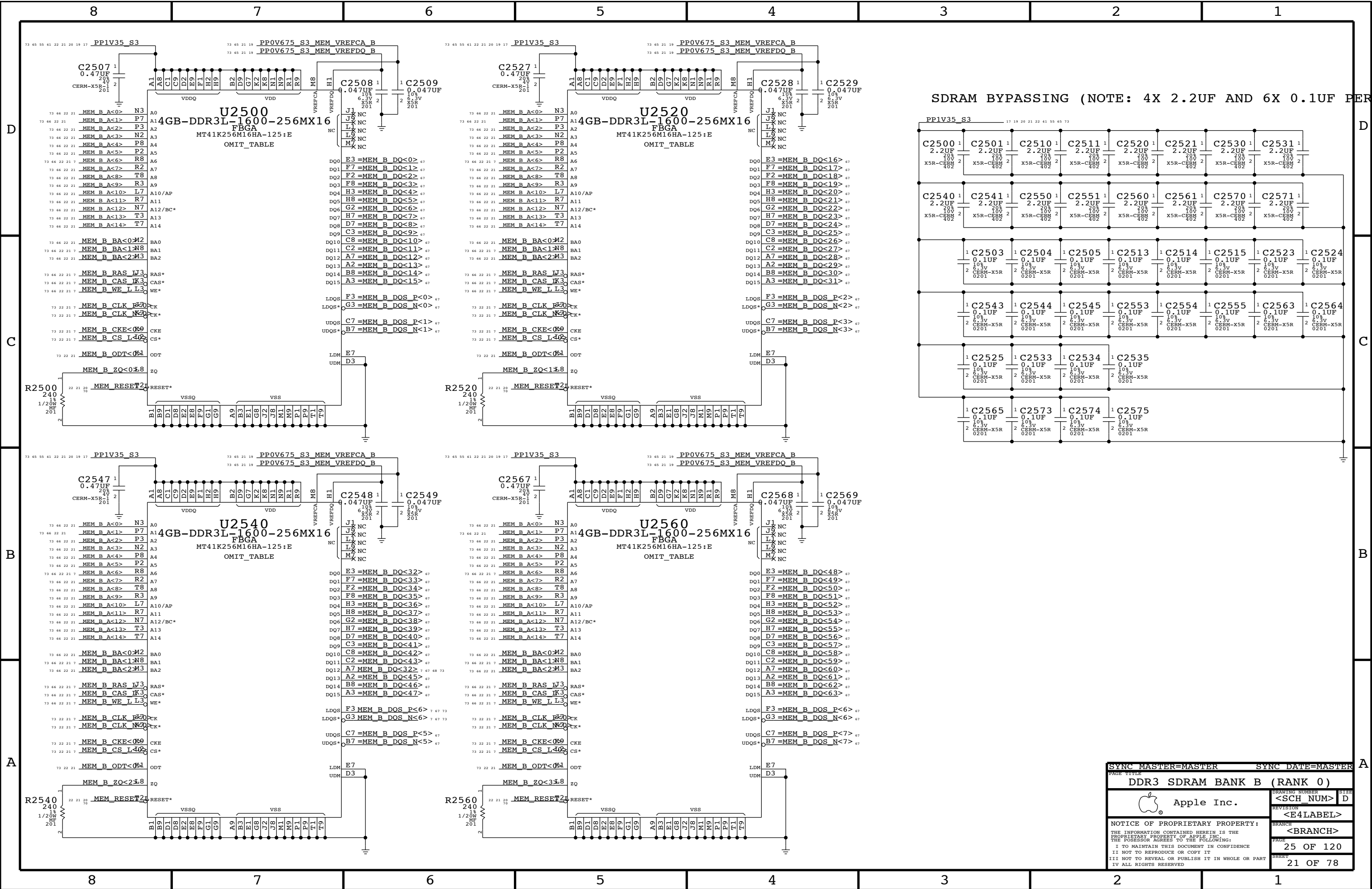


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
197S0480	1	XTAL, 25MHZ, 20PPM, 12PF, 3.2X2.5X.6MM, 85C	Y1905		

PAGE TITLE		PAGE TITLE	
Chipset Support		Chipset Support	
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DDR3 SDRAM Bank A (Rank 0)			
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DDR3 SDRAM BANK B (RANK 0)		<SCH_NUM>	
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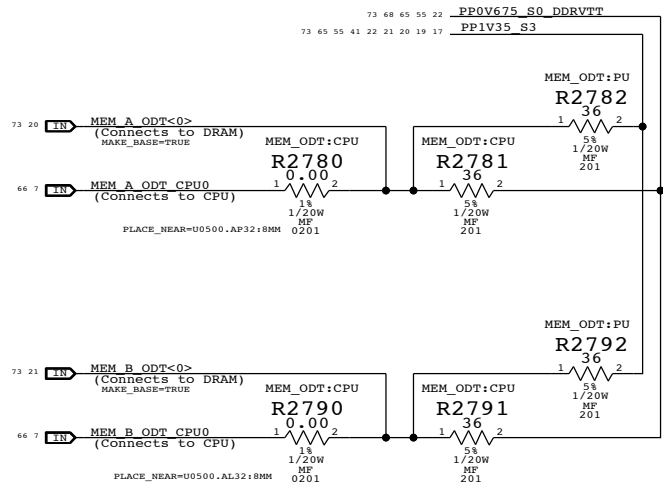
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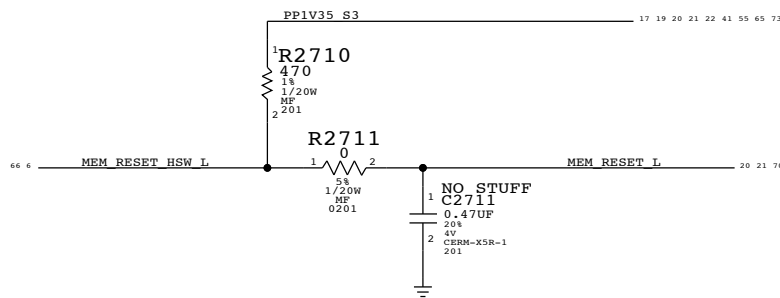
Memory ODT Option

MEM_ODT:CPU drives ODT from CPU, terminated to 0.675V VTT.
MEM_ODT:PU disconnect ODT from CPU, ODT pins on DRAM pulled up to 1.35V VDDQ.



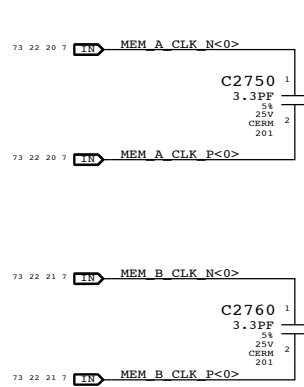
Memory Reset Pull Up

Reset is an open drain in Haswell ULT and needs pull up



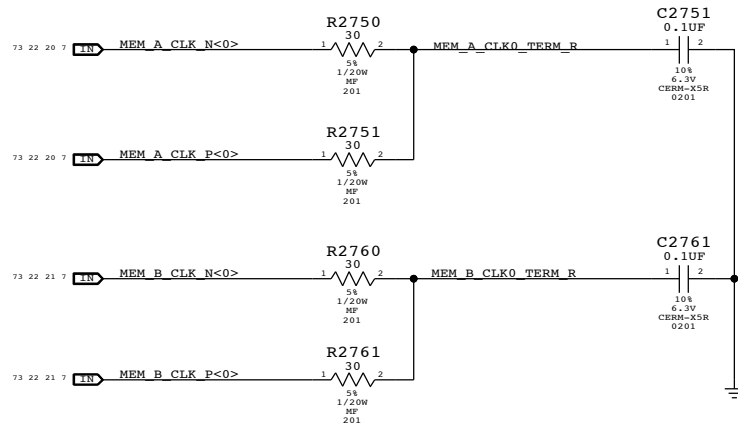
Memory Clock Near-End Termination

Place Source C termination before first DRAM

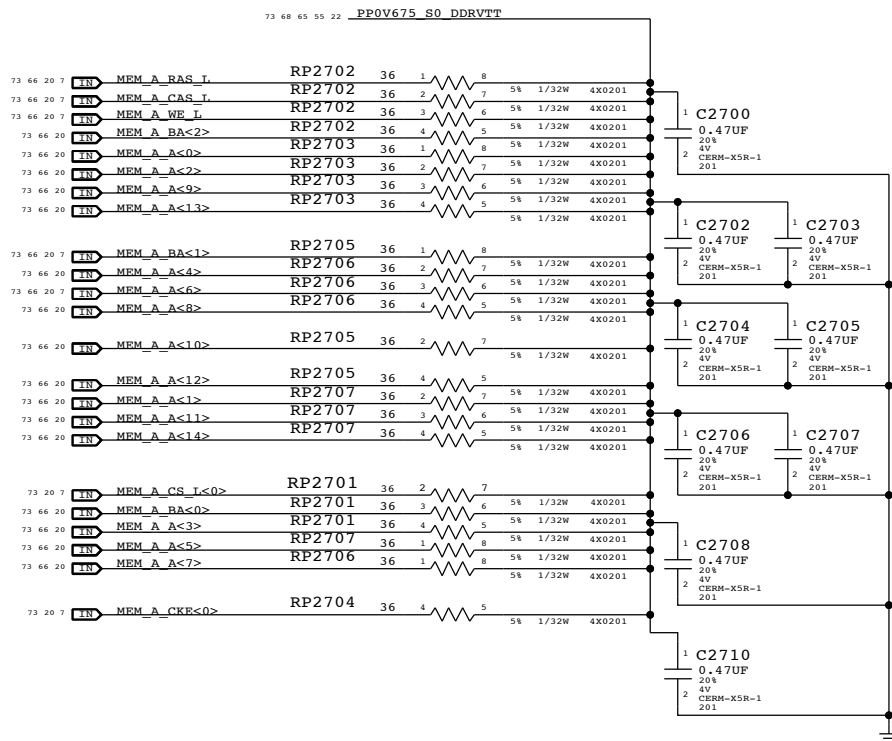


Memory Clock Far-End Termination

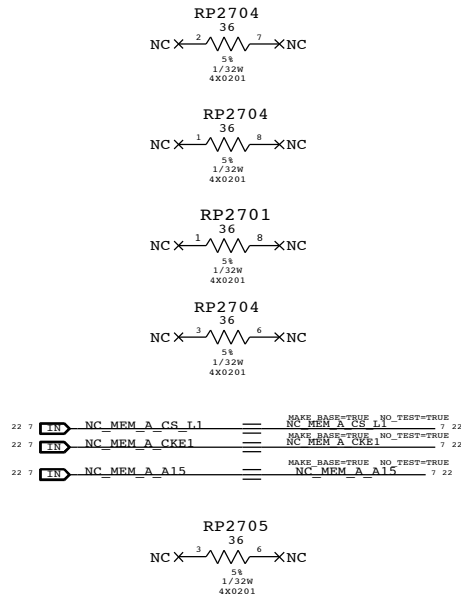
Place RC end termination after last DRAM



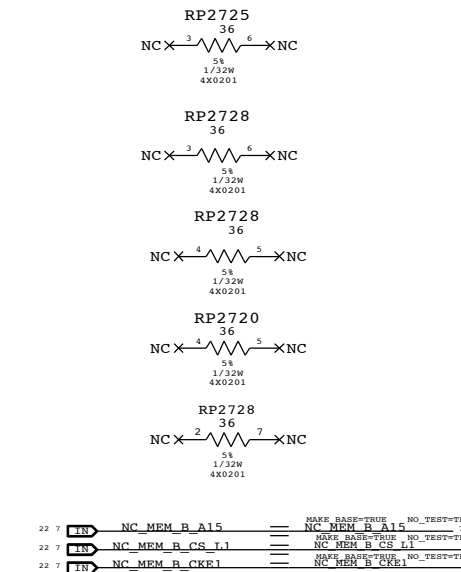
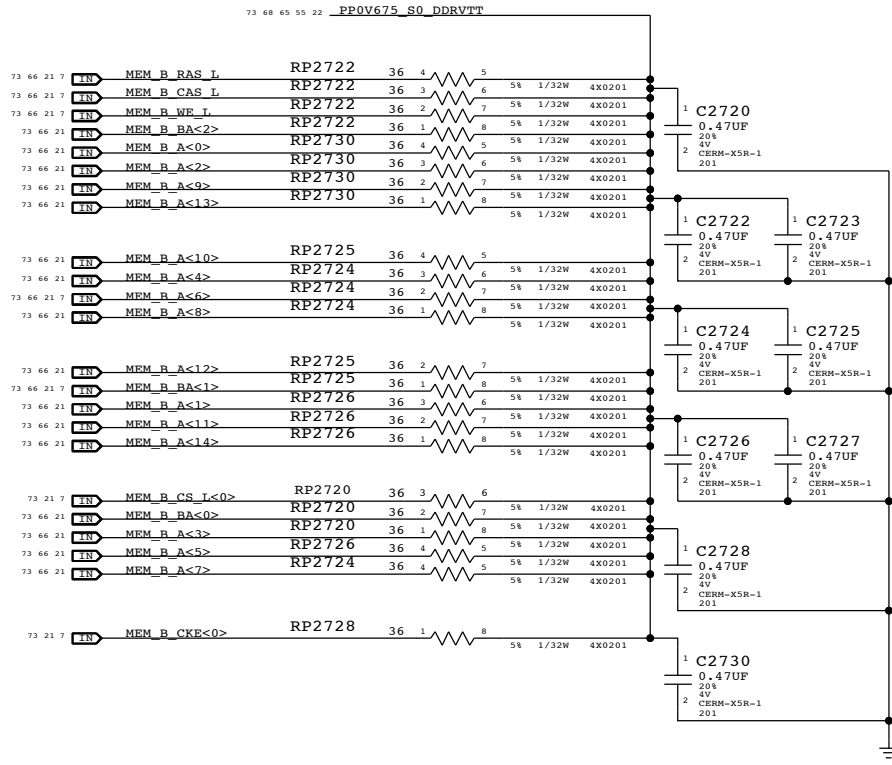
Memory CMD/CTL Termination - Channel A



MEMORY RPACK SPARES

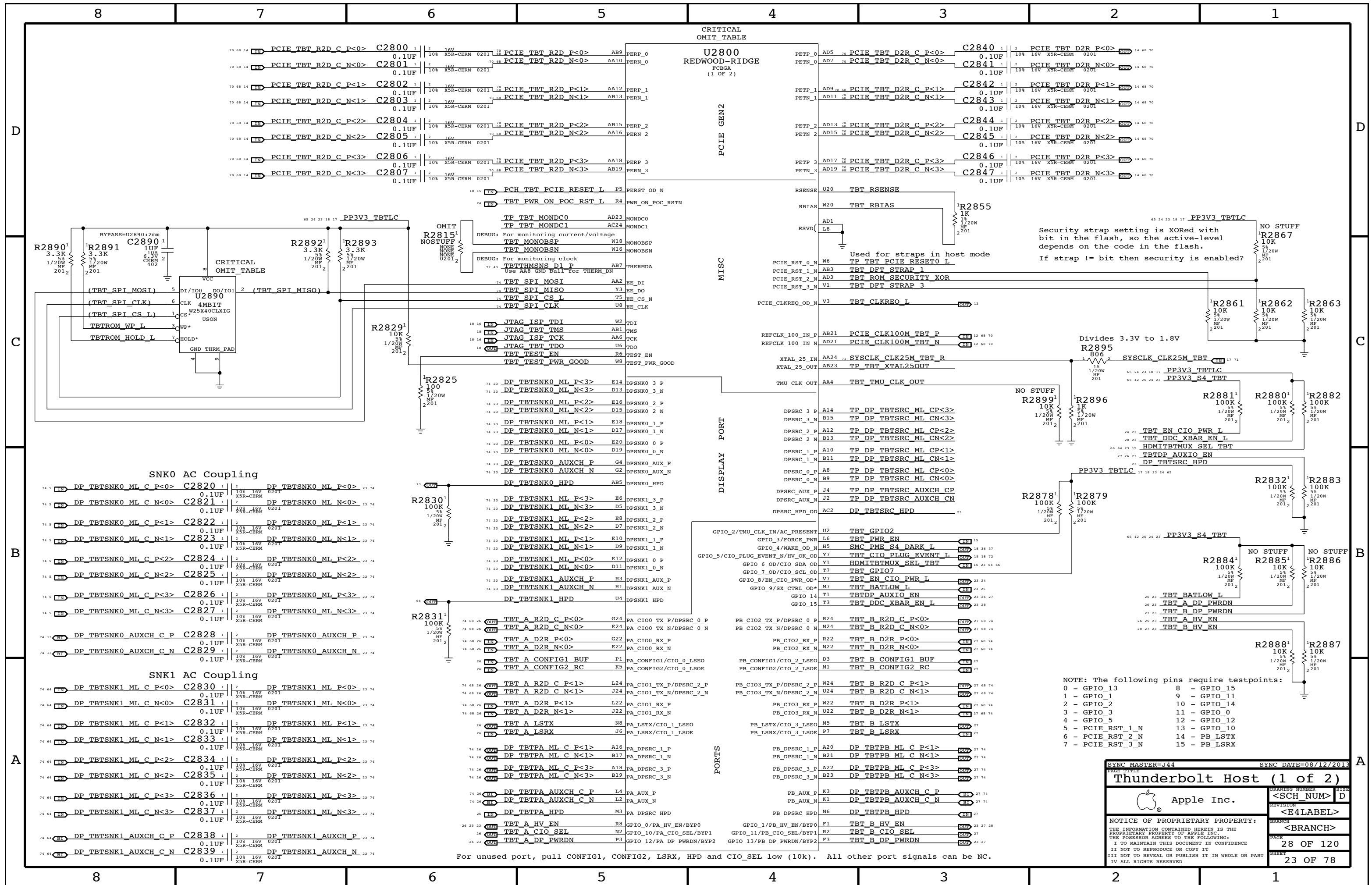


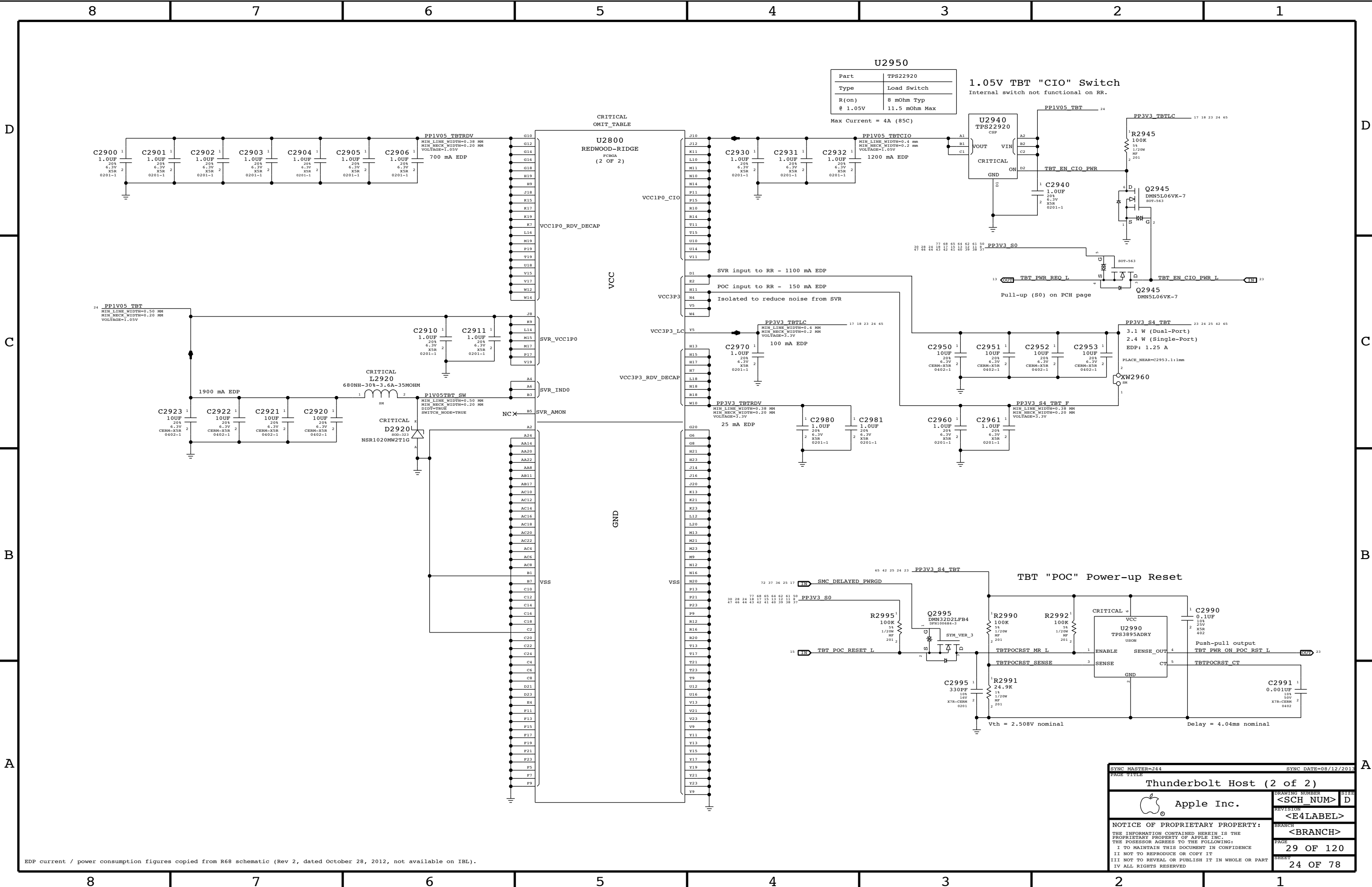
Memory CMD/CTL Termination - Channel B



SYNC MASTER=J44 YONAS-4GB SYNC DATE=04/02/2013


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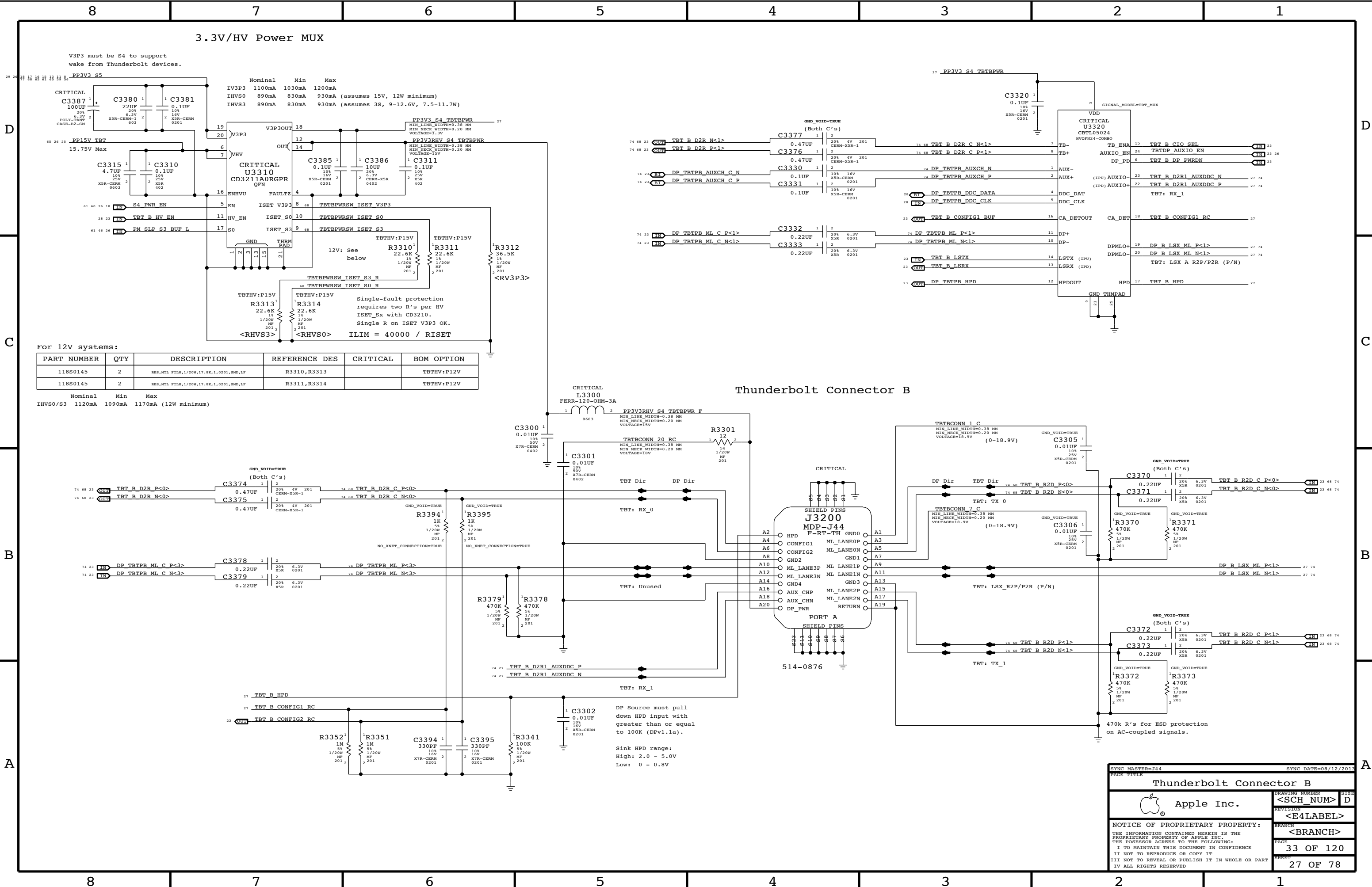


U2950	
Part	TPS22920
Type	Load Switch
R(on)	8 mOhm Typ
@ 1.05V	11.5 mOhm Max
Max Current = 4A (85C)	

1.05V TBT "CIO" Switch
Internal switch not functional on RR.

SYNC MASTER=J44		SYNC DATE=08/12/2013	
PAGE TITLE			
Thunderbolt Host (2 of 2)			
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EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).



D

C

B

A

D

C

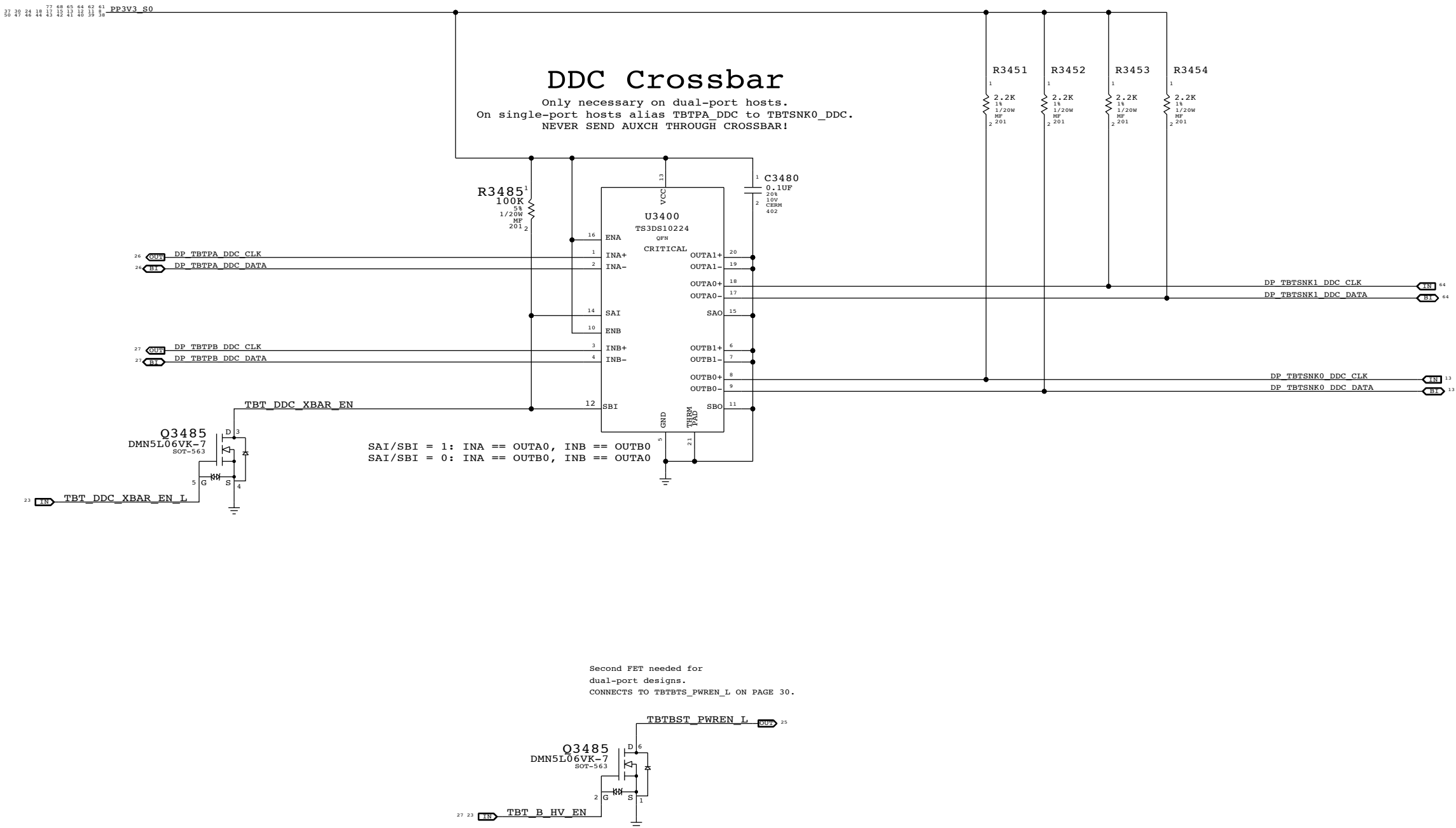
B


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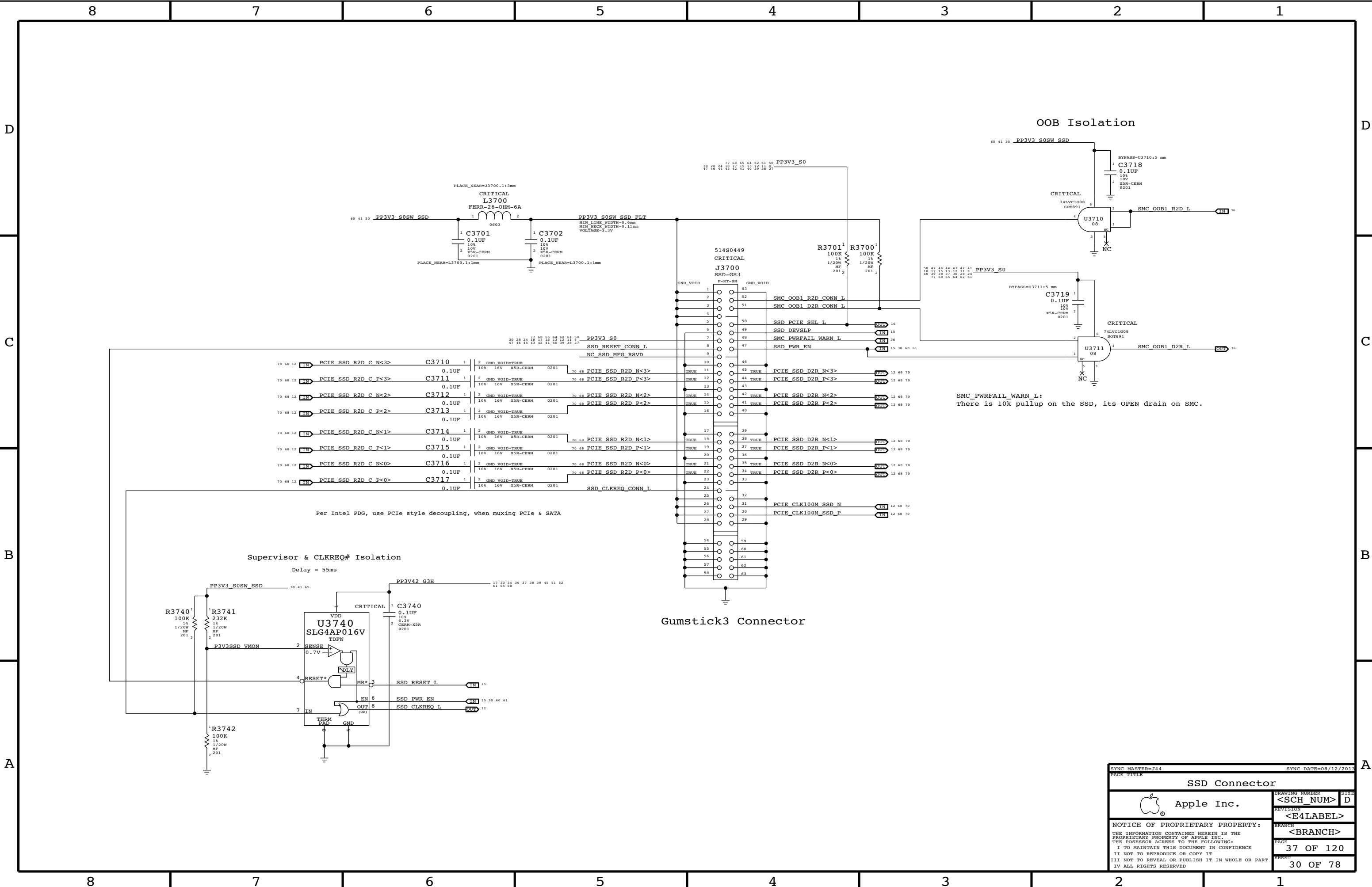
DDC Pull-Ups

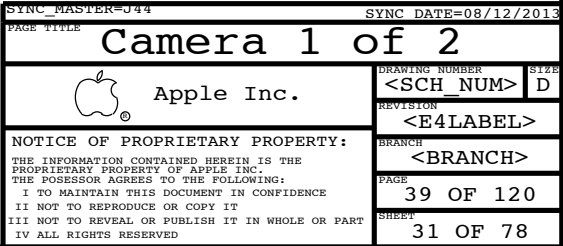
2.2k pull-ups are required by PCH to indicate active display interface.
DP++ spec violation, should remove!

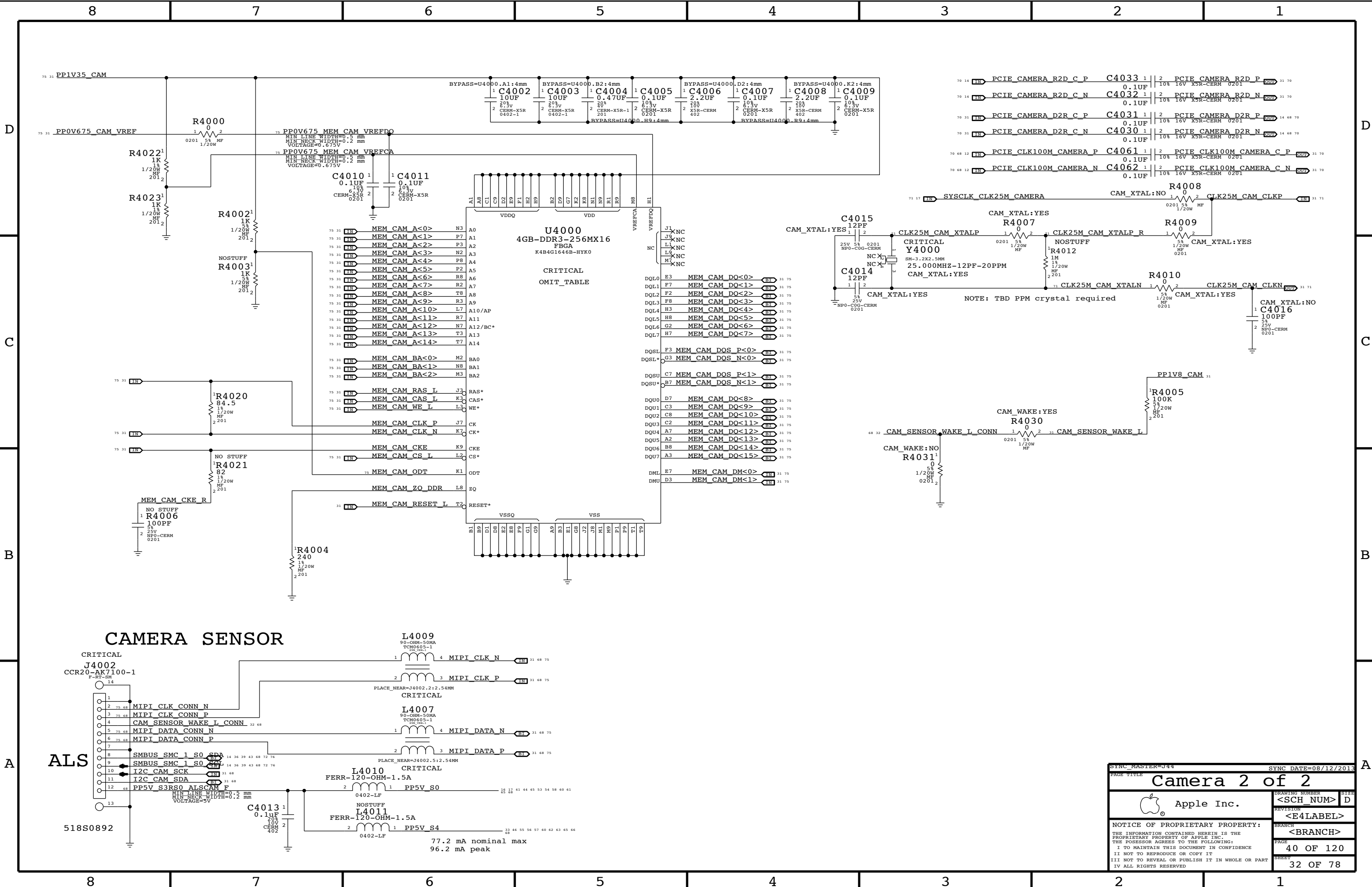
NOTE: Only DDC_DATA is sensed, so DDC_CLK pull-ups are unstuffed.

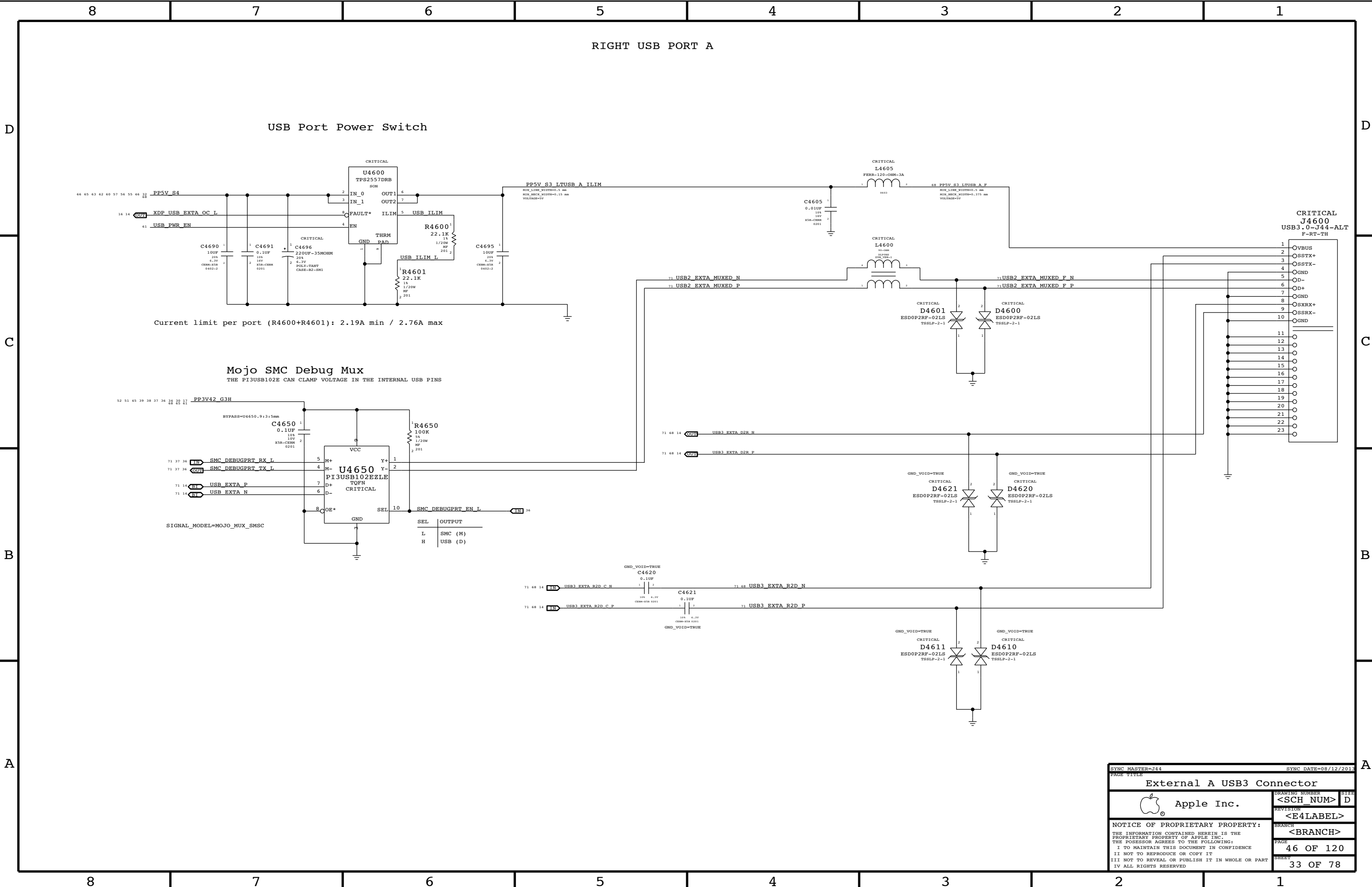


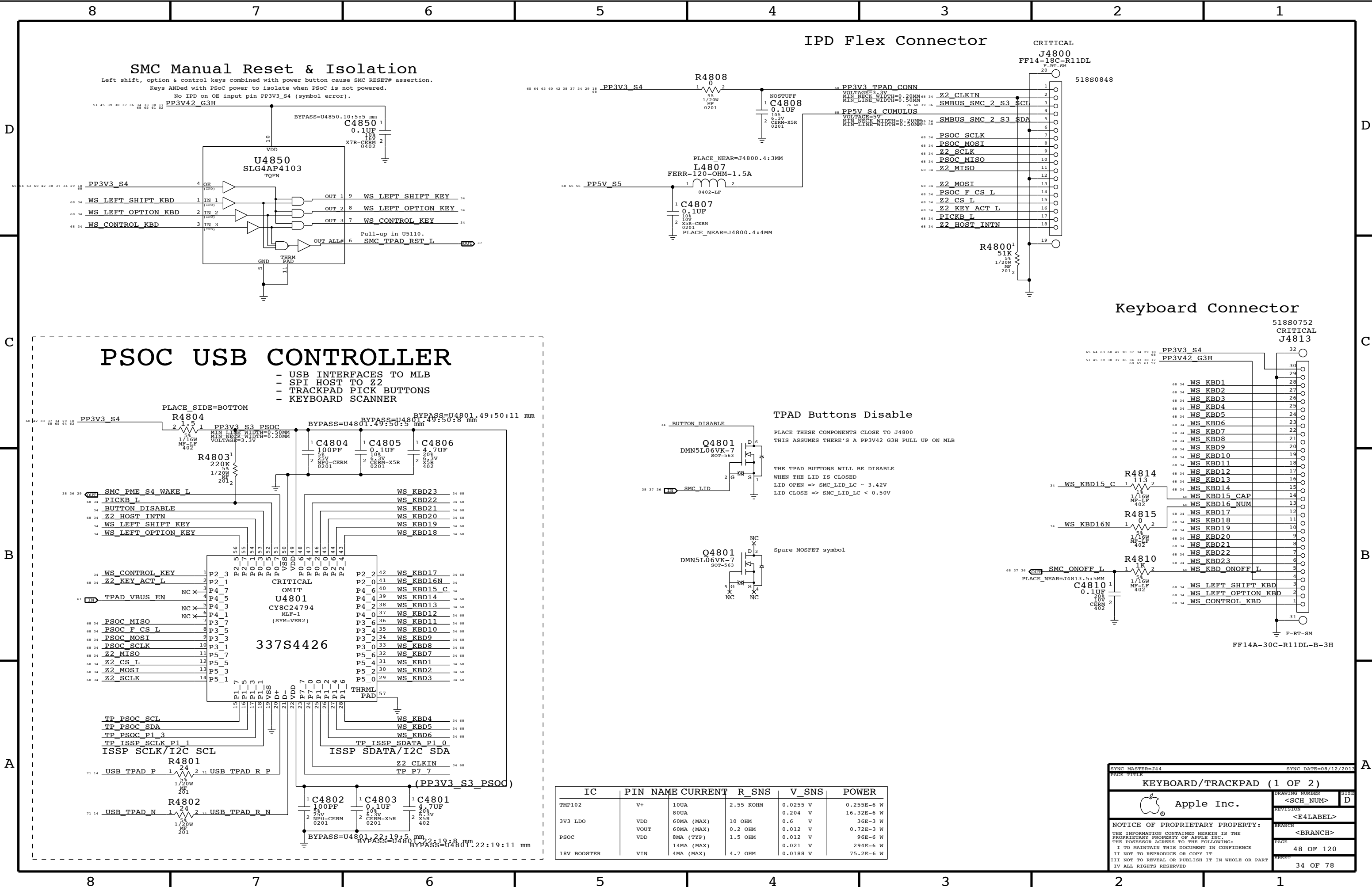
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DDC Crossbar			
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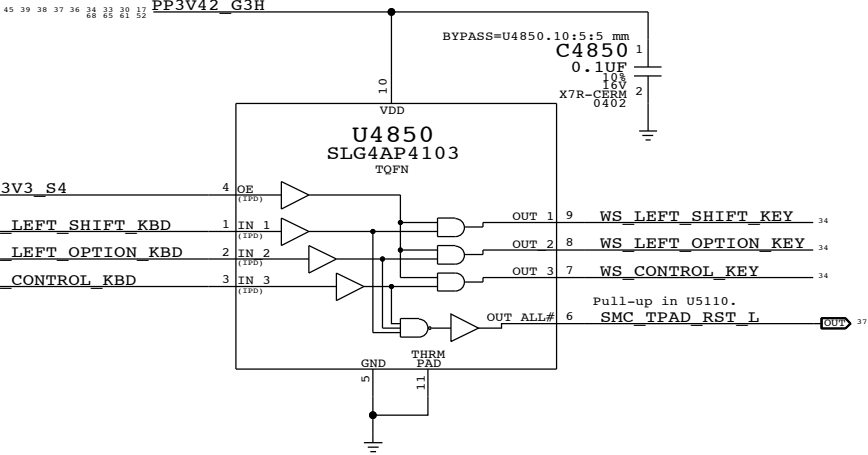






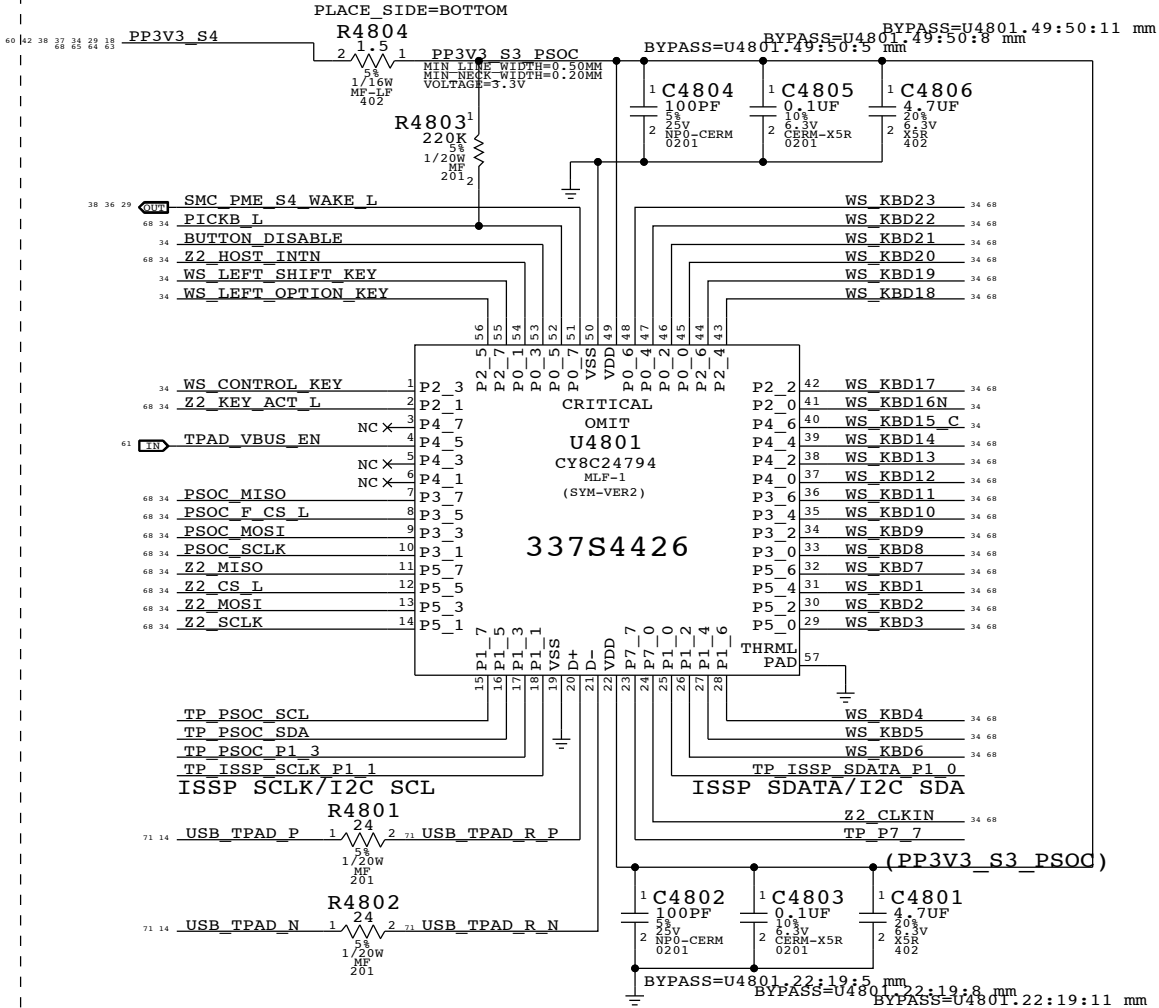
SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSoc power to isolate when PSoc is not powered.
No IPD on OE input pin PP3V3_S4 (symbol error).

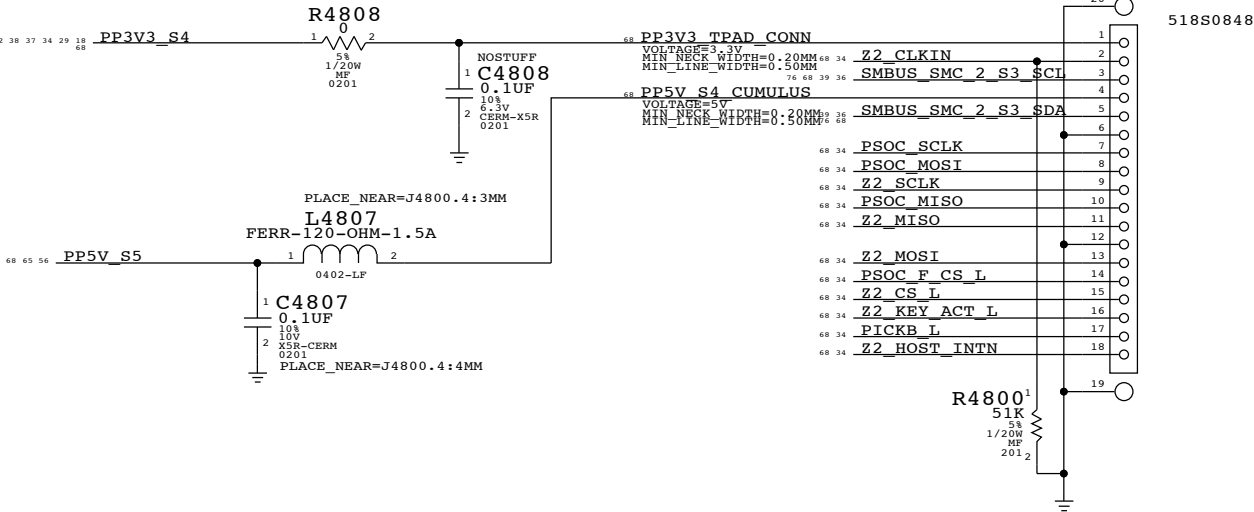


PSOC USB CONTROLLER

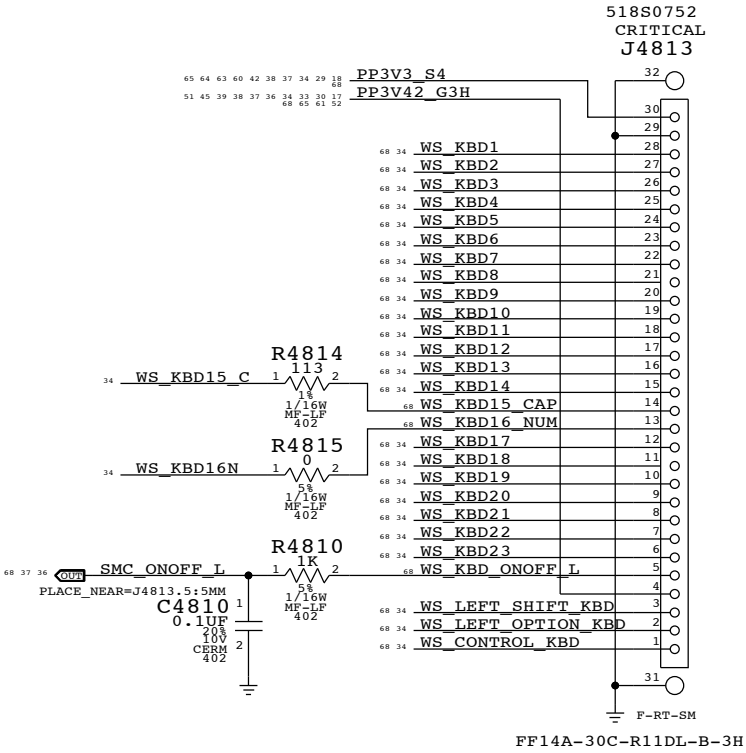
- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



IPD Flex Connector

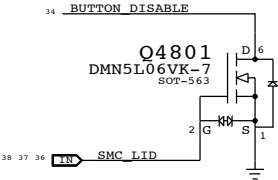


Keyboard Connector



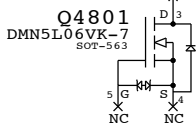
TPAD Buttons Disable

PLACE THESE COMPONENTS CLOSE TO J4800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB



THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

Spare MOSFET symbol



IC	PIN	NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W	
		80UA		0.204 V	16.32E-6 W	
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W	
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W	
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W	
		14MA (MAX)		0.021 V	294E-6 W	
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W	

SYNC MASTER=J44

SYNC DATE=08/12/2013

KEYBOARD/TRACKPAD (1 OF 2)

Apple Inc.

DRAWING NUMBER

<SCH_NUM>

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REVISION

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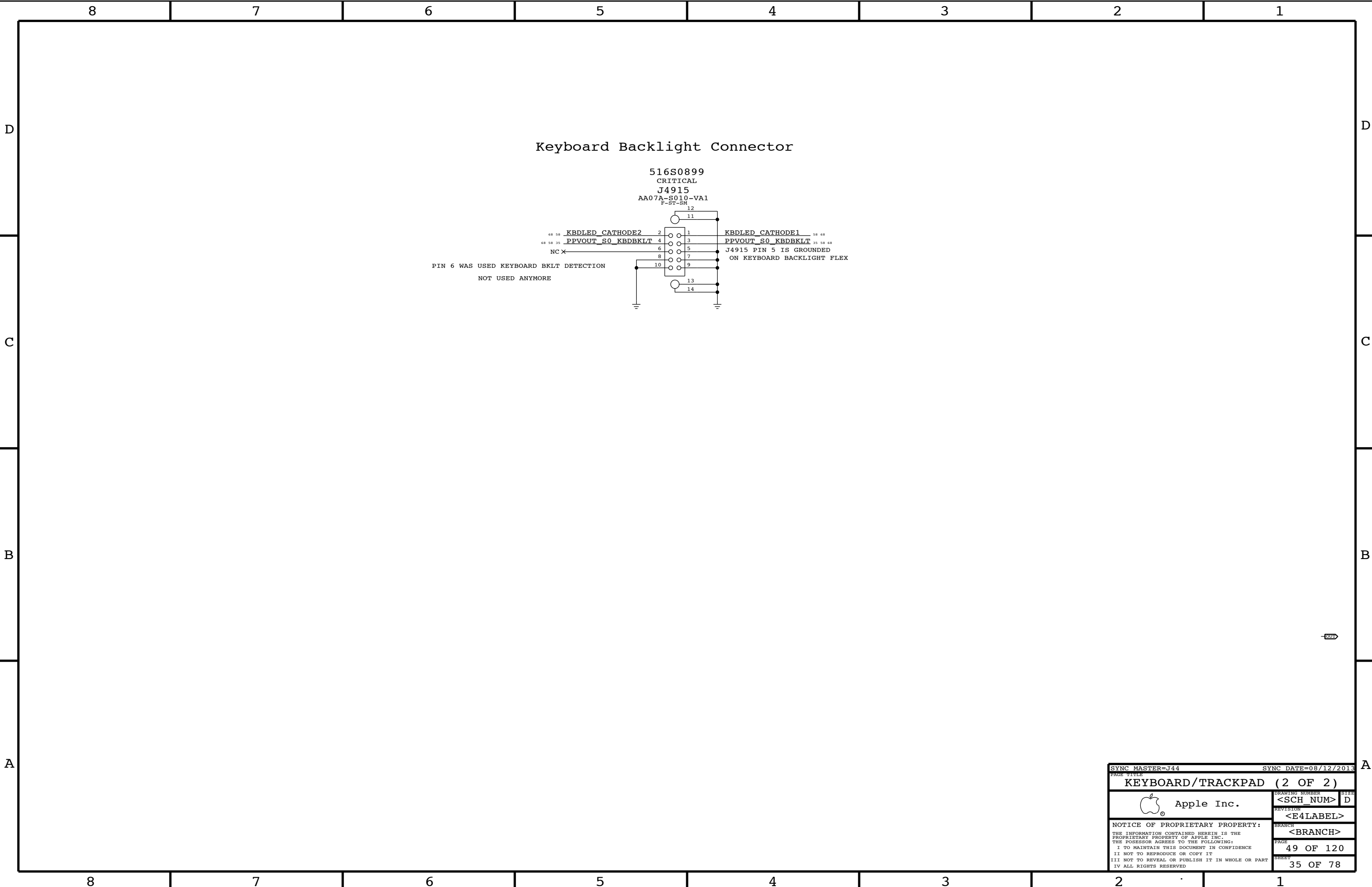
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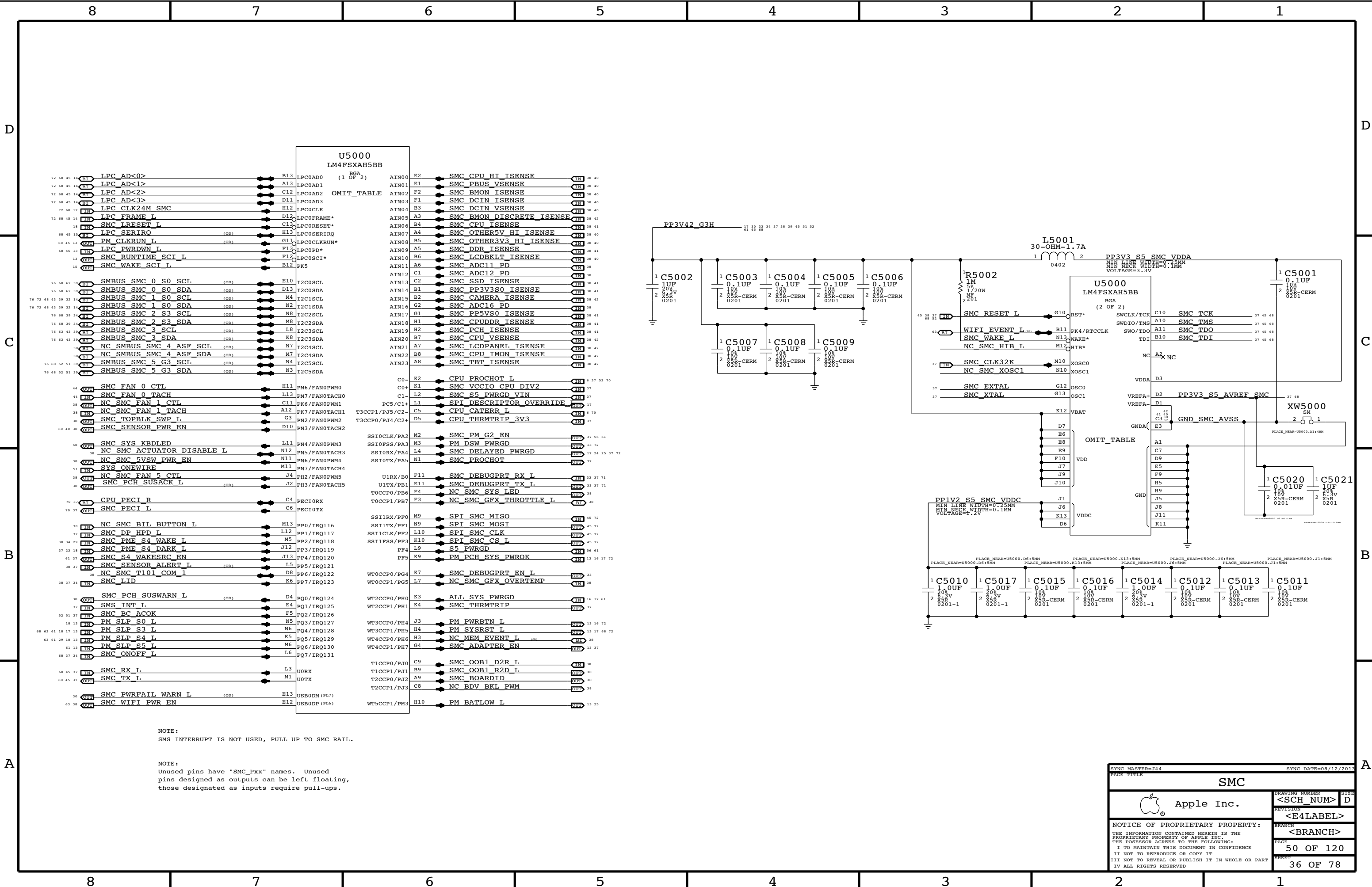
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SHEET

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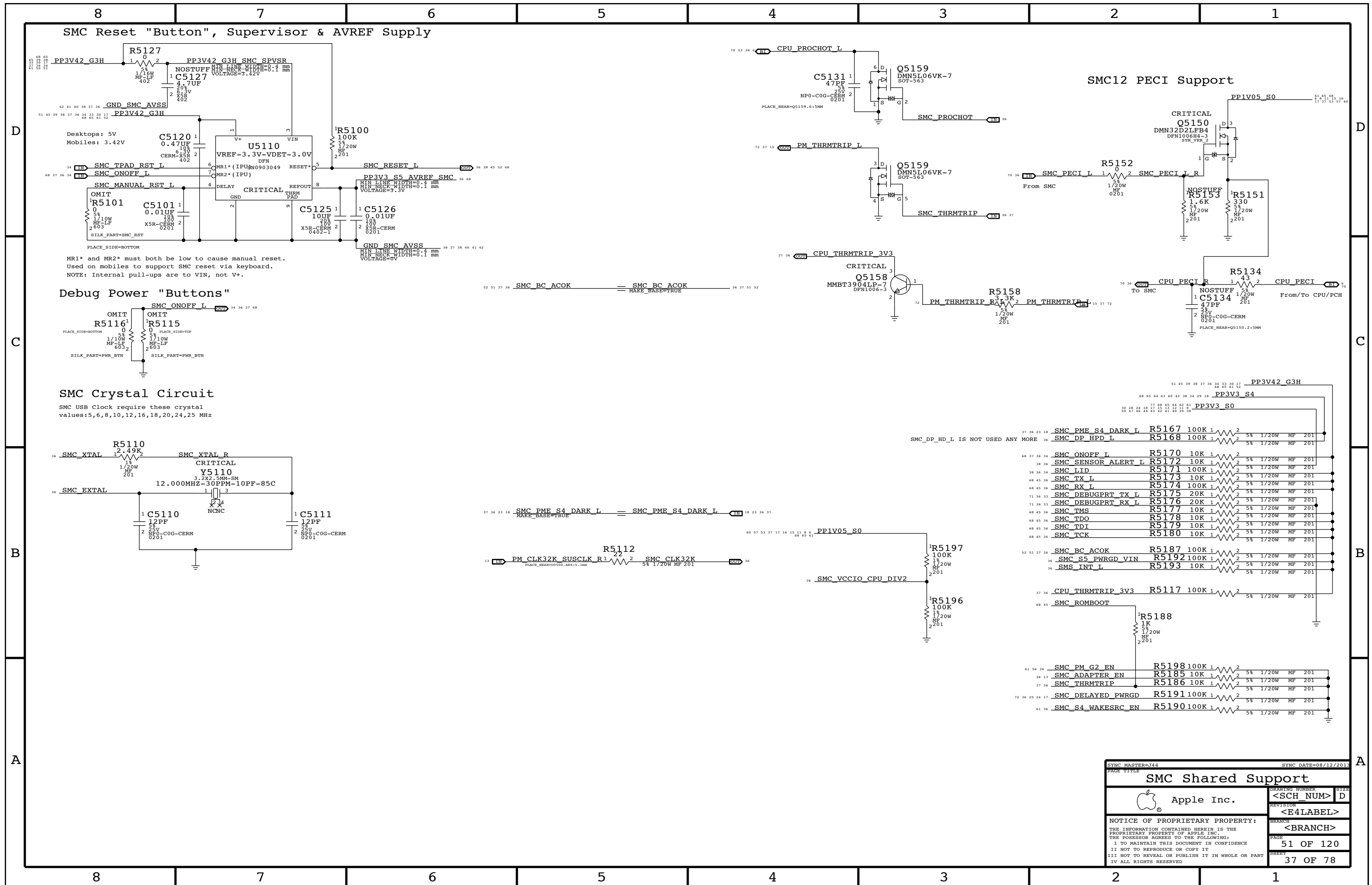


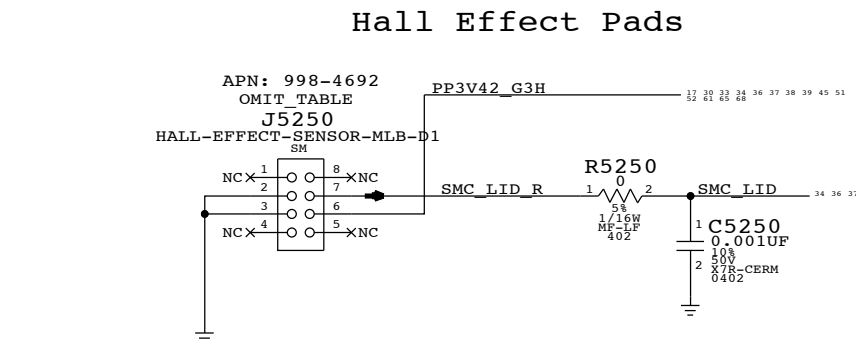
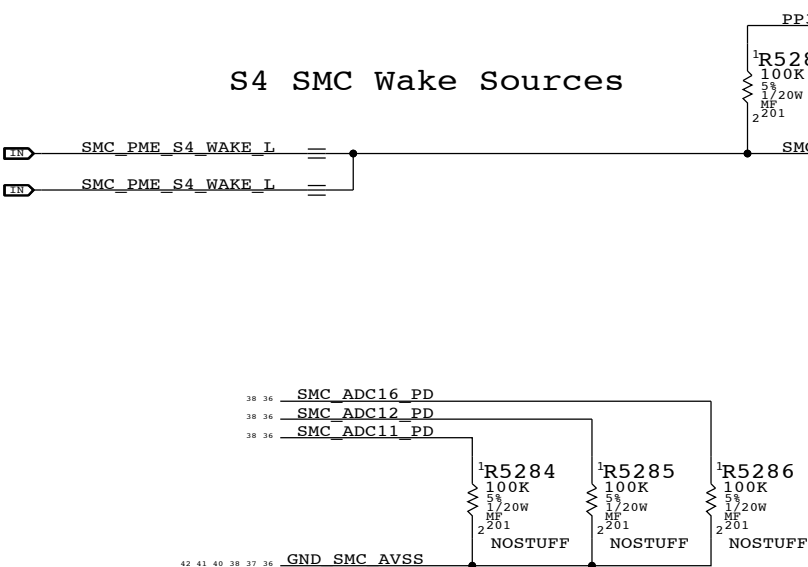
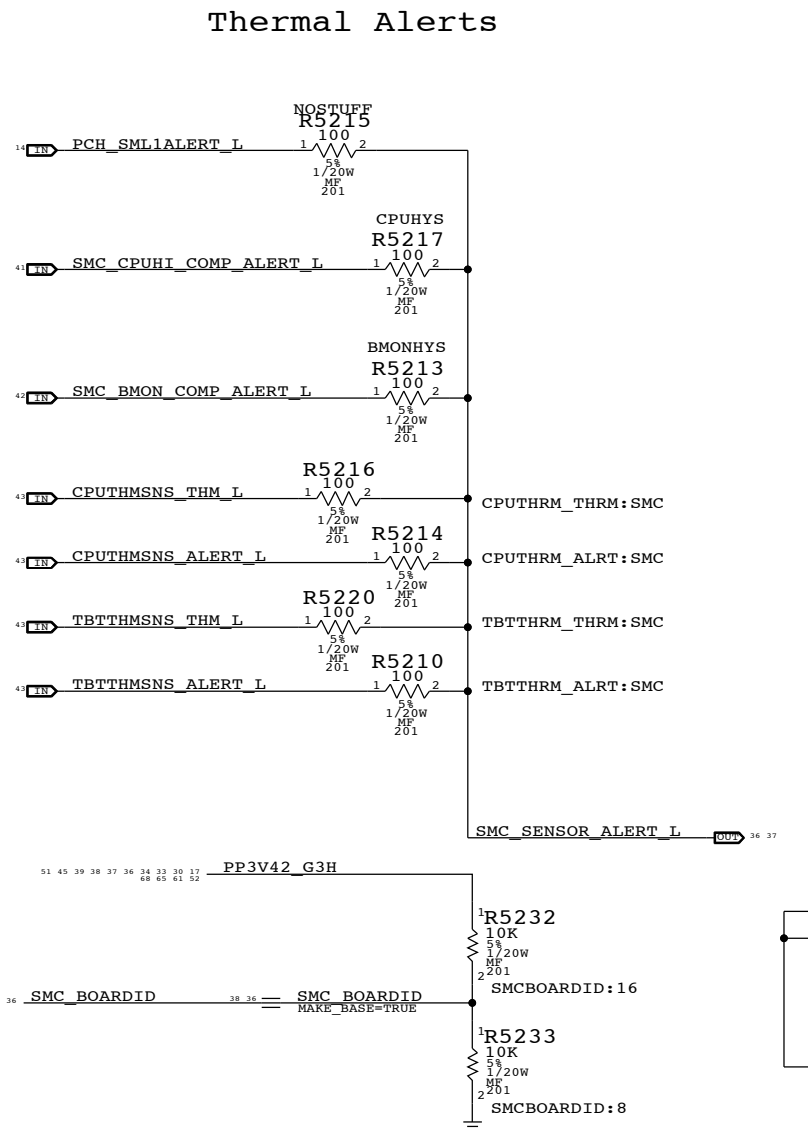
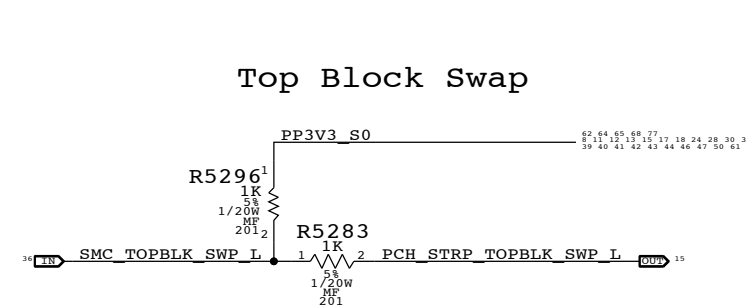
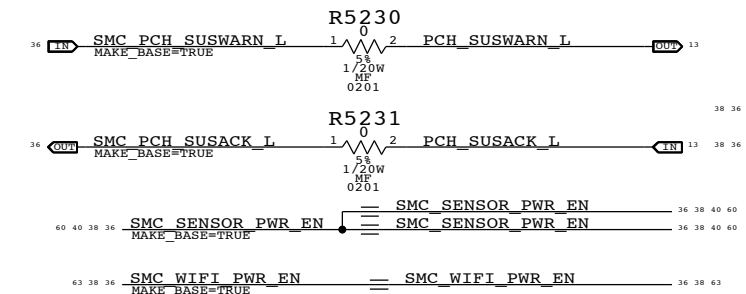
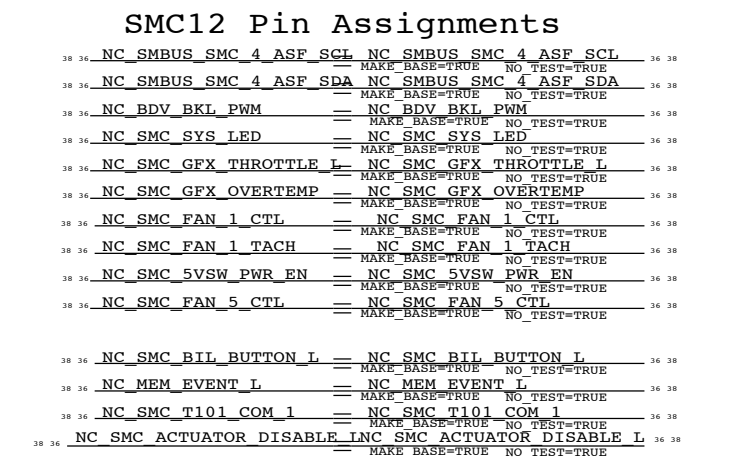
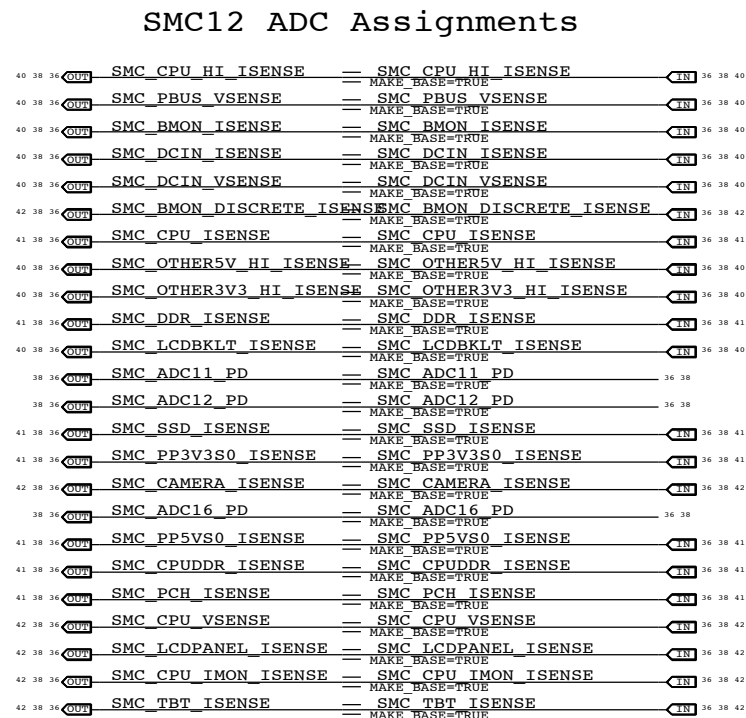


NOTE:
SMS INTERRUPT IS NOT USED, PULL UP TO SMC RAIL.

NOTE:
Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

SYNC MASTER=J44		SYNC DATE=08/12/2013	
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SMC		DRAWING NUMBER	
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REVISION		SIZE	
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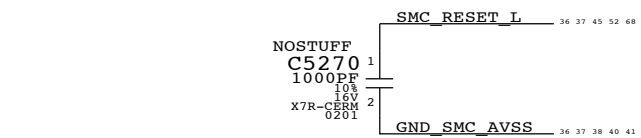
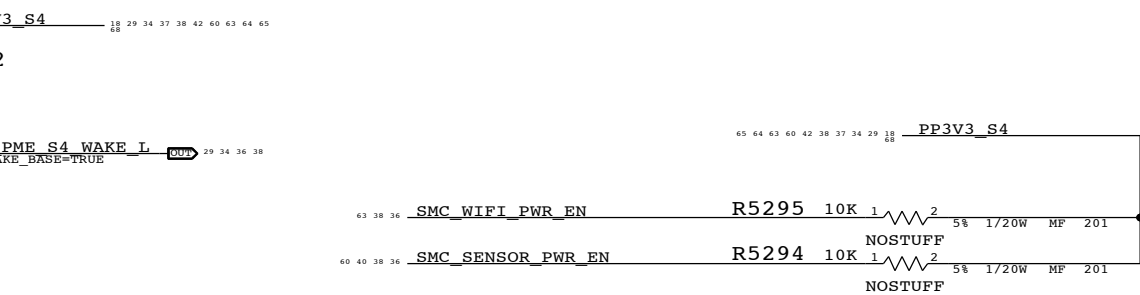
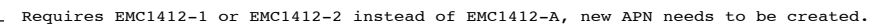



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
677-0912	1	SUBASSY,PCBA HALL EFFECT,J44	J5250	CRITICAL	

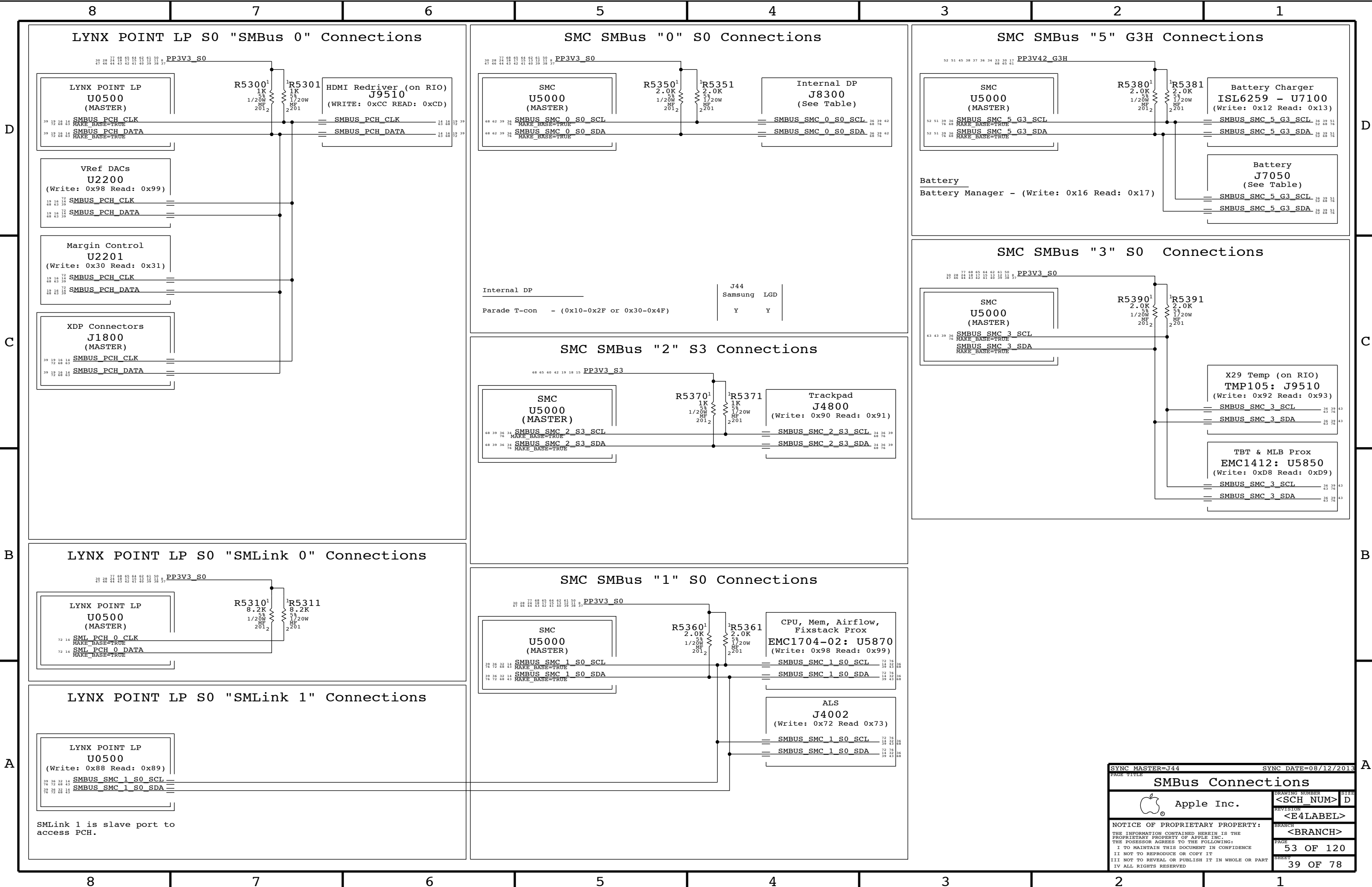
639-4502 (J44 HALL EFFECT BOARD) REPORTS TO 677-0912

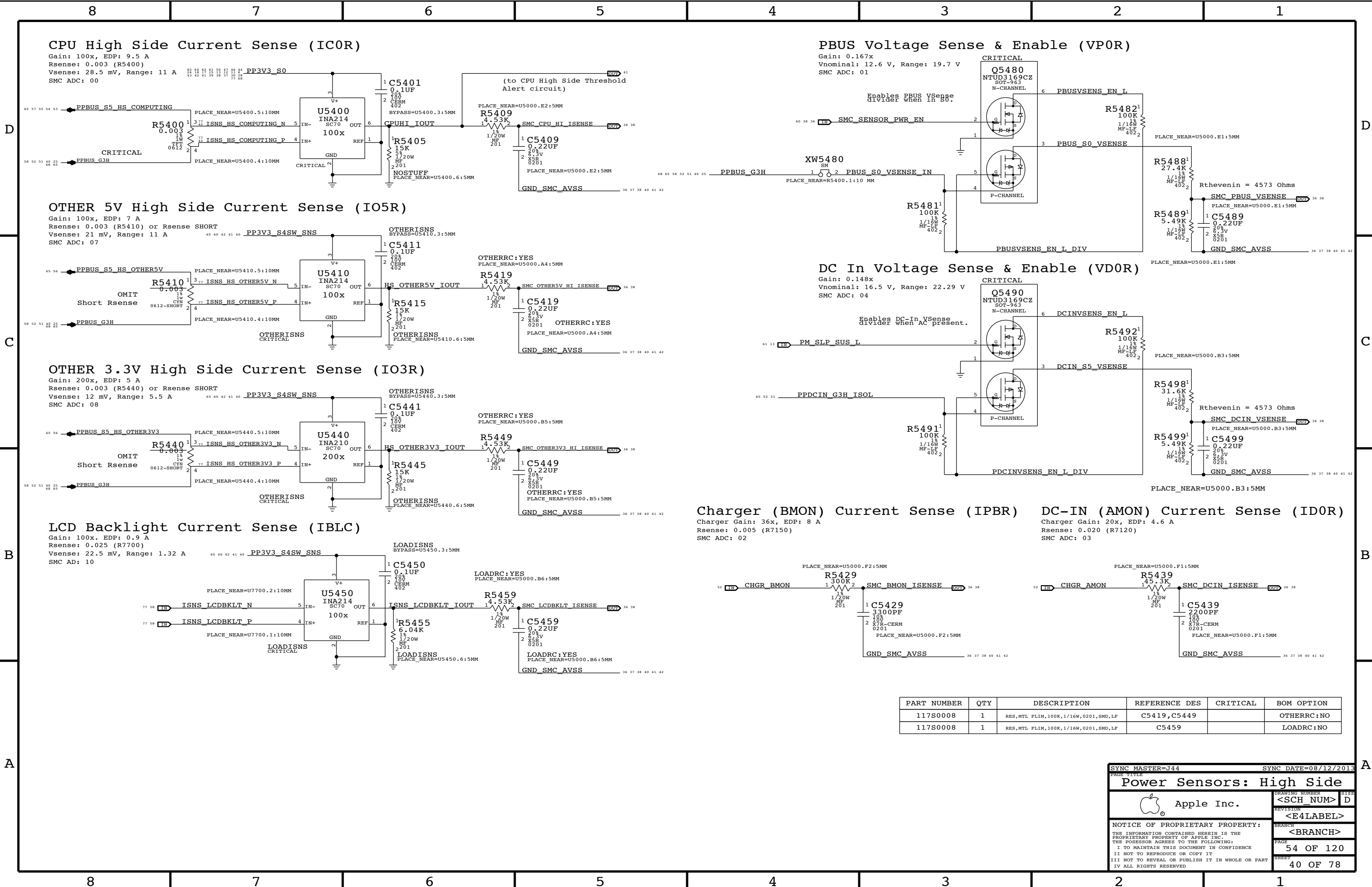
Specify one of these BOM GROUPS.	
BOM GROUP	BOM OPTIONS
CPUTHRM:BOTH	CPUTHRM_THRM:SMC,CPUTHRM_ALRT:SMC
CPUTHRM:THRM	CPUTHRM_THRM:SMC,CPUTHRM_ALRT:PU
CPUTHRM:ALRT	CPUTHRM_THRM:PU,CPUTHRM_ALRT:SMC
CPUTHRM:NONE	CPUTHRM_THRM:PU,CPUTHRM_ALRT:PU

Specify one of these BOM GROUPS.	
BOM GROUP	BOM OPTIONS
TBTTHRM:BOTH	TBTTHRM_THRM:SMC,TBTTHRM_ALRT:SMC
TBTTHRM:THRM	TBTTHRM_THRM:SMC,TBTTHRM_ALRT:PU
TBTTHRM:ALRT	TBTTHRM_THRM:PU,TBTTHRM_ALRT:SMC
TBTTHRM:NONE	TBTTHRM_THRM:PU,TBTTHRM_ALRT:PU
TBTTHRM:GONE	



PAGE TITLE		SMC Project Support	
	Apple Inc.		DRAWING NUMBER <SCH NUM>
			SIZE D
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		BRANCH <BRANCH>	
		PAGE 52 OF 120	
		SHEET 38 OF 78	





PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5419,C5449		OTHERRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5459		LOADRC:NO

SYNC MASTER=J44

SYNC DATE=08/12/2013

Power Sensors: High Side

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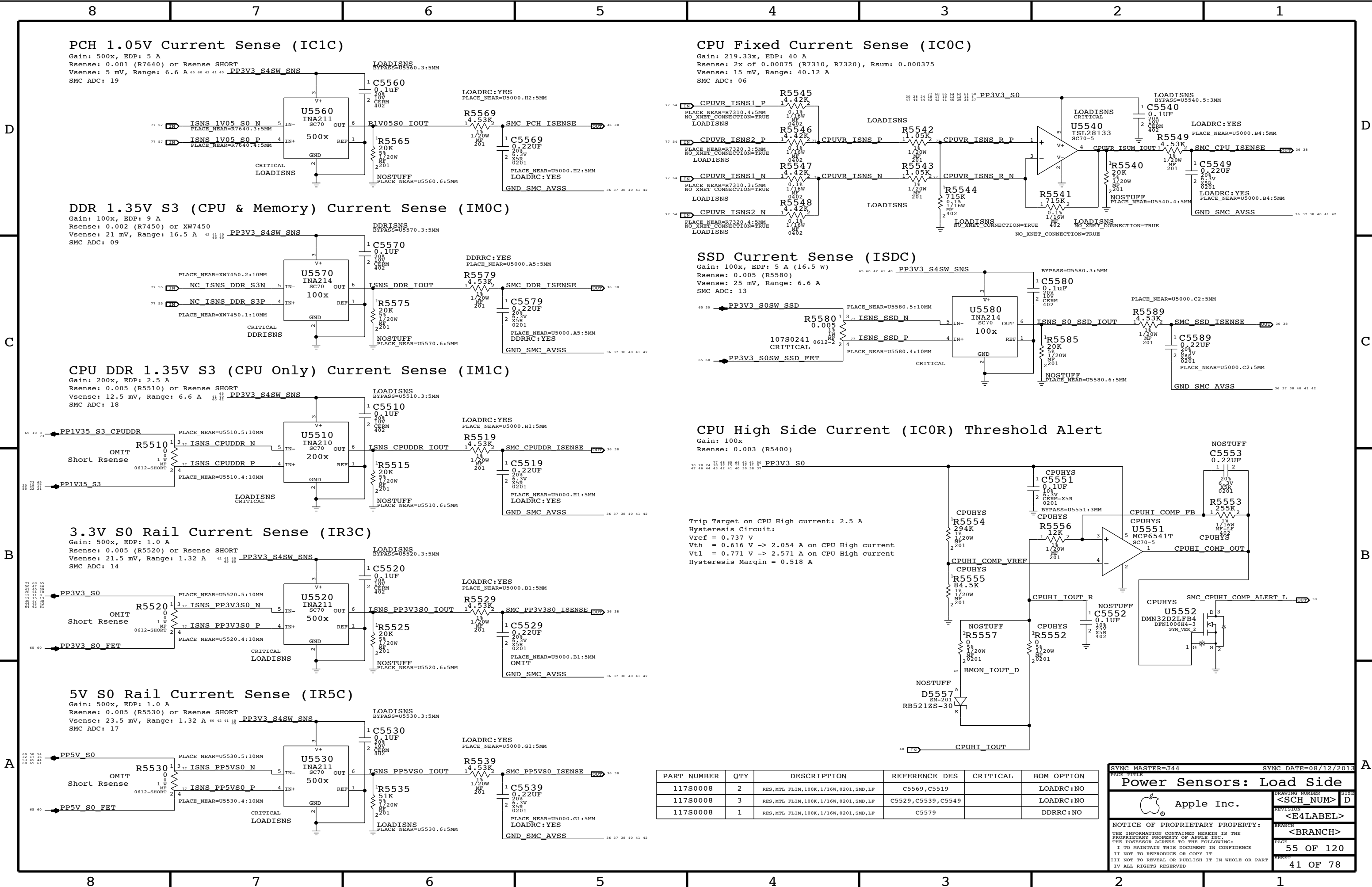
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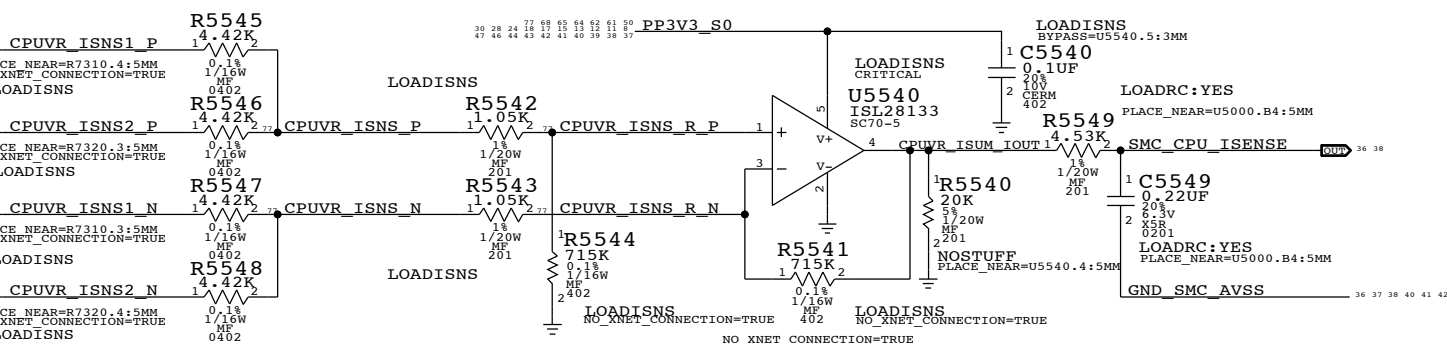
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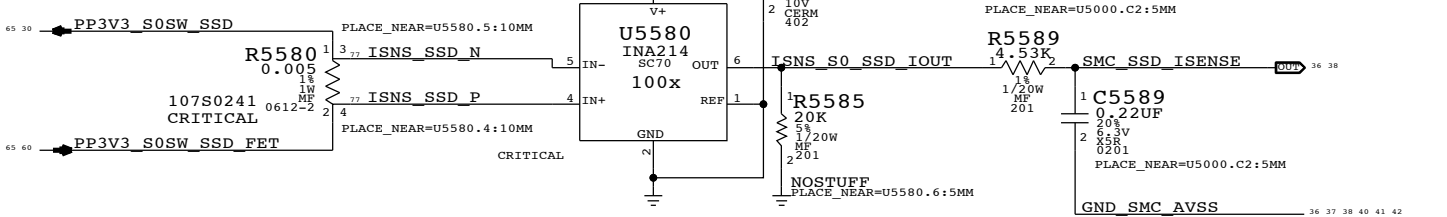
CPU Fixed Current Sense (IC0C)

Gain: 219.33x, EDP: 40 A
Rsense: 2x of 0.00075 (R7310, R7320), Rsum: 0.000375
Vsense: 15 mV, Range: 40.12 A
SMC ADC: 06



SSD Current Sense (ISDC)

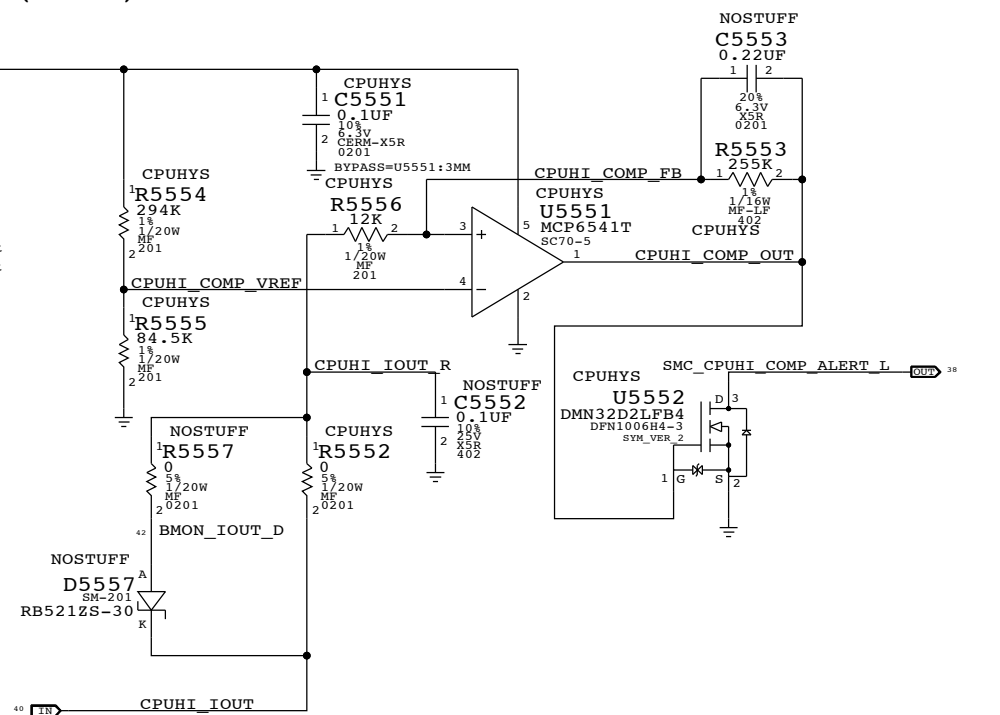
Gain: 100x, EDP: 5 A (16.5 W)
Rsense: 0.005 (R5580)
Vsense: 25 mV, Range: 6.6 A
SMC ADC: 13



CPU High Side Current (IC0R) Threshold Alert

Gain: 100x
Rsense: 0.003 (R5400)

Trip Target on CPU High current: 2.5 A
Hysteresis Circuit:
Vref = 0.737 V
Vth = 0.616 V -> 2.054 A on CPU High current
Vtl = 0.771 V -> 2.571 A on CPU High current
Hysteresis Margin = 0.518 A



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL,FLIM,100K,1/16W,0201,SMD,LF	C5569,C5519		LOADRC:NO
117S0008	3	RES,MTL,FLIM,100K,1/16W,0201,SMD,LF	C5529,C5539,C5549		LOADRC:NO
117S0008	1	RES,MTL,FLIM,100K,1/16W,0201,SMD,LF	C5579		DDRRC:NO

SYNC MASTER=J44

SYNC DATE=08/12/2013

Power Sensors: Load Side

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The schematic diagram illustrates the U5660 INA210 circuit. The central component is the U5660 INA210 IC, which is configured with a 200x gain. The circuit includes a 3.3V supply (PP3V3_S0) connected to the V+ pin. A 0.1uF bypass capacitor (C5660) is connected to the V+ pin. The IN- pin is connected to the INSN_HS_COMPUTING_P signal, and the IN+ pin is connected to the INSN_HS_COMPUTING_N signal. The REF pin is connected to the INSN_CPUHIGAIN_OUT1 signal. The GND pin is connected to ground. The circuit also includes several resistors (R5660, R5661, R5662, R5665, R5666, R5667, R5668, R5669) and capacitors (C5660, C5665). The output is labeled INSN_CPUHIGAIN_OUT1. The circuit is designed for a 200x gain and includes a 15K resistor (R5664) and a 1K resistor (R5662). The circuit is also labeled with 'NOSTUFF' and 'PLACE_NEAR=U5660.6:5MM'.

SENSE+ pins of EMC1704 sink 10-20uA current.
This deviation has been designed in our Peak Detection circuit

With 10uA sink:	0.125A	- 2.1A	->	13mV	- 83 mV
With 20uA sink:	0.125A	- 2.1A	->	23mV	- 92 mV

Gain: 50x. EDP: 8 A
Rsense: 0.005 (R7150)
Vsense: 50 mV, Range: 13.2 A
SMC AD: 05

SE **0.005** 36 38

36 28 24 16 08 05 13 12 11 80 PP3V3_S0
47 46 44 43 42 41 40 39 38 37

1 BMONHYS
C5671
0.1uF
10V
2 CERM-X5R
0201
DIP16SS=115671-3MM

1 2
NOSTUFF
C5673
0.22uF
20V
6.3V
0501
R5673
255K

0.0. A8:5MM

36 35 34 33 32 31 30

Trip Target on Battery current: 3.5 A
 Hysteresis Circuit:
 $V_{ref} = 0.854 \text{ V}$
 $V_{th} = 0.758 \text{ V} \rightarrow 3.031 \text{ A on Battery current}$
 $V_{tl} = 0.887 \text{ V} \rightarrow 3.549 \text{ A on Battery current}$
 Hysteresis Margin = 0.518 A

SMC ADC: 20

XW5680

R5689

SMC CPU VSENSE

PPVCC S0 CPU

CPUVSENSE IN

PLACE_NEAR=R7310.2:5 MM

PLACE_NEAR=U5000.B7:5MM

C5689

0.22uF

20V

6.3V

XSR

0201

GND_SMC_AVSS

Gain: 1 A / 28.273 mV, Range: 40 A.

SMC ADC: 22

SMC CPUVIR_IMON

R5699

SMC CPU IMON ISENSE

16 38

With R7210 (Ri) set to 316 Ohm,
R7310 (Rsen) set to 0.75 mOhm,
R7230 set to 95.3 kOhm,
Num Phases (N) is 2, and Io (ICCmax) is 40A,
then Ia of Io gives 28.273mV at the Vimom.

PLACE_NEAR=U5000.B8:5MM

R5699
0.22UF

205V
2XSR
0201

NOSTUFF
PLACE_NEAR=U5000.B8:5MM

GND SMC AVSS

36 37 38 40 41 42

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	<BRANCH>	
	PAGE	56 OF 120
	SHEET	

Gain: 200x. EDP: 2.8 A
Rsense: 0.005 (R5640) or Rsense SHORT
Vsense: 14 mV, Range: 3.3 A
SMC AD: 23

PP3V3_S4 TBT

Short Rsense

PP3V3_S4

PLACE_NEAR=U5640.5:10MM

ISNS_TBT_N

ISNS_TBT_P

PLACE_NEAR=U5640.4:10MM

TBTISNS

U5640

INA2110

200x

REF

GND

R5648

1/20W 0.1% 0201

NOSTUFF

PLACE_NEAR=XW5640.2:10MM

ISNS_TBT_IVIN

ISNS_TBT_IVOUT

PP3V3_S4SW_SNS

TBTISNS

EVPASS=U5640.3:5MM

C5640

0.1uF

10V 0.1% 0201

PLACE_NEAR=XW5640.2:10MM

TBTISNS

R5647

1/20W 0.1% 0201

R5649

4.53K

1/20W 0.1% 0201

SMC TBT IS

C5649

0.22uF

2.5V 0.1% 0201

TBTTRC: YES

PLACE_NEAR=U5000.A8:5MM

TBTTRC: YES

PLACE_NEAR=

GND SMC

Gain: 500x. EDP: 1 A
RSENSE: 0.005 (R8320) or Rsense SHORT
Vsense: 5 mV, Range: 1.32 A 65 60 42 41 40
SMC AD: 21

LOADISNS
BYPASS=U5620.3:5MM

C5620
0.1UF
180V
2 180V 402

LOADRC:YES
PLACE_NEAR=U5000.A7:5MM

R5629
4.53K
1 20W MF 201

SMC_LCDPANEL_ISENSE

C5629
0.22UF
20V
2 20V 0201

LOADRC:YES
PLACE_NEAR=U5000.A7:5MM

GND_SMC_AVSS

U5620
INA211
SC70
500x
OUT
REF
GND

ISNS_LCDPANEL_N
ISNS_LCDPANEL_P


LOADISNS
PLACE_NEAR=U5620.6:5MM

36 37 38 40

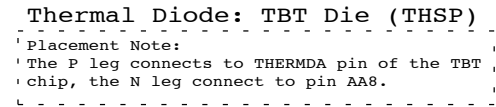
Gain: 500x. EDP: 0.82 A
Rsense: 0.005 (R5610) or XW5610
Vsense: 4.1 mV, Range: 1.32 A
SMC AD: 15

The schematic diagram illustrates the internal circuitry of the SMC AD15 camera module. It features three main power input sections on the left: PP3V3_S3RS0_CAMERA, PP3V3_S3RS0_CAMERA_R, and PP3V3_S3. The first two sections are connected to a common XW5610 sense point, which then splits into two paths: CAMERA_3V3:S0 and CAMERA_3V3:S3. These paths include resistors R5611, R5612, and R5613, along with a 1/16W resistor and a 402 capacitor. The third section, PP3V3_S3, is connected to a 1/16W resistor and a 402 capacitor. The central part of the diagram shows the U5610 INA211 SCT0 500x operational amplifier, which is configured with its non-inverting input (IN-) to the common sense point, its inverting input (IN+) to the common sense point, and its output (OUT) to the common sense point. The op-amp is powered by V+ and GND. The output of the op-amp is connected to the ISNS_CAMERA_IOUT pin, which is also connected to the ISNS_CAMERA_IOUT pin of the SMC CAMERA_ISENSE module. The SMC CAMERA_ISENSE module includes a 4.53k resistor (R5619) and a 0.22uF capacitor (C5619). The module is also connected to the GND_SMC_AVSS pin. The right side of the diagram shows the SMC CAMERA_ISENSE module with its own sense point, ISNS_CAMERA_IOUT, and a 4.53k resistor (R5619) and a 0.22uF capacitor (C5619). The module is also connected to the GND_SMC_AVSS pin. The bottom right corner shows the GND_SMC_AVSS pin connected to the GND_SMC_AVSS pin of the SMC CAMERA_ISENSE module.

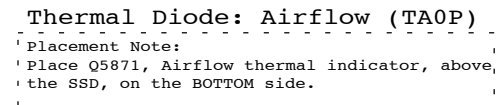
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	4	RES,NTL FILM,100K,1/16W,0201,SMD,LF	C5619,C5629,C5649		
117S0008	1	RES,NTL FILM,100K,1/16W,0201,SMD,LF	C5679		

SYNC MASTER=J44		SYNC DATE=08/12/20	
PAGE 1112			
Power Sensors: Extended			
 Apple Inc.		DRAWING NUMBER <SCH NUM>	
		REVISION <E4LABEL>	
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I2C Write: 0xD8, I2C Read: 0xD9



I2C Write: 0x98, I2C Read: 0x99



```

' Placement Note:
' Place Q5872 between two rows of Memory devices
' between channel A and B, on the BOTTOM side.
'


```

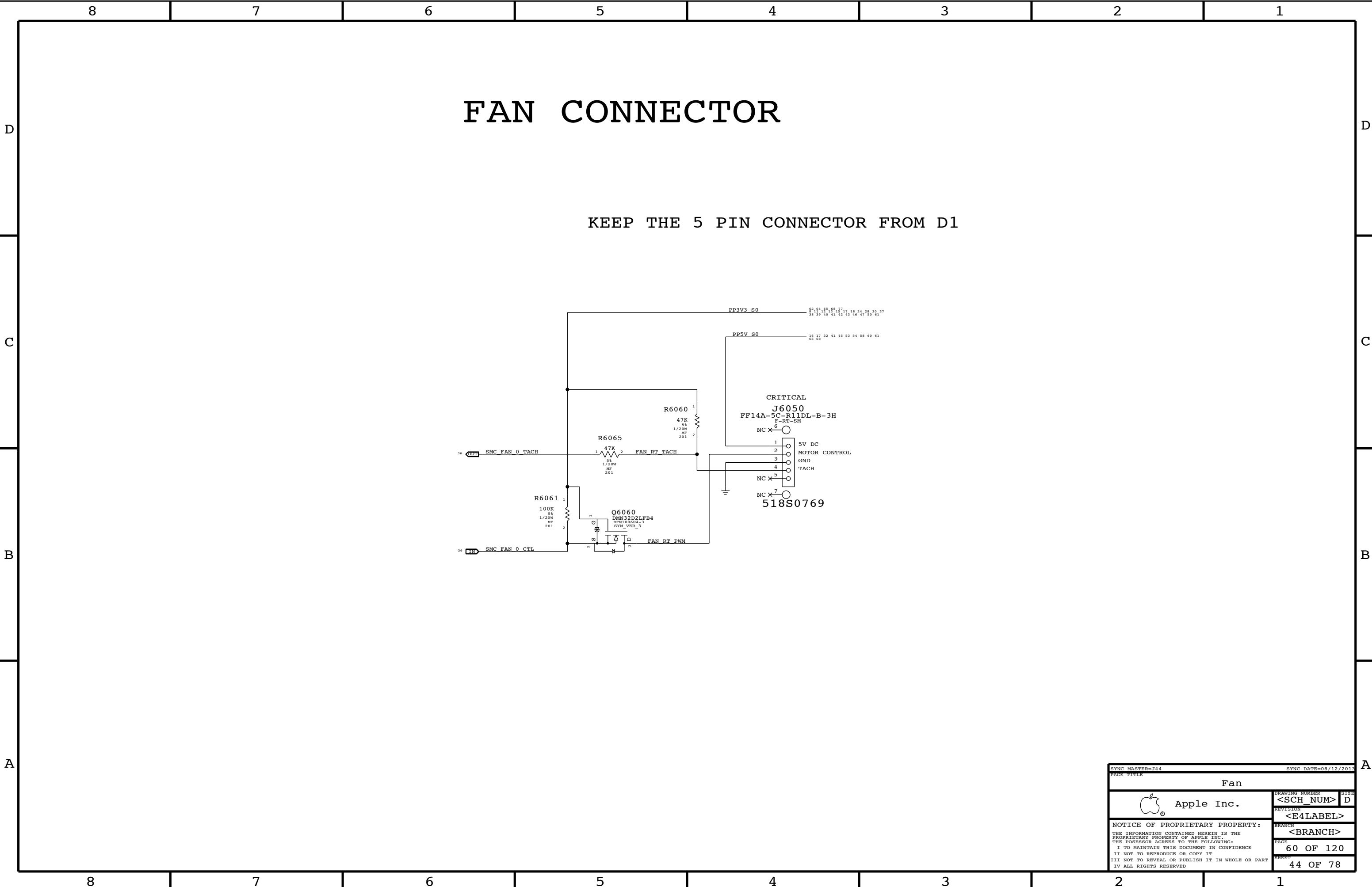
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| Placement Note:  
| Place Q5873 under the CPU,  
| on the BOTTOM side.  
L - - - - -
```

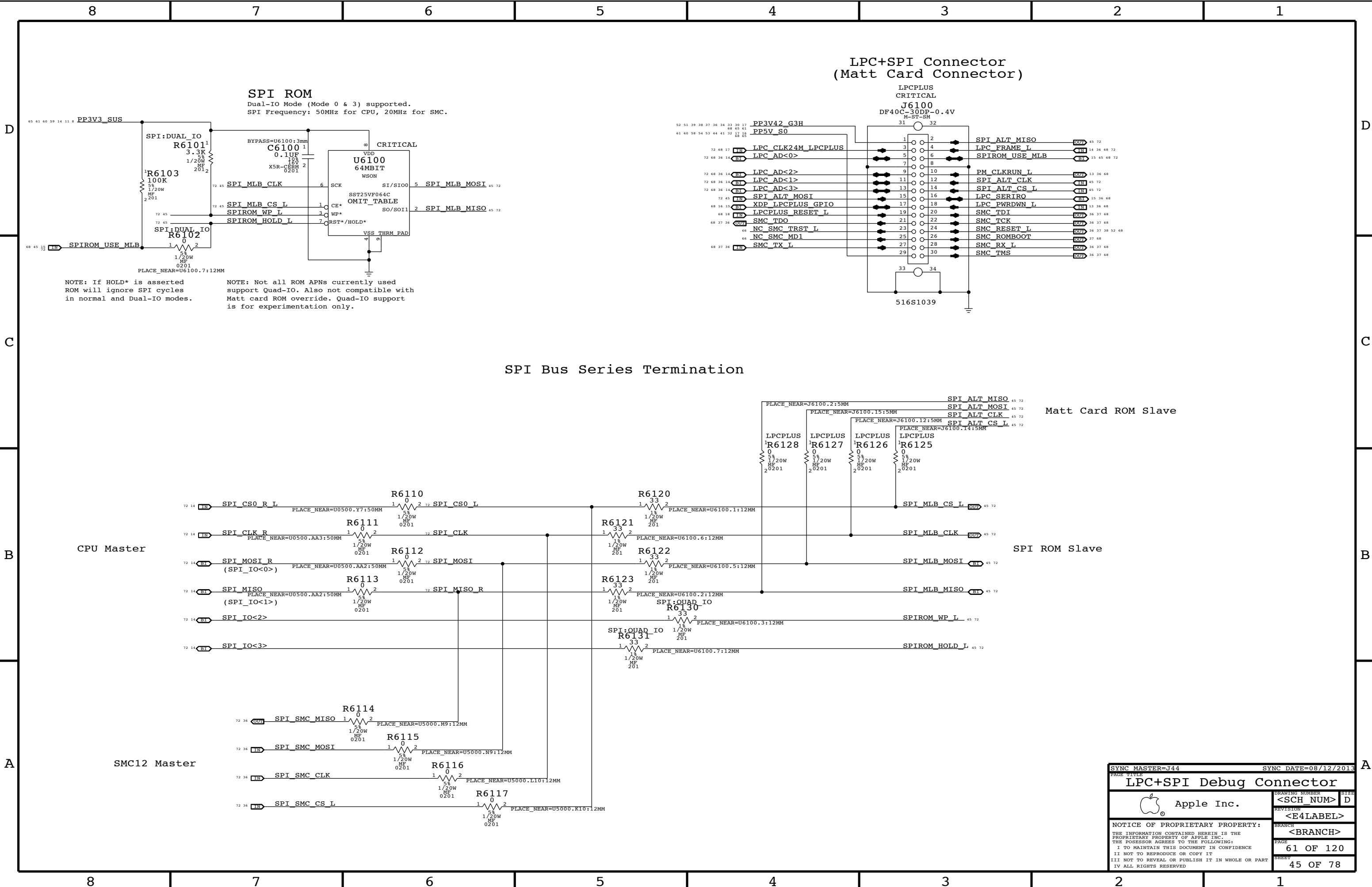
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' Placement Note:
' Place U5870 at corner near Fan,
' on the TOP side.

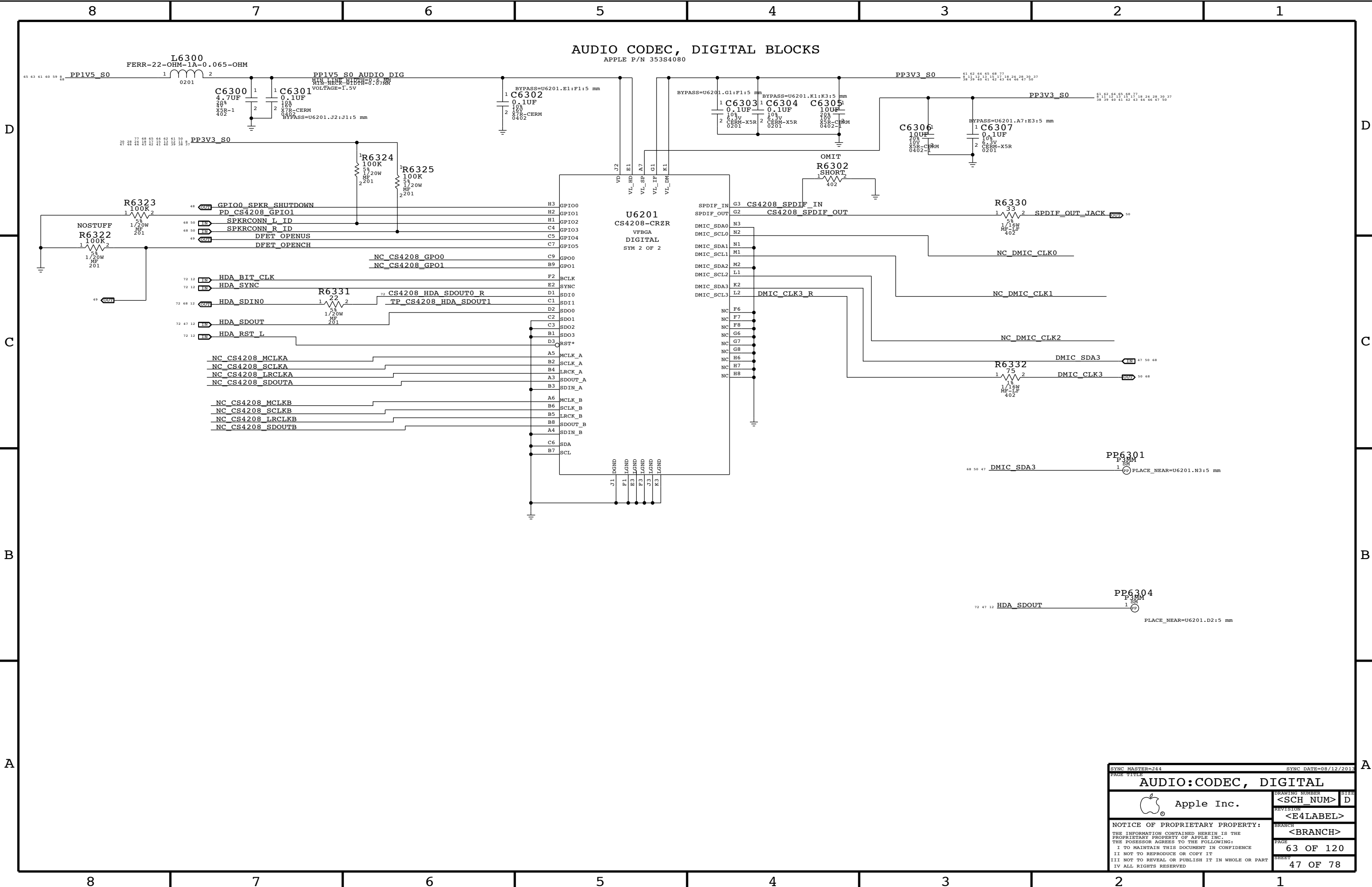
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Thermal Sensors			
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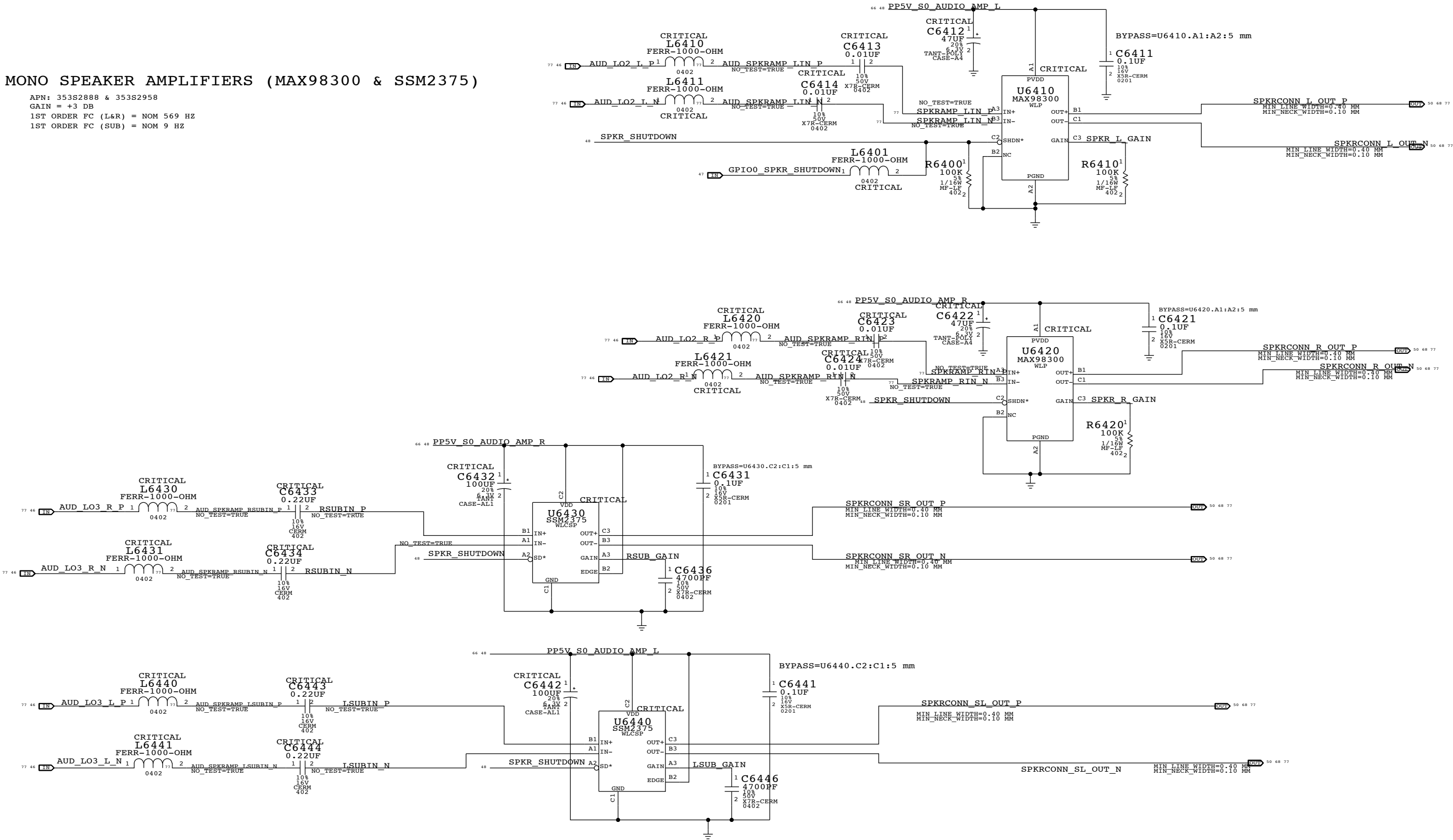



SYNC MASTER=J44		SYNC DATE=08/12/2013	
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LPC+SPI Debug Connector			
 Apple Inc.	DRAWING NUMBER		SIZE
	<SCH_NUM>		D
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		45 OF 78	

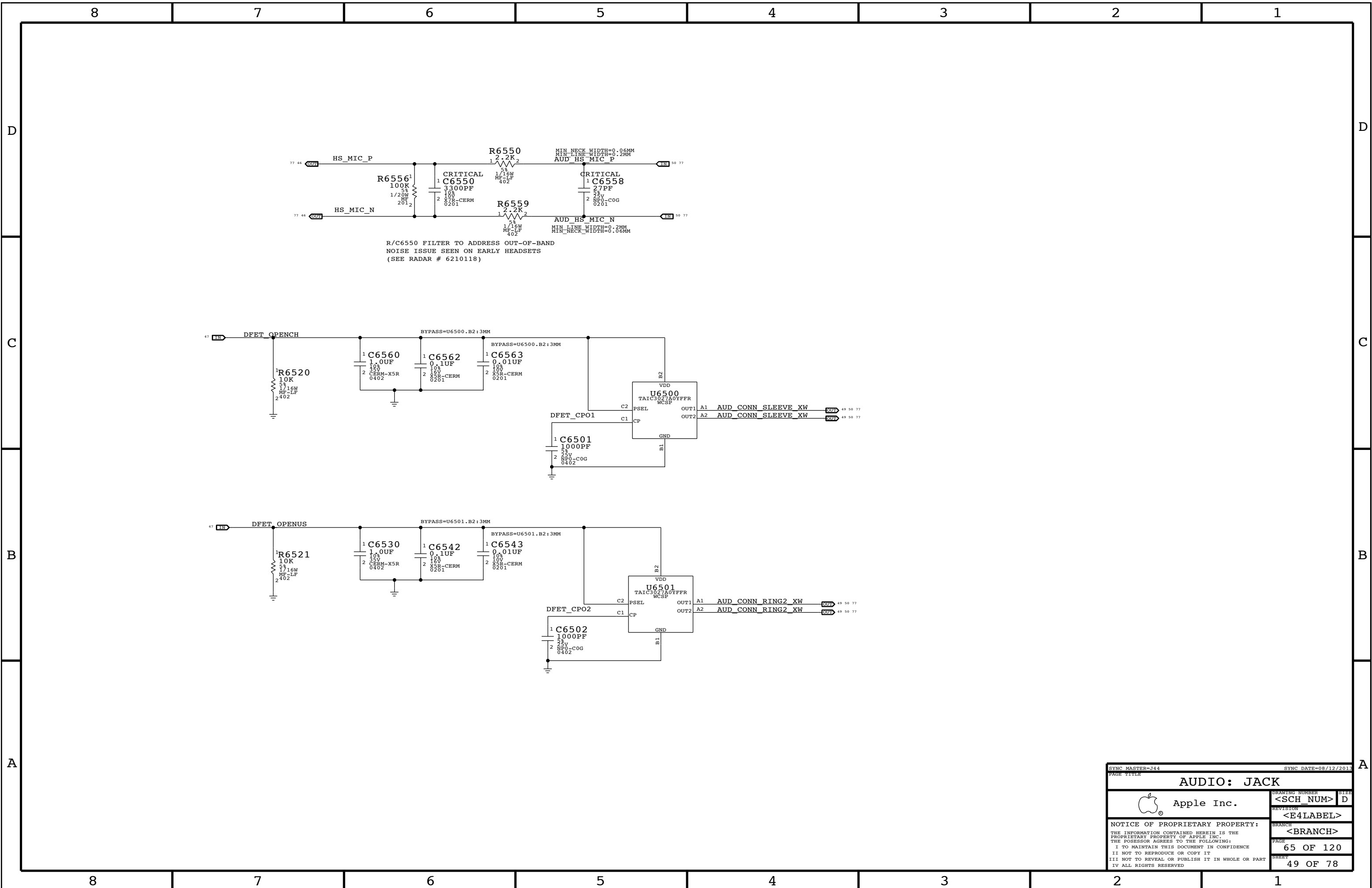


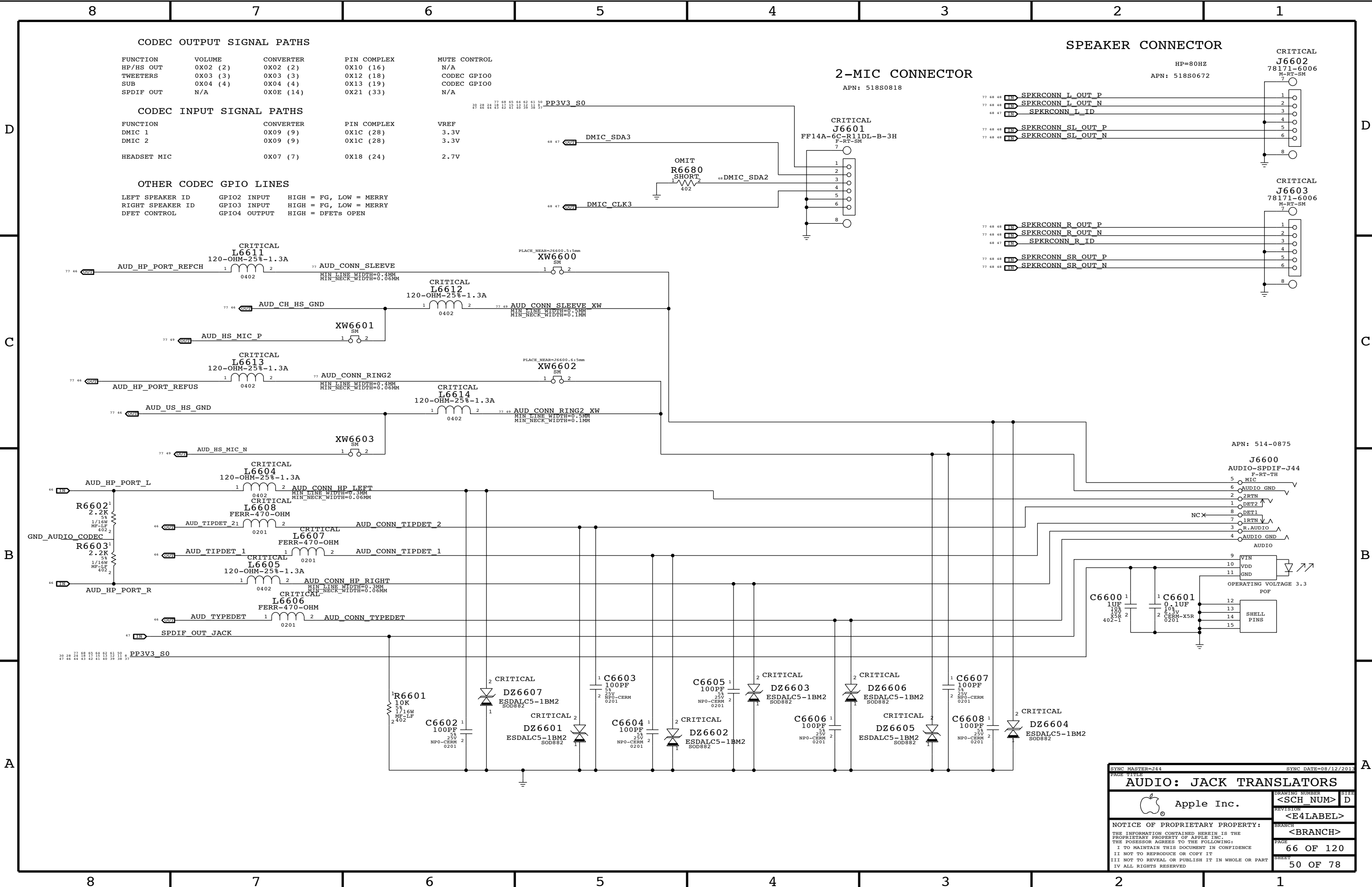
4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)

APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ



SYNC MASTER=J44		SYNC DATE=08/12/2013	
PAGE TITLE			
AUDIO: SPEAKER AMP			
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		BRANCH	
		<BRANCH>	
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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL
HP/HS OUT	0X02 (2)	0X02 (2)	0X10 (16)	N/A
TWEETERS	0X03 (3)	0X03 (3)	0X12 (18)	CODEC GPIO0
SUB	0X04 (4)	0X04 (4)	0X13 (19)	CODEC GPIO0
SPDIF OUT	N/A	0X0E (14)	0X21 (33)	N/A

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF
DMIC 1	0X09 (9)	0X1C (28)	3.3V
DMIC 2	0X09 (9)	0X1C (28)	3.3V
HEADSET MIC	0X07 (7)	0X18 (24)	2.7V

OTHER CODEC GPIO LINES

LEFT SPEAKER ID	GPIO2 INPUT	HIGH = FG, LOW = MERRY
RIGHT SPEAKER ID	GPIO3 INPUT	HIGH = FG, LOW = MERRY
DFET CONTROL	GPIO4 OUTPUT	HIGH = DFETs OPEN

2-MIC CONNECTOR

APN: 518S0818

SPEAKER CONNECTOR

HP=80HZ
APN: 518S0672

CRITICAL
J6602
78171-6006
M-RT-SM

CRITICAL
J6603
78171-6006
M-RT-SM

APN: 514-0875

J6600
AUDIO-SPDIF-J44
F-RT-TH

OPERATING VOLTAGE 3.3
POF

SYNC MASTER=J44

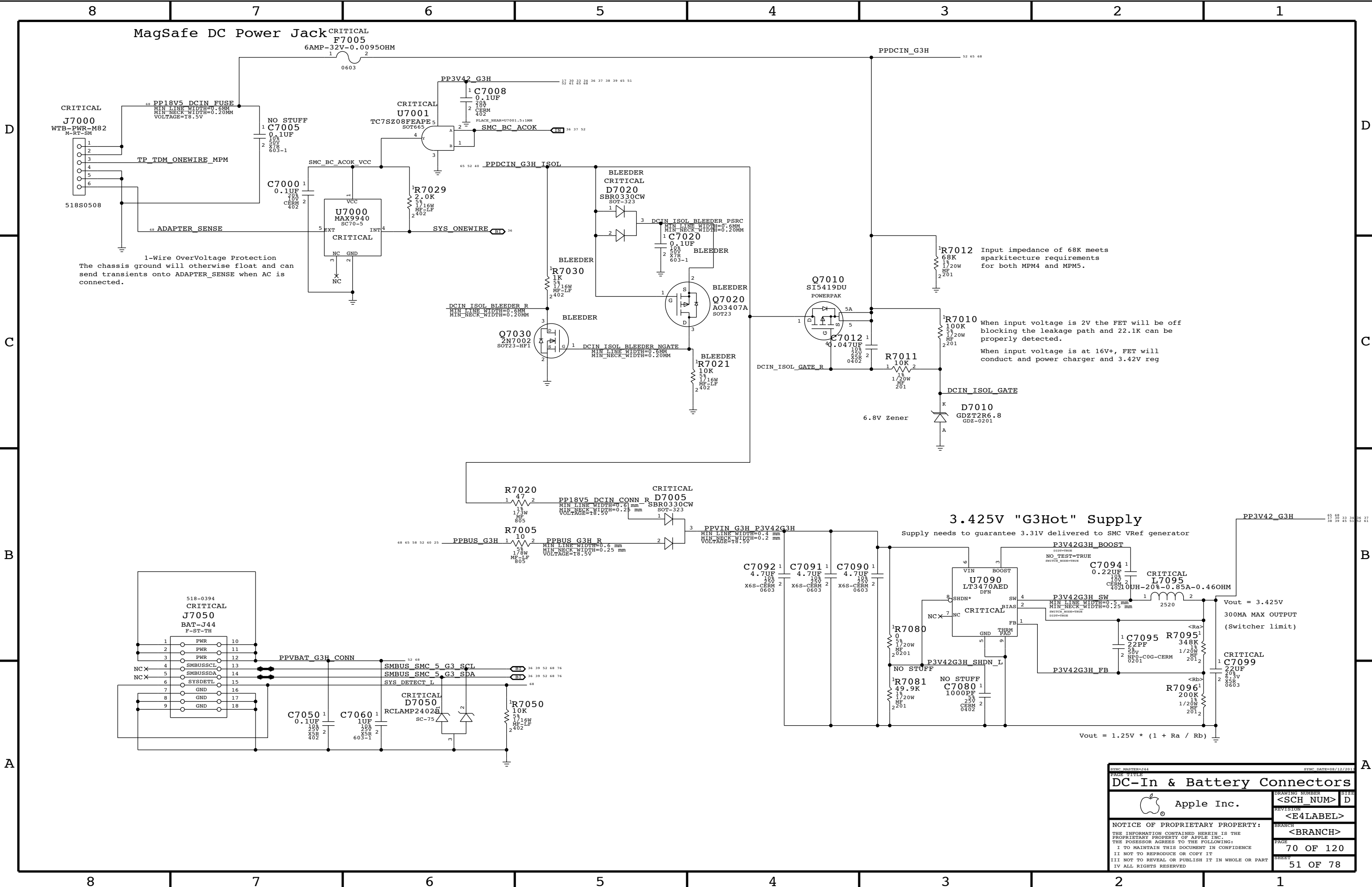
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AUDIO: JACK TRANSLATORS

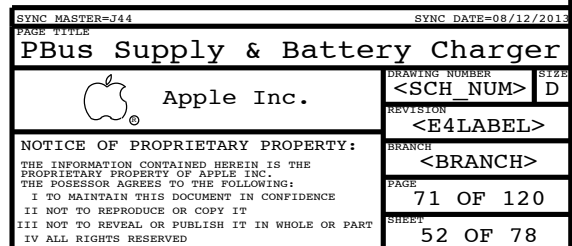
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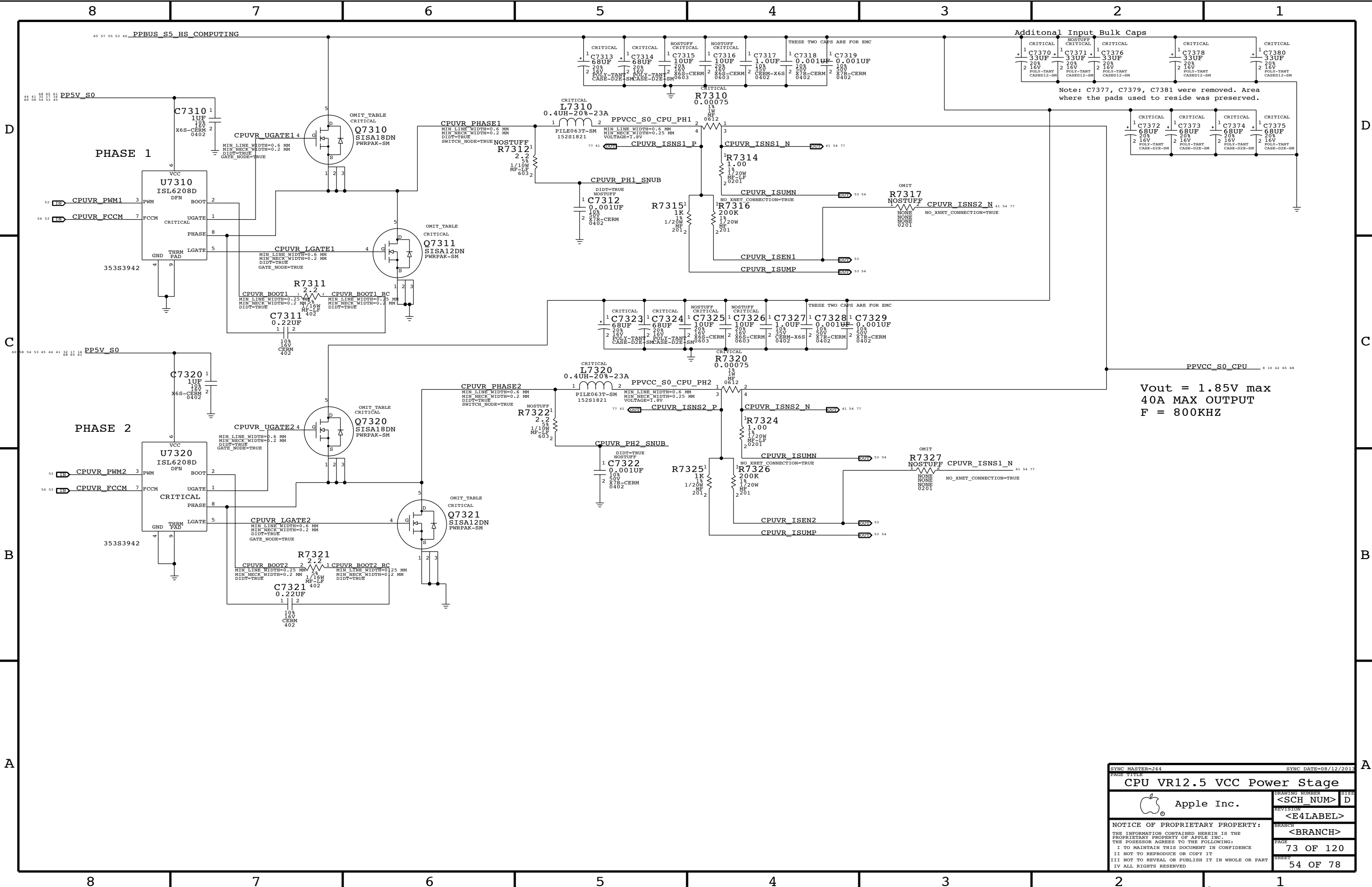
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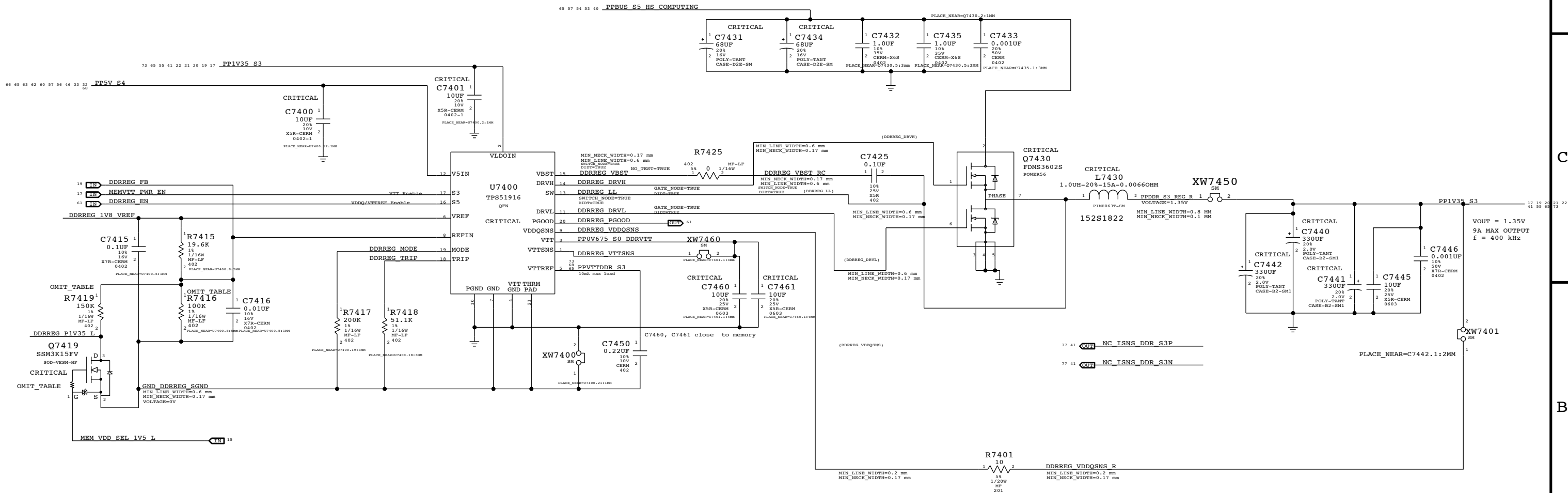


Inrush Limiter

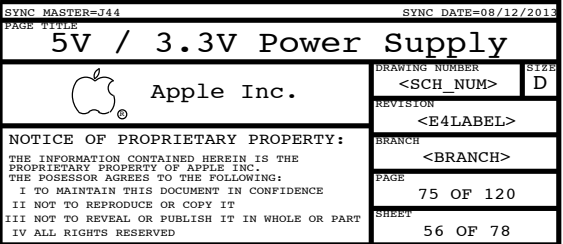




DDR3L (1V35 S3) REGULATOR



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0411	1	RES,MTL FILM,1/16W,100K,1,0402,SMD,LF	R7416	CRITICAL	PPDDR:1V5
114S0391	1	RES,MTL FILM,1/16W,60.4K,1,0402,SMD,LF	R7416	CRITICAL	PPDDR:1V35
376S0612	1	MOSFET,N-CH,30V,100MA,7.00HM,SOT-723,HF	Q7419	CRITICAL	PPDDR:1V5
114S0428	1	RES, MTL FILM,1/16W,150k,0402,SMD,LF	R7419	CRITICAL	PPDDR:1V5



D

C

B

A

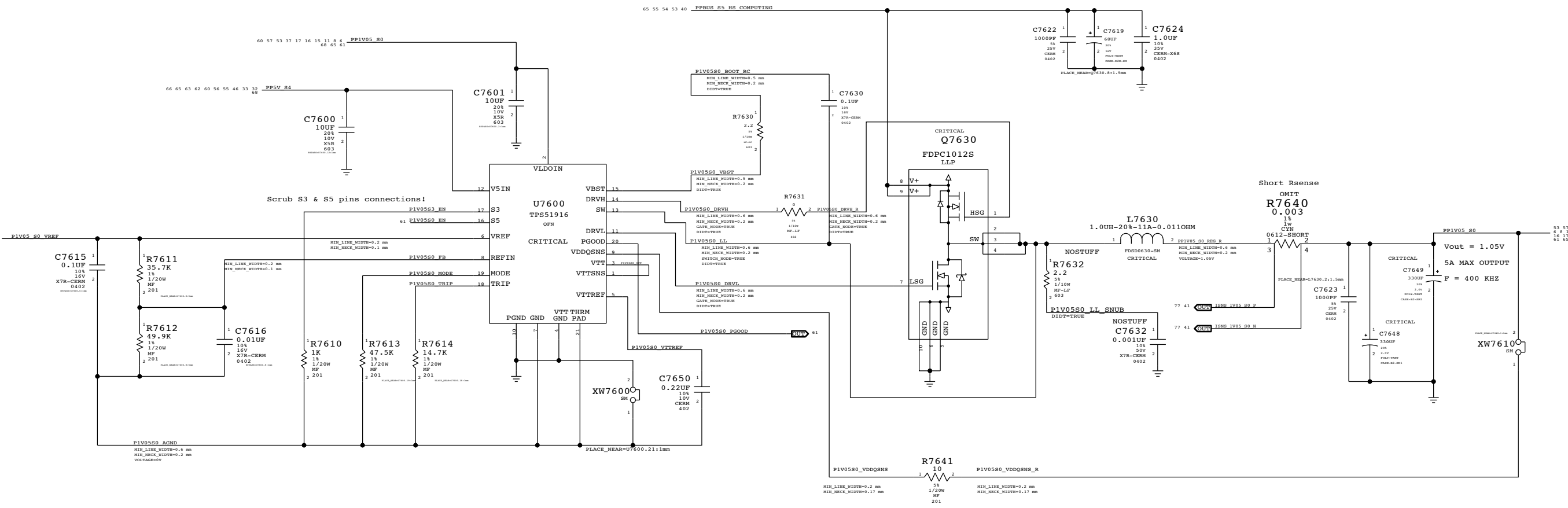
D


C

B

A

1.05V S0 Regulator



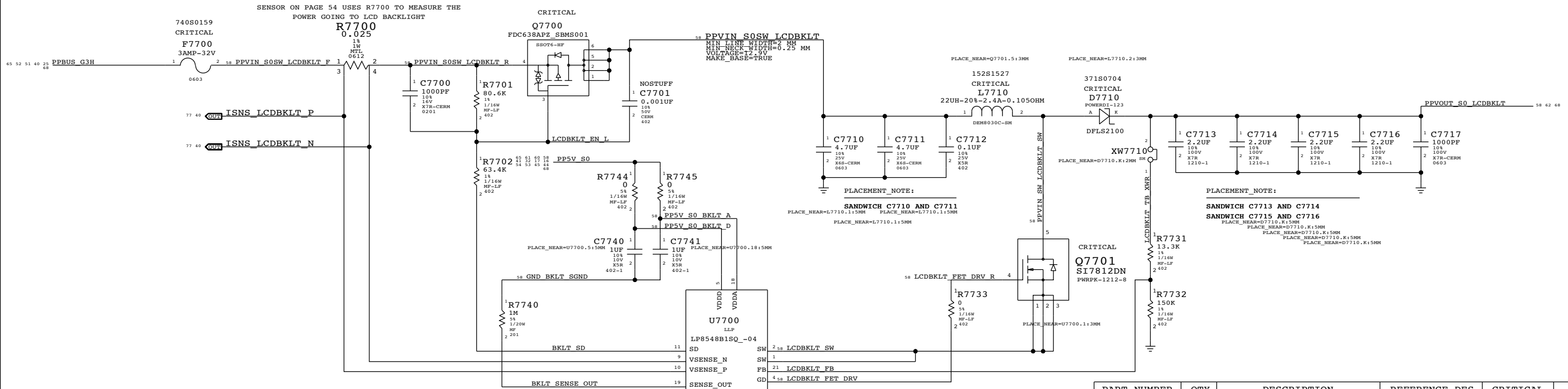
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1.05V S0 Power Supply			
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Power aliases provided by this page:

- PPVIN_S0SW_LCDBKLTFTET	(9-12.6V LCD BACKLIGHT INPUT)
- PPSV_S0_BKLT	(5V BACKLIGHT DRIVER INPUT)
- PPSV_S0SW_KBDLED	(5V KEYBOARD BACKLIGHT INPUT)

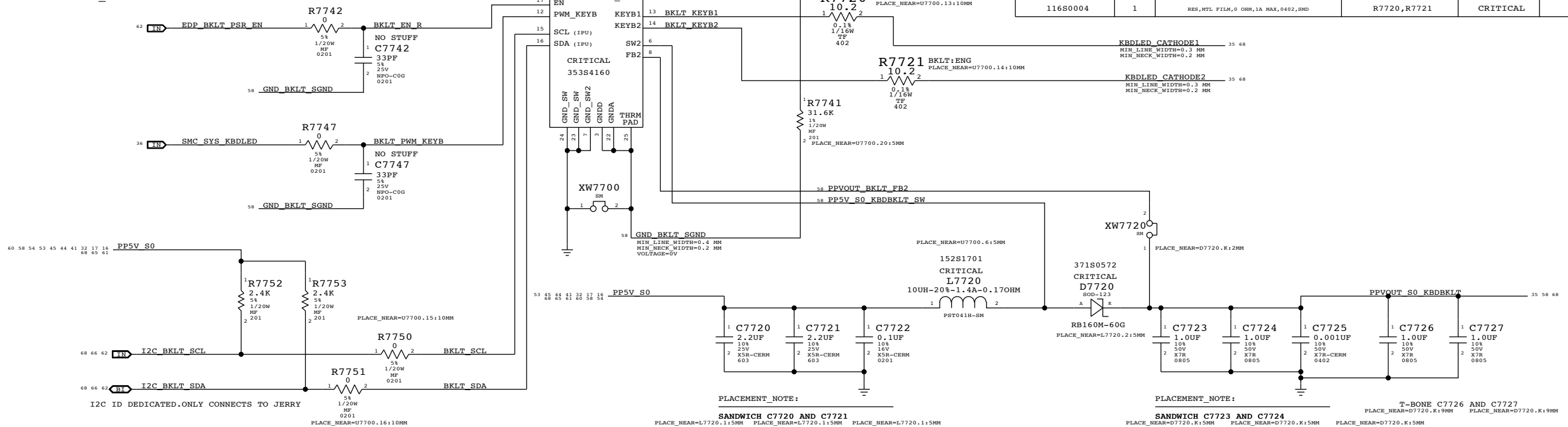
BOM options provided by this page:

BKLT:ENG - Stuffs 10.2 ohm series R for engineering build
BKLT:PROD - Stuffs 0 ohm series R for production

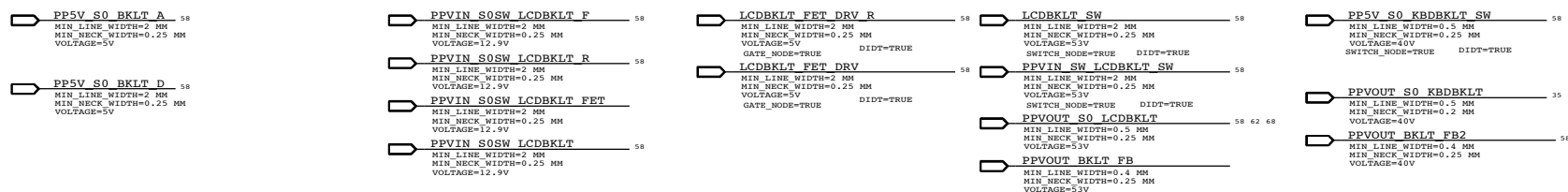



PLATFORM_RESET NO LONGER GATES THE BKLT_EN AS BOTH COME FROM PCH NOW

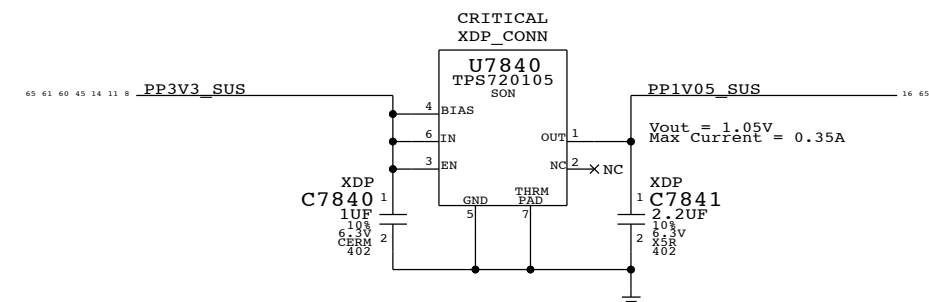
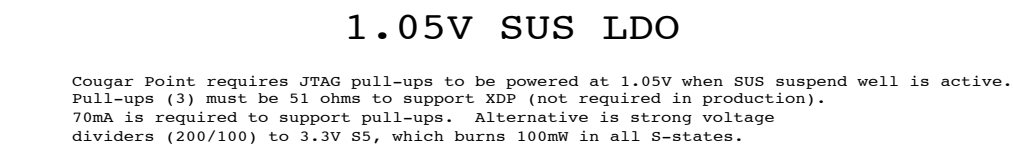
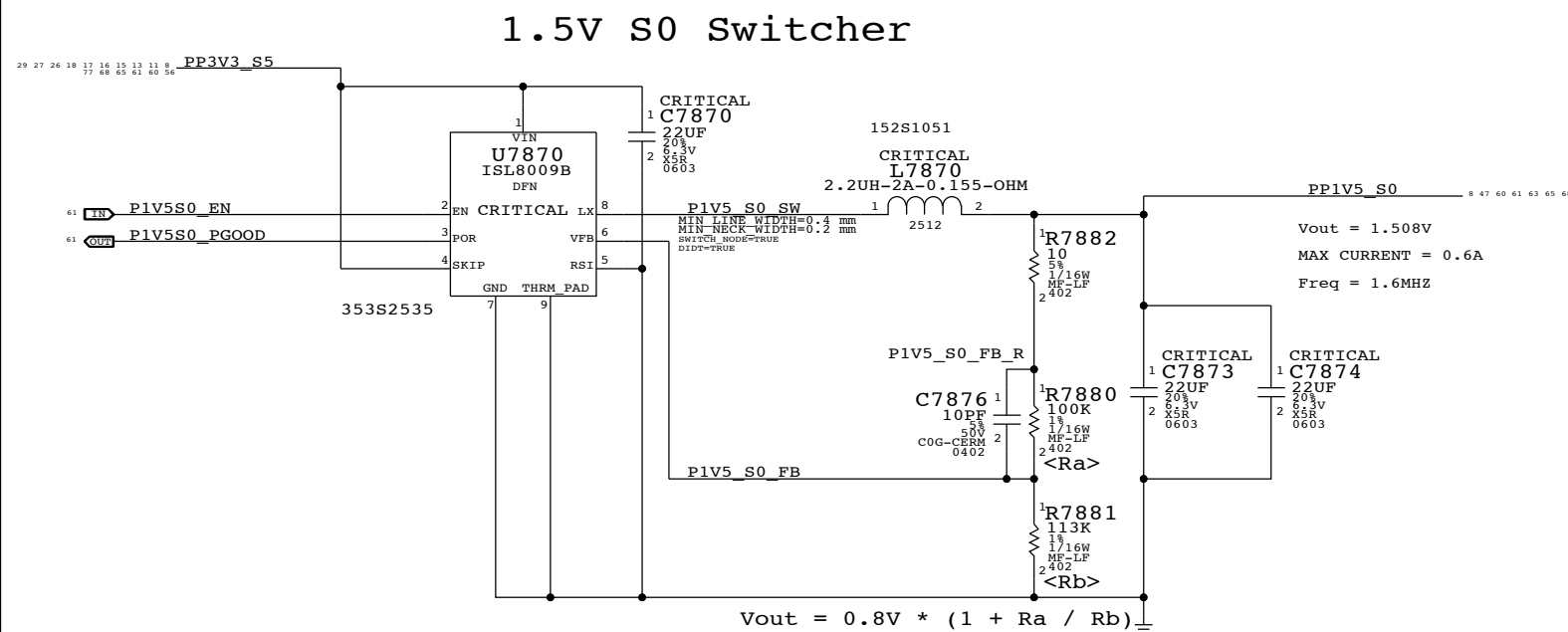
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,NTL FILM,0 OHM,1A MAX,0402,SMD	R7720,R7721	CRITICAL	BKLT:PROD

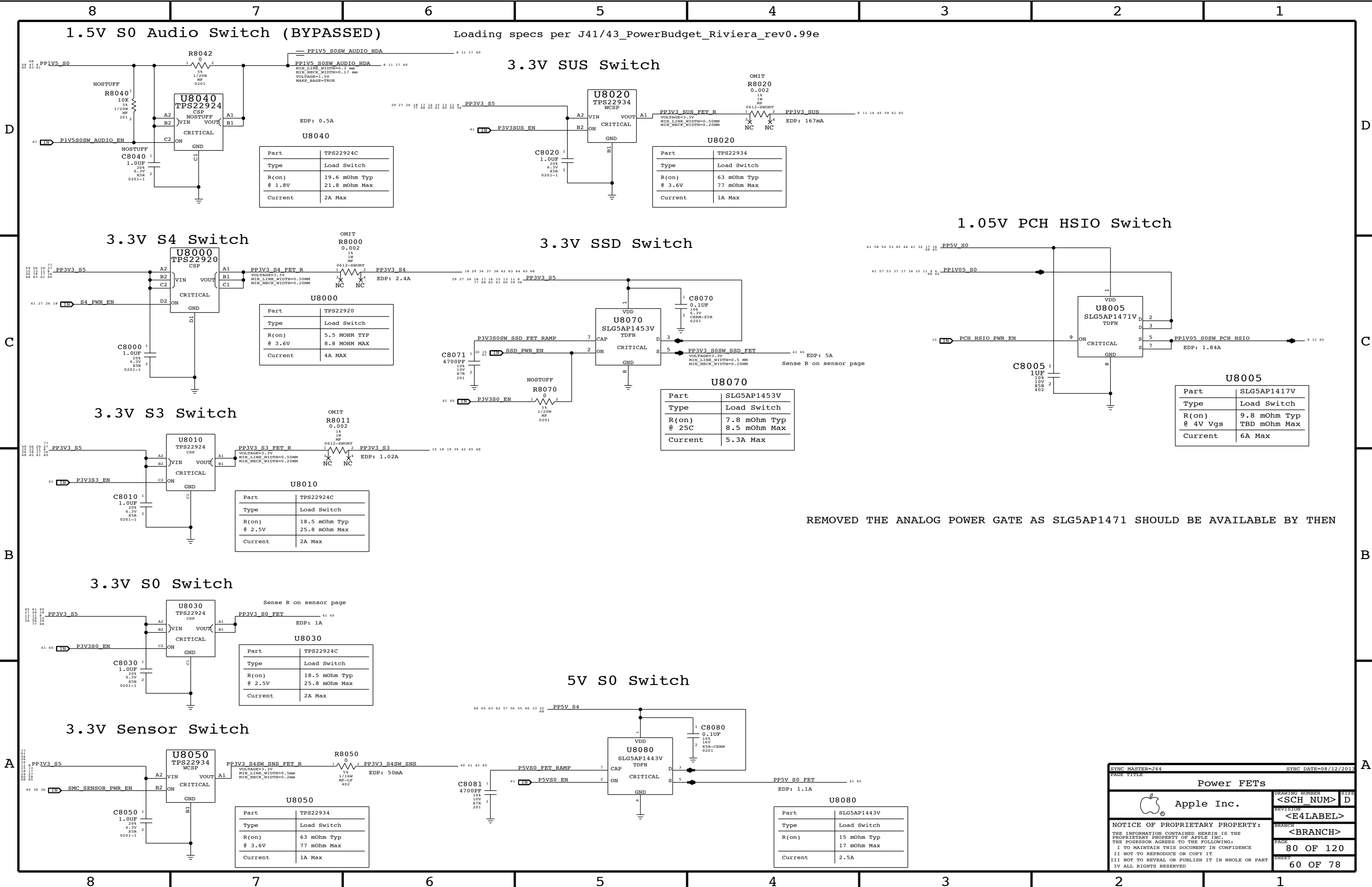


KBD BKLT LINE WIDTHS



SYMC MASTER=J44		SYMC DATE=08/12/2013	
PAGE TITLE		PAGE TOTAL	
LCD AND KBD BKLT DRIVER			
 Apple Inc.		DRAWING NUMBER <SCH NUM>	
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Loading specs per J41/43_PowerBudget_Riviera_rev0.99e

3.3V SUS Switch

Part	TPS22934
Type	Load Switch
R(on) @ 3.6V	63 mOhm Typ 77 mOhm Max
Current	1A Max

Part	TPS22934
Type	Load Switch
R(on) @ 3.6V	63 mOhm Typ 77 mOhm Max
Current	1A Max


1.05V PCH HSIO Switch

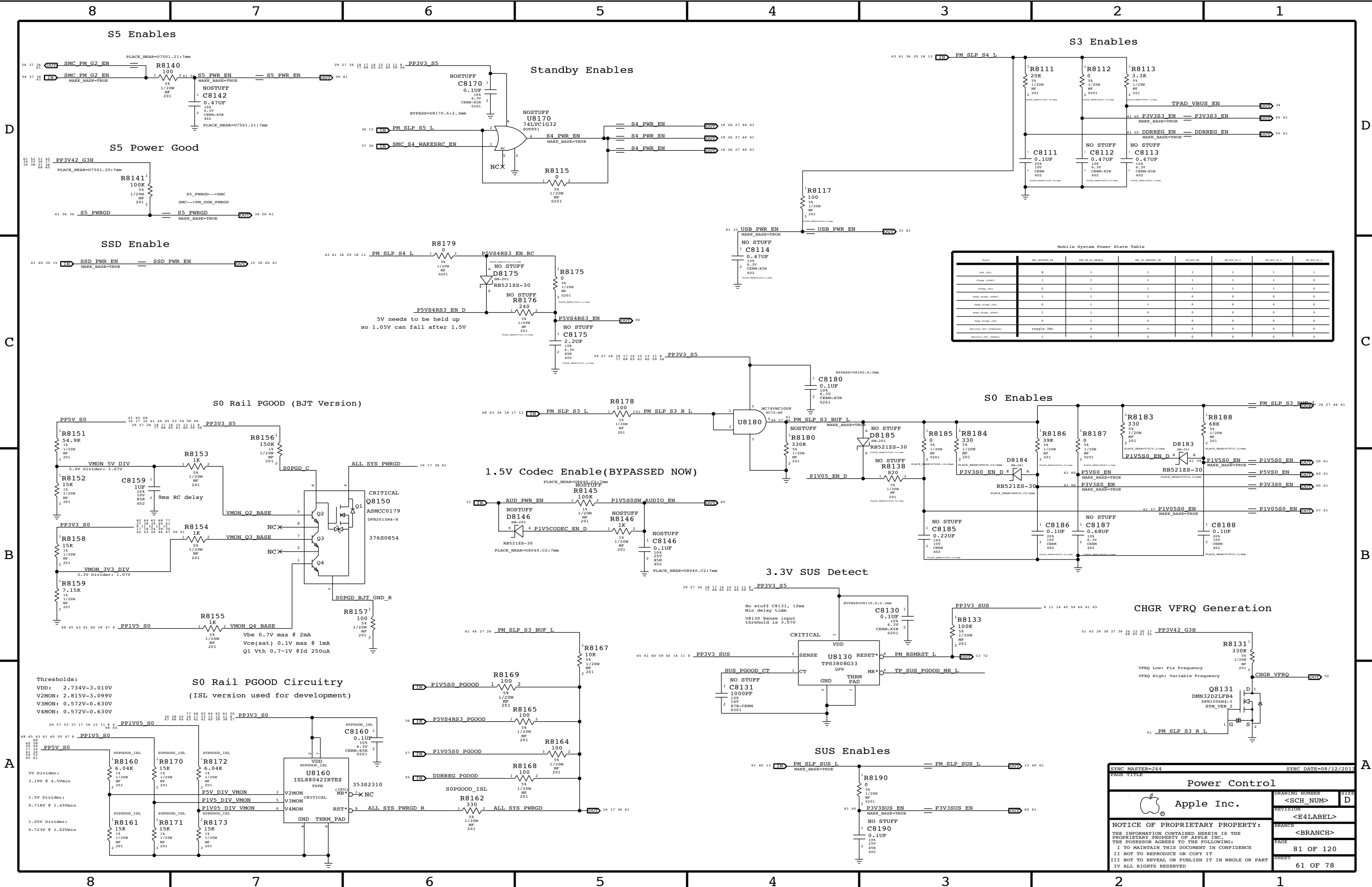
Part	SLG5AP1471V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ TBD mOhm Max
Current	6A Max

REMOVED THE ANALOG POWER GATE AS SLG5AP1471 SHOULD BE AVAILABLE BY THEN

5V S0 Switch

Part	SLG5AP1443V
Type	Load Switch
R(on) @ 2.5V	15 mOhm Typ 17 mOhm Max
Current	2.5A

SYNC MASTER=J44		SYNC DATE=08/12/2013	
PAGE TITLE			
Power FETs			
	Apple Inc.	DRAWING NUMBER	SIZE
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Mobile System Power State Table

STATE	SMC_PMCEN_EN	SMC_PMCEN_DISABLE	SMC_PMCEN_DISABLE	PM_PMCEN	PM_PMCEN_P1_L	PM_PMCEN_P1_L	PM_PMCEN_P1_L
Wakeup (S0)	X			1	1	1	1
Slamp (S0)	1	1	1	1	1	1	0
Slamp (S0)	0	1	1	1	1	1	0
Slamp (S0)	1	1	1	0	0	0	0
Slamp (S0)	0	1	1	0	0	0	0
Slamp (S0)	1	1	0	0	0	0	0
Slamp (S0)	0	1	0	0	0	0	0
Battery off (S0)	toggle 38z	0	0	0	0	0	0
Battery off (S0)	1	0	0	0	0	0	0

Thresholds:
VDD: 2.734V-3.010V
V2MON: 2.815V-3.099V
V3MON: 0.572V-0.630V
V4MON: 0.572V-0.630V

SYNC MASTER=J44

SYNC DATE=08/12/2013

Power Control

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LCD PANEL INTERFACE (eDP)
NEEDS FINAL CHECK AGAINST UPDATE FOR NEW PANEL

Panel uses EDP_PANEL_PWR_PSR_EN to discharge the LCD before power goes away

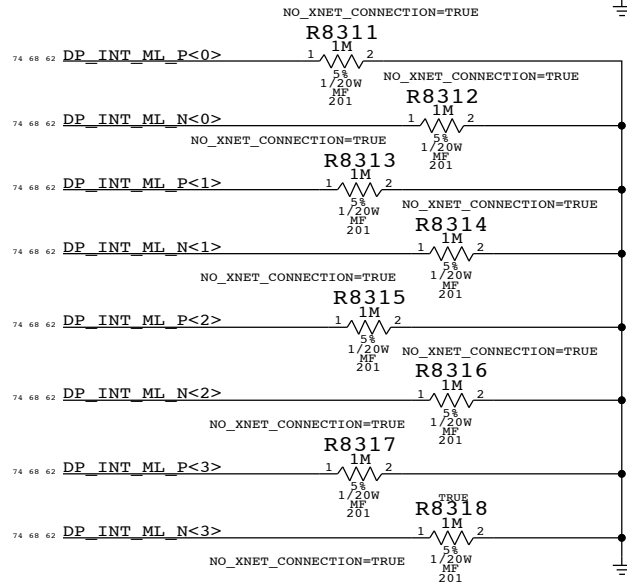
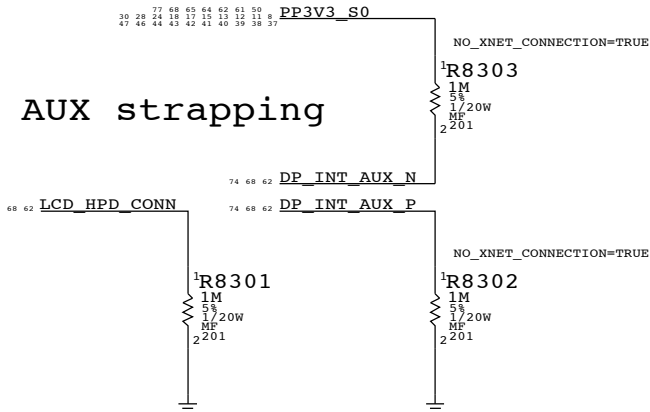
LCD Panel HPD & AUX strapping


Part	SLG5AP1443V
Type	Load Switch
R(on)	15 mOhm Typ 17 mOhm Max
Current	2.5A

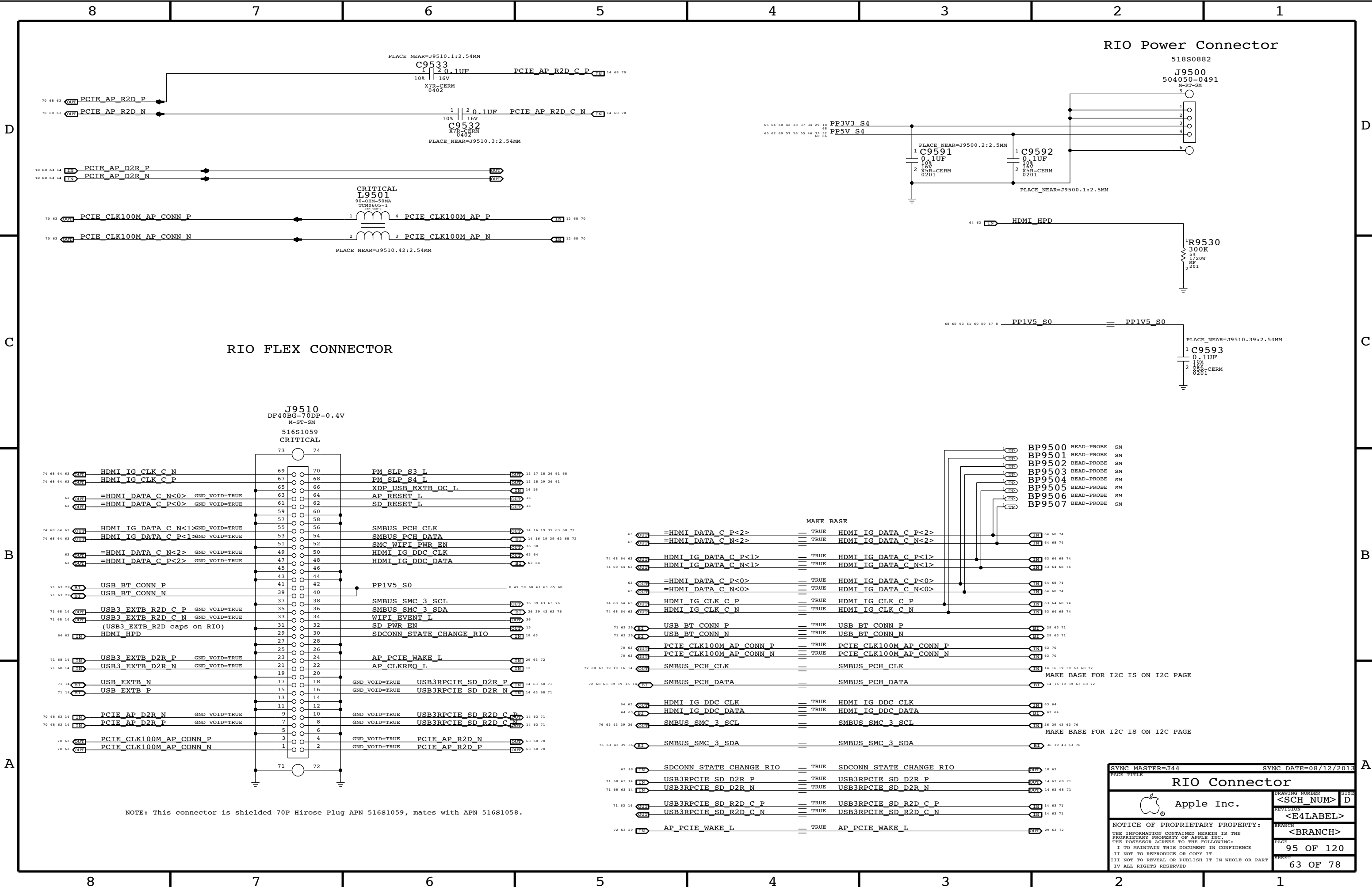
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Part	SLG5AP1443V
Type	Load Switch
R(on)	15 mOhm Typ 17 mOhm Max
Current	2.5A

LCD Panel HPD & AUX strapping



SYNC MASTER#J44	SYNC DATE=08/12/2013
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eDP Display Connector	
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NOTE: This connector is shielded 70P Hirose Plug APN 516S1059, mates with APN 516S1058.

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RIO Connector

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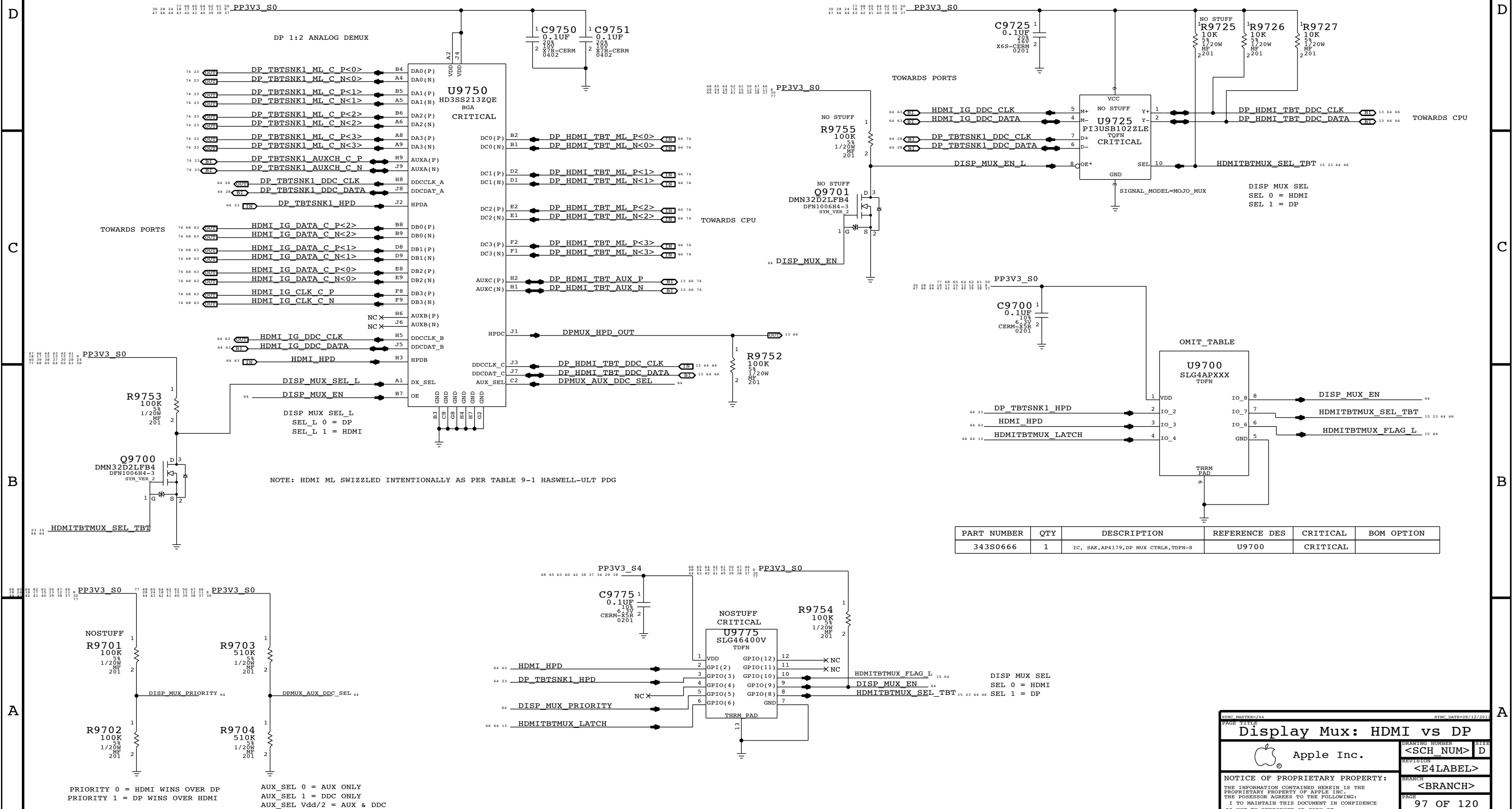
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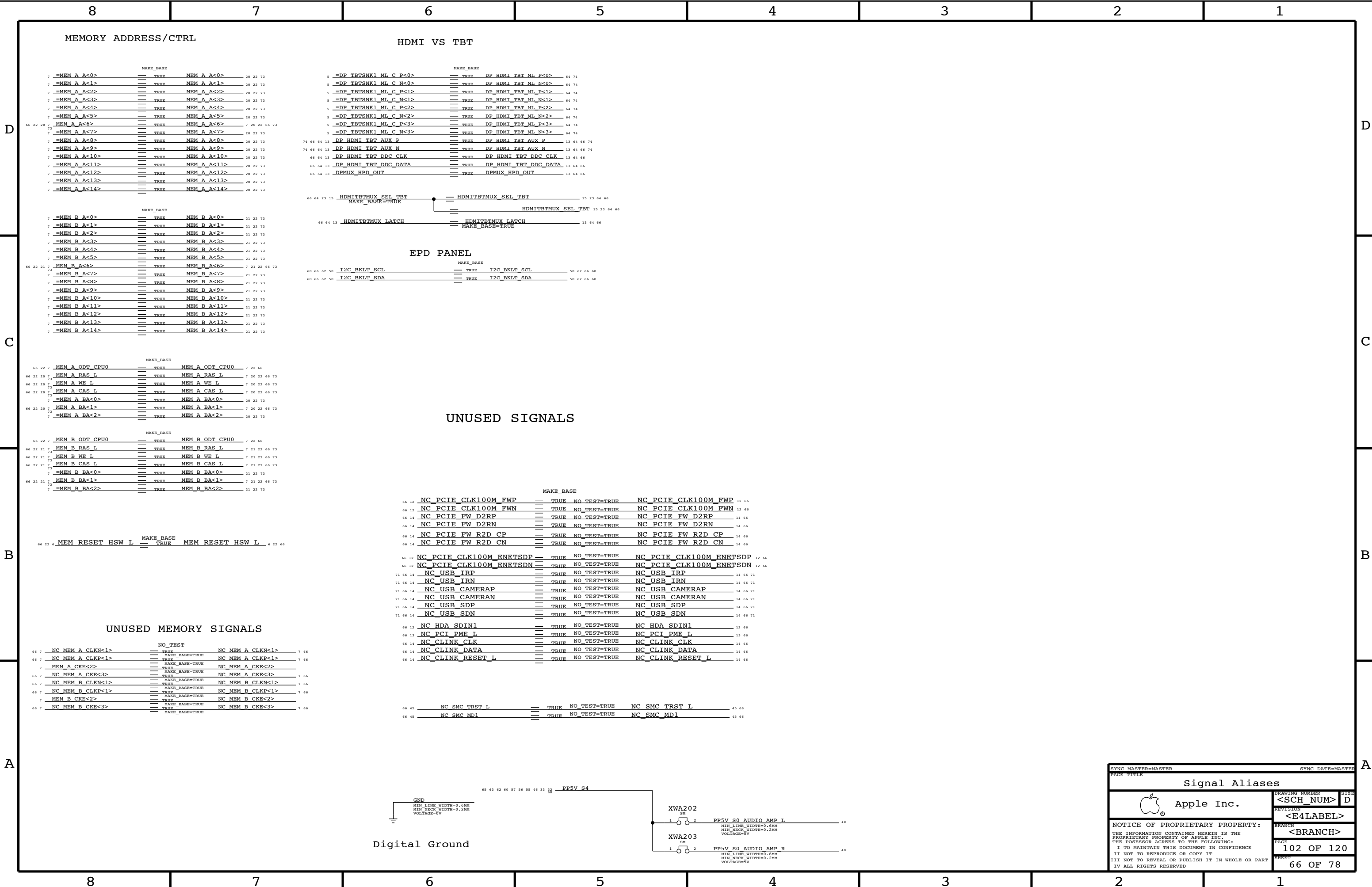
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DISPLAY MUX: DP OR HDMI





UNUSED MEMORY SIGNALS

66 7

==NC_MEM A_CLKN<1>

==NC_MEM A_CLKP<1>

==MEM A_CKE<2>

==NC_MEM A_CKE<3>

==NC_MEM B_CLKN<1>

==NC_MEM B_CLKP<1>

==MEM B_CKE<2>

==NC_MEM B_CKE<3>

==TRUE

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NC_MEM A_CLKP<1>

NC_MEM A_CKE<2>

NC_MEM A_CKE<3>

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NC_MEM B_CLKP<1>

NC_MEM B_CKE<2>

NC_MEM B_CKE<3>

7 66

UNUSED SIGNALS

66 12

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==NC_PCIE_CLK100M_FWN

==NC_PCIE_FW_D2RP

==NC_PCIE_FW_D2RN

==NC_PCIE_FW_R2D_CP

==NC_PCIE_FW_R2D_CN

==NC_PCIE_CLK100M_ENETSDP

==NC_PCIE_CLK100M_ENETSDN

==NC_USB_IRP

==NC_USB_IRN

==NC_USB_CAMERAP

==NC_USB_CAMERAN

==NC_USB_SDP

==NC_USB_SDN

==NC_HDA_SDIN1

==NC_PCI_PME_L

==NC_CLINK_CLK

==NC_CLINK_DATA

==NC_CLINK_RESET_L

==NC_SMC_TRST_L

==NC_SMC_MD1

==TRUE

NO_TEST=TRUE

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NC_PCIE_CLK100M_FWN

NC_PCIE_FW_D2RP

NC_PCIE_FW_D2RN

NC_PCIE_FW_R2D_CP

NC_PCIE_FW_R2D_CN

NC_PCIE_CLK100M_ENETSDP

NC_PCIE_CLK100M_ENETSDN

NC_USB_IRP

NC_USB_IRN

NC_USB_CAMERAP

NC_USB_CAMERAN

NC_USB_SDP

NC_USB_SDN

NC_HDA_SDIN1

NC_PCI_PME_L

NC_CLINK_CLK

NC_CLINK_DATA

NC_CLINK_RESET_L

NC_SMC_TRST_L

NC_SMC_MD1

12 66

HDMI VS TBT

5

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==DP_TBTSNK1_ML_C_N<2>

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==DP_TBTSNK1_ML_C_N<3>

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==DP_HDMI_TBT_AUX_N

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==DP_HDMI_TBT_DDC_DATA

==DPMUX_HPD_OUT

==TRUE

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DP_HDMI_TBT_ML_N<1>

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DP_HDMI_TBT_ML_N<3>

DP_HDMI_TBT_AUX_P

DP_HDMI_TBT_AUX_N

DP_HDMI_TBT_DDC_CLK

DP_HDMI_TBT_DDC_DATA

DPMUX_HPD_OUT

64 74

66 64 13

==HDMI_TBTMUX_SEL_TBT

==HDMI_TBTMUX_LATCH

==TRUE

HDMI_TBTMUX_SEL_TBT

HDMI_TBTMUX_LATCH

15 23 64 66

EPD PANEL

68 66 62 58

==I2C_BKLT_SCL

==I2C_BKLT_SDA

==TRUE

I2C_BKLT_SCL

I2C_BKLT_SDA

58 62 66 68

66 64 23 15

==HDMI_TBTMUX_SEL_TBT

==HDMI_TBTMUX_LATCH

==TRUE

HDMI_TBTMUX_SEL_TBT

HDMI_TBTMUX_LATCH

15 23 64 66

Digital Ground

45 63 62 60 57 56 55 46 33 32

==PP5V_S4

==GND

==XWA202

==XWA203

MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V

1 2

PP5V_S0_AUDIO_AMP_L

48

1 2

PP5V_S0_AUDIO_AMP_R

48

87654321

Signal Aliases

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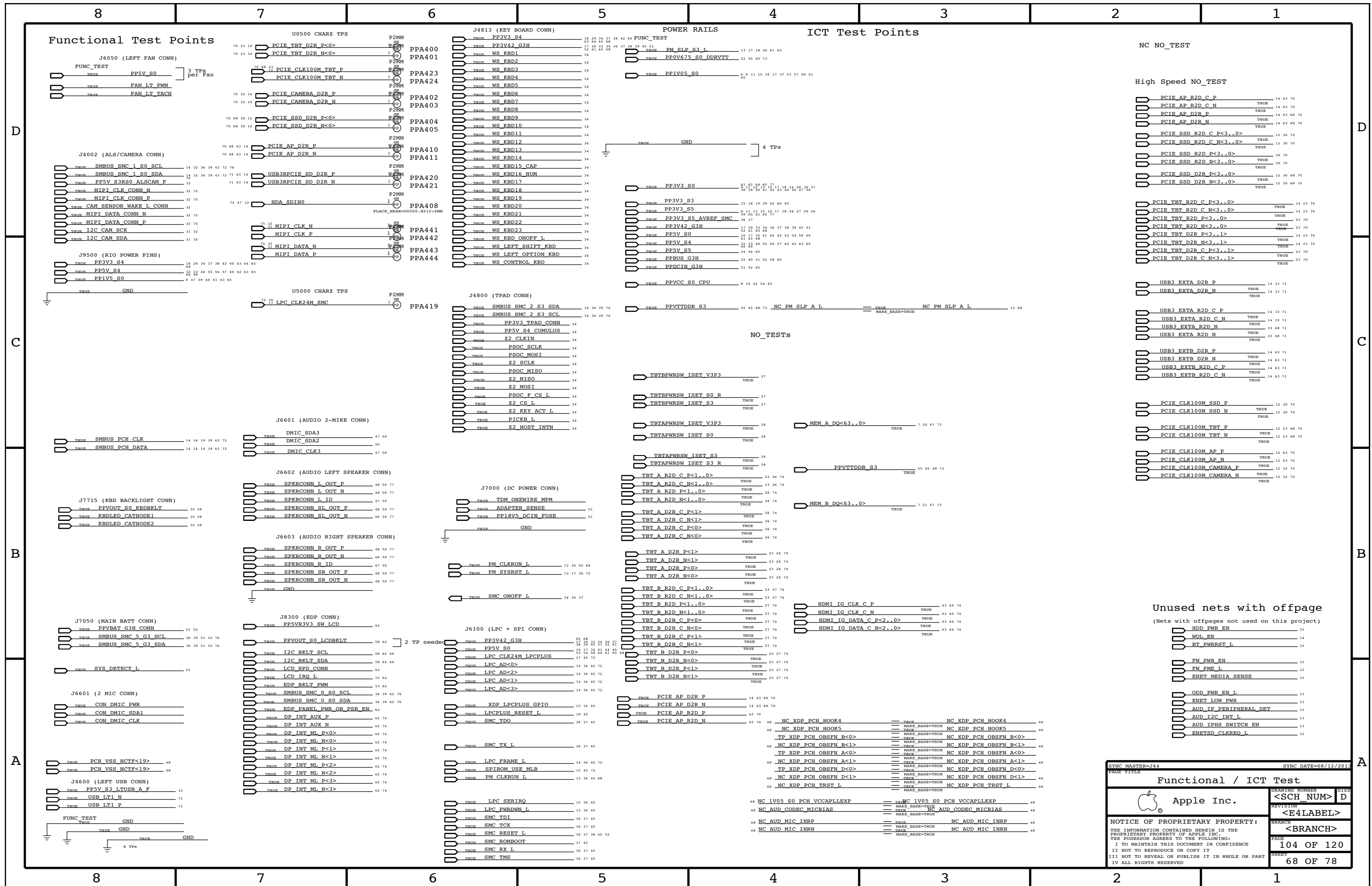
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8	7	6	5	4	3	2	1
Memory Bit/Byte Swizzle							
HAKE_BASE							
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73 68 7	TRUE	MEM A DQ<33>	=	MEM A DQ<24>	20		
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73 68 7	TRUE	MEM A DQ<63>	=	MEM A DQ<5>	20		
73 7	TRUE	MEM A DQS P<0>	=	MEM A DQS P<7>	20		
73 7	TRUE	MEM A DQS N<0>	=	MEM A DQS N<7>	20		
73 7	TRUE	MEM A DQS P<1>	=	MEM A DQS P<5>	20		
73 7	TRUE	MEM A DQS N<1>	=	MEM A DQS N<5>	20		
73 7	TRUE	MEM A DQS P<2>	=	MEM A DQS P<2>	20		
73 7	TRUE	MEM A DQS N<2>	=	MEM A DQS N<2>	20		
73 7	TRUE	MEM A DQS P<3>	=	MEM A DQS P<4>	20		
73 7	TRUE	MEM A DQS N<3>	=	MEM A DQS N<4>	20		
73 7	TRUE	MEM A DQS P<4>	=	MEM A DQS P<3>	20		
73 7	TRUE	MEM A DQS N<4>	=	MEM A DQS N<3>	20		
73 7	TRUE	MEM A DQS P<5>	=	MEM A DQS P<1>	20		
73 7	TRUE	MEM A DQS N<5>	=	MEM A DQS N<1>	20		
73 67 20 7	TRUE	MEM A DQS P<6>	=	MEM A DQS P<6>	7 20 67 73		
73 67 20 7	TRUE	MEM A DQS N<6>	=	MEM A DQS N<6>	7 20 67 73		
73 7	TRUE	MEM A DQS P<7>	=	MEM A DQS P<0>	20		
73 7	TRUE	MEM A DQS N<7>	=	MEM A DQS N<0>	20		
HAKE_BASE							
73 68 7	TRUE	MEM B DQ<0>	=	MEM B DQ<8>	21		
73 68 7	TRUE	MEM B DQ<1>	=	MEM B DQ<14>	21		
73 68 7	TRUE	MEM B DQ<2>	=	MEM B DQ<11>	21		
73 68 7	TRUE	MEM B DQ<3>	=	MEM B DQ<9>	21		
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73 68 7	TRUE	MEM B DQ<5>	=	MEM B DQ<10>	21		
73 68 7	TRUE	MEM B DQ<6>	=	MEM B DQ<15>	21		
73 68 7	TRUE	MEM B DQ<7>	=	MEM B DQ<13>	21		
73 68 7	TRUE	MEM B DQ<8>	=	MEM B DQ<24>	21		
73 68 7	TRUE	MEM B DQ<9>	=	MEM B DQ<30>	21		
73 68 7	TRUE	MEM B DQ<10>	=	MEM B DQ<29>	21		
73 68 7	TRUE	MEM B DQ<11>	=	MEM B DQ<27>	21		
73 68 7	TRUE	MEM B DQ<12>	=	MEM B DQ<28>	21		
73 68 7	TRUE	MEM B DQ<13>	=	MEM B DQ<26>	21		
73 68 7	TRUE	MEM B DQ<14>	=	MEM B DQ<25>	21		
73 68 7	TRUE	MEM B DQ<15>	=	MEM B DQ<31>	21		
73 68 7	TRUE	MEM B DQ<16>	=	MEM B DQ<5>	21		
73 68 7	TRUE	MEM B DQ<17>	=	MEM B DQ<1>	21		
73 68 7	TRUE	MEM B DQ<18>	=	MEM B DQ<6>	21		
73 68 7	TRUE	MEM B DQ<19>	=	MEM B DQ<3>	21		
73 68 7	TRUE	MEM B DQ<20>	=	MEM B DQ<4>	21		
73 68 7	TRUE	MEM B DQ<21>	=	MEM B DQ<7>	21		
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73 68 7	TRUE	MEM B DQ<24>	=	MEM B DQ<21>	21		
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73 68 7	TRUE	MEM B DQ<26>	=	MEM B DQ<20>	21		
73 68 7	TRUE	MEM B DQ<27>	=	MEM B DQ<22>	21		
73 68 7	TRUE	MEM B DQ<28>	=	MEM B DQ<23>	21		
73 68 7	TRUE	MEM B DQ<29>	=	MEM B DQ<19>	21		
73 68 7	TRUE	MEM B DQ<30>	=	MEM B DQ<18>	21		
73 68 7	TRUE	MEM B DQ<31>	=	MEM B DQ<16>	21		
73 68 7	TRUE	MEM B DQ<32>	=	MEM B DQ<32>	7 21 67 68 73		
73 68 7	TRUE	MEM B DQ<33>	=	MEM B DQ<40>	21		
73 68 7	TRUE	MEM B DQ<34>	=	MEM B DQ<45>	21		
73 68 7	TRUE	MEM B DQ<35>	=	MEM B DQ<43>	21		
73 68 7	TRUE	MEM B DQ<36>	=	MEM B DQ<46>	21		
73 68 7	TRUE	MEM B DQ<37>	=	MEM B DQ<42>	21		
73 68 7	TRUE	MEM B DQ<38>	=	MEM B DQ<47>	21		
73 68 7	TRUE	MEM B DQ<39>	=	MEM B DQ<41>	21		
73 68 7	TRUE	MEM B DQ<40>	=	MEM B DQ<60>	21		
73 68 7	TRUE	MEM B DQ<41>	=	MEM B DQ<56>	21		
73 68 7	TRUE	MEM B DQ<42>	=	MEM B DQ<63>	21		
73 68 7	TRUE	MEM B DQ<43>	=	MEM B DQ<61>	21		
73 68 7	TRUE	MEM B DQ<44>	=	MEM B DQ<62>	21		
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73 68 7	TRUE	MEM B DQ<46>	=	MEM B DQ<59>	21		
73 68 7	TRUE	MEM B DQ<47>	=	MEM B DQ<57>	21		
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73 68 7	TRUE	MEM B DQ<49>	=	MEM B DQ<37>	21		
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73 7	TRUE	MEM B DQS P<2>	=	MEM B DQS P<0>	21		
73 7	TRUE	MEM B DQS N<2>	=	MEM B DQS N<0>	21		
73 7	TRUE	MEM B DQS P<3>	=	MEM B DQS P<2>	21		
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73 7	TRUE	MEM B DQS N<4>	=	MEM B DQS N<5>	21		
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73 7	TRUE	MEM B DQS N<5>	=	MEM B DQS N<7>	21		
73 67 21 7	TRUE	MEM B DQS P<6>	=	MEM B DQS P<6>	7 21 67 73		
73 67 21 7	TRUE	MEM B DQS N<6>	=	MEM B DQS N<6>	7 21 67 73		
73 7	TRUE	MEM B DQS P<7>	=	MEM B DQS P<6>	21		
73 7	TRUE	MEM B DQS N<7>	=	MEM B DQS N<6>	21		

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Memory Bit/Byte Swizzle			
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J44 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS				BOARD AREAS		BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA, P65BGA, BGA_MEM		MM	16.5
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.095 MM	0.095 MM			
50_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP, BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.083 MM	0.083 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.102 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.118 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.186 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	ISL2, ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	TOP, BOTTOM	Y	0.146 MM	0.146 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2, ISL11	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.125 MM		0.155 MM	0.155 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	ISL2, ISL11	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	TOP, BOTTOM	Y	0.105 MM	0.105 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2, ISL11	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.101 MM	0.101 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P65_BGA	*	Y	0.071MM	0.071MM		0.075MM	0.126MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1T01_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE
*	*	P65BGA	P075_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
P072_SPACE	*	0.071 MM	?
P075_SPACE	*	0.075 MM	?


Stackup-Defined Spacing Rules

Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	-	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1X_DIELECTRIC	TOP, BOTTOM	0.058 MM	?
1X_DIELECTRIC	ISL3, ISL4, ISL9, ISL10	0.053 MM	?
1X_DIELECTRIC	ISL2, ISL11, ISL6, ISL7, ISL8, ISL11	0.101 MM	?

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	P65BGA	P65_BGA

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PCB Rule Definitions			
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USB 2 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIA5	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4X_DIELECTRIC	?	USB	TOP,BOTTOM	=6X_DIELECTRIC	?
USB_RBIA5	*	=6X_DIELECTRIC	?	USB_RBIA5	TOP,BOTTOM	=10X_DIELECTRIC	?

USB 3 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	*	=3X_DIELECTRIC	?	USB3_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
USB3_TXRX	*	=6X_DIELECTRIC	?	USB3_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
USB3_2OTHER	*	=4X_DIELECTRIC	?	USB3_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_*	*	*	USB3_2OTHER
USB3_*	=SAME	*	USB3_2SAME
USB3_TX	*_RX	*	USB3_TXRX
USB3_RX	*_TX	*	USB3_TXRX

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_25M	*	=5x_DIELECTRIC	?











































SATA Interface Constraints (Not Used)

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	*	=3X_DIELECTRIC	?	SATA_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
SATA_TXRX	*	=6X_DIELECTRIC	?	SATA_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
SATA_2OTHER	*	=4X_DIELECTRIC	?	SATA_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA_*	*	*	SATA_2OTHER
SATA_*	=SAME	*	SATA_2SAME
SATA_TX	*_RX	*	SATA_TXRX
SATA_RX	*_TX	*	SATA_TXRX

USB Constraints

ELECTRICAL CONST SET		NET TYPE			
		PHYSICAL	SPACING		
	USB_BT	USB_85D	USB	USB_BT_P	14 29
	USB_BT	USB_85D	USB	USB_BT_N	14 29
	USB_BT	USB_85D	USB	USB_BT_CONN_P	29 63
	USB_BT	USB_85D	USB	USB_BT_CONN_N	29 63
	USB_EXT_A	USB_85D	USB	USB_EXT_A_P	14 33
	USB_EXT_A	USB_85D	USB	USB_EXT_A_N	14 33
		DEFAULT	DEFAULT	SMC_DEBUGPRT_RX_L	33
		DEFAULT	DEFAULT	SMC_DEBUGPRT_TX_L	33
	USB_EXT_A	USB_85D	USB	USB2_EXT_A_MUXED_P	33
	USB_EXT_A	USB_85D	USB	USB2_EXT_A_MUXED_N	33
	USB_EXT_A	USB_85D	USB	USB2_EXT_A_MUXED_F_P	33
	USB_EXT_A	USB_85D	USB	USB2_EXT_A_MUXED_F_N	33
	USB_EXT_A	USB_85D	USB	USB_LT1_P	68
	USB_EXT_A	USB_85D	USB	USB_LT1_N	68
	USB_EXTB	USB_85D	USB	USB_EXTB_P	14 63
	USB_EXTB	USB_85D	USB	USB_EXTB_N	14 63
	USB_TPAD	USB_85D	USB	USB_TPAD_P	14 34
	USB_TPAD	USB_85D	USB	USB_TPAD_N	14 34
	USB_TPAD	USB_85D	USB	USB_TPAD_R_P	34
	USB_TPAD	USB_85D	USB	USB_TPAD_R_N	34
	USB3_EXT_A_D2R	USB_85D	USB3_RX	USB3_EXT_A_D2R_P	14 33
	USB3_EXT_A_D2R	USB_85D	USB3_RX	USB3_EXT_A_D2R_N	14 33
	USB3_EXT_A_R2D	USB_85D	USB3_TX	USB3_EXT_A_R2D_P	33
	USB3_EXT_A_R2D	USB_85D	USB3_TX	USB3_EXT_A_R2D_N	33 68
	USB3_EXT_A_R2D	USB_85D	USB3_TX	USB3_EXT_A_R2D_C_P	14 33
	USB3_EXT_A_R2D	USB_85D	USB3_TX	USB3_EXT_A_R2D_C_N	14 33
	USB3_EXTB_D2R	USB_85D	USB3_RX	USB3_EXTB_D2R_P	14 63
	USB3_EXTB_D2R	USB_85D	USB3_RX	USB3_EXTB_D2R_N	14 63
	USB3_EXTB_R2D	USB_85D	USB3_TX	USB3_EXTB_R2D_C_P	14 63
	USB3_EXTB_R2D	USB_85D	USB3_TX	USB3_EXTB_R2D_C_N	14 63
	USB3_SD_D2R	USB3_85D	USB3_RX	USB3RPCIE_SD_D2R_P	14 63
	USB3_SD_D2R	USB3_85D	USB3_RX	USB3RPCIE_SD_D2R_N	14 63
	USB3_SD_R2D	USB3_85D	USB3_TX	USB3RPCIE_SD_R2D_C_P	14 63
	USB3_SD_R2D	USB3_85D	USB3_TX	USB3RPCIE_SD_R2D_C_N	14 63
	USB_NC	USB_85D	USB	NC_USB_IRP	14 66
	USB_NC	USB_85D	USB	NC_USB_IRN	14 66
	USB_NC	USB_85D	USB	TP_USB_5P	14
	USB_NC	USB_85D	USB	TP_USB_5N	14
	USB_NC	USB_85D	USB	NC_USB_SDP	14 66
	USB_NC	USB_85D	USB	NC_USB_SDN	14 66
	USB_NC	USB_85D	USB	NC_USB_CAMERAP	14 66
	USB_NC	USB_85D	USB	NC_USB_CAMERAN	14 66
	PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS	14
		SATA_85D	SATA_RX	DUMMY_SATA_D2R_P	
		SATA_85D	SATA_RX	DUMMY_SATA_D2R_N	
		SATA_85D	SATA_TX	DUMMY_SATA_R2D_P	
		SATA_85D	SATA_TX	DUMMY_SATA_R2D_N	
	SYSCLK_CLK25M	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X1	17
	SYSCLK_CLK25M	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2	17
	SYSCLK_CLK25M	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2_R	17
	SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA	17 32
	SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKP	31 32
	SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP_R	32
	SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP	32
	SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALN	32
	SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKN	31 32
	SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	17 23
	SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	23

Notes:
This is here to keep the SATA rules.

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USB Constraints

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?


PCH Single Net Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
PCH_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_12MIL	*	0.305 MM	?
PCH_15MIL	*	0.381 MM	?
PCH_18MIL	*	0.457 MM	?
PCH_20MIL	*	0.508 MM	?

PCH Net Properties

ELECTRICAL CONST SET		NET TYPE		
		PHYSICAL	SPACING	
□	LPC_AD	LPC_45S	LPC	LPC AD<3..0>
□	LPC_AD	LPC_45S	LPC	LPC FRAME_L
□	LPC_CLK24M_SMC	CLK_LPC_45S	CLK_LPC	LPC CLK24M_SMC_R
□	LPC_CLK24M_SMC	CLK_LPC_45S	CLK_LPC	LPC CLK24M_SMC
□	LPC_CLK24M_LPCPLUS	CLK_LPC_45S	CLK_LPC	LPC CLK24M_LPCPLUS
□	LPC_CLK24M_LPCPLUS	CLK_LPC_45S	CLK_LPC	LPC CLK24M_LPCPLUS_R
□	SMBUS_PCH	SMB_45S	SMB	SMBUS_PCH_CLK
□	SMBUS_PCH	SMB_45S	SMB	SMBUS_PCH_DATA
□	SML_PCH_0	SMB_45S	SMB	SML_PCH_0_CLK
□	SML_PCH_0	SMB_45S	SMB	SML_PCH_0_DATA
□		SMB_45S	SMB	SMBUS_SMC_1_S0_SCL
□		SMB_45S	SMB	SMBUS_SMC_1_S0_SDA
□	HDA_BIT_CLK	HDA_45S	HDA	HDA BIT_CLK
□	HDA_BIT_CLK	HDA_45S	HDA	HDA BIT_CLK_R
□	HDA_SYNC	HDA_45S	HDA	HDA SYNC
□	HDA_SYNC	HDA_45S	HDA	HDA SYNC_R
□	HDA_RST	HDA_45S	HDA	HDA RST_R_L
□	HDA_RST	HDA_45S	HDA	HDA RST_L
□	HDA_SDIN	HDA_45S	HDA	HDA SDIN0
□	HDA_SDIN	HDA_45S	HDA	CS4208_HDA_SDOU0_R
□	HDA_SDOU0P	HDA_45S	HDA	HDA SDOU0T
□	HDA_SDOU0T	HDA_45S	HDA	HDA SDOU0T_R
□	SPI_MLB	SPT_45S	SPT	SPI ALT_CLK
□	SPI_MLB	SPT_45S	SPT	SPI_CLK
□	SPI_MLB	SPT_45S	SPT	SPI_CLK_R
□	SPI_MLB	SPT_45S	SPT	SPI_MLB_CLK
□	SPI_MLB	SPT_45S	SPT	SPI_SMC_CLK
□	SPI_MLB	SPT_45S	SPT	SPI_ALT_CS_L
□	SPI_MLB	SPT_45S	SPT	SPI_CS0_L
□	SPI_MLB	SPT_45S	SPT	SPI_CS0_R_L
□	SPI_MLB	SPT_45S	SPT	SPI_MLB_CS_L
□	SPI_MLB	SPT_45S	SPT	SPI_SMC_CS_L
□	SPI_MLB	SPT_45S	SPT	SPI_ALT_MISO
□	SPI_MLB	SPT_45S	SPT	SPI_MISO
□	SPI_MLB	SPT_45S	SPT	SPI_MISO_R
□	SPI_MLB	SPT_45S	SPT	SPI_MLB_MISO
□	SPI_MLB	SPT_45S	SPT	SPI_SMC_MISO
□	SPI_MLB	SPT_45S	SPT	SPI_ALT_MOSI
□	SPI_MLB	SPT_45S	SPT	SPI_MOSI
□	SPI_MLB	SPT_45S	SPT	SPI_MOSI_R
□	SPI_MLB	SPT_45S	SPT	SPI_MLB_MOSI
□	SPI_MLB	SPT_45S	SPT	SPI_SMC_MOSI
□	SPI_MLB_IO2	SPT_45S	SPT	SPI_IO<2>
□	SPI_MLB_IO2	SPT_45S	SPT	SPIROM_WP_L
□	SPI_MLB_IO3	SPT_45S	SPT	SPI_IO<3>
□	SPI_MLB_IO3	SPT_45S	SPT	SPIROM_HOLD_L
□	SPI_MLB_IO3	SPT_45S	SPT	SPIROM_USE_MLB
□	PCH_RTCX	PCH_45S	PCH_15MTTL	PCH_CLK32K_RTCX1
□	PCH_SRTCRCST	PCH_45S	PCH_15MTTL	PCH_SRTCRCST_L
□	PCH_RTCRCST	PCH_45S	PCH_15MTTL	RTC RESET_L
□	PCH_THRMTRIP	PCH_45S	PCH_18MTTL	PM_THRMTRIP_L
□	PCH_THRMTRIP	PCH_45S	PCH_18MTTL	PM_THRMTRIP_R_L
□		PCH_45S	PCH_15MTTL	PCH_INTRUDER_L
□		PCH_45S	PCH_15MTTL	PCH_INTVRMEN
□		PCH_45S	PCH_15MTTL	PCH_DSWVRMEN
□		PCH_45S	PCH_15MTTL	PM_RSMRST_L
□		PCH_45S	PCH_15MTTL	PM_SYSRST_L
□		PCH_45S	PCH_15MTTL	XDP_DBRESET_L
□		PCH_45S	PCH_15MTTL	PM_PCH_SYS_PWROK
□		PCH_45S	PCH_15MTTL	XDP_SYS_PWROK
□		PCH_45S	PCH_15MTTL	SYS_PWROK_R
□		PCH_45S	PCH_15MTTL	PM_PCH_PWROK
□		PCH_45S	PCH_15MTTL	PM_S0_PGOOD
□		PCH_45S	PCH_15MTTL	SMC_DELAYED_PWRGD
□		PCH_45S	PCH_15MTTL	PM_DSW_PWRGD
□		PCH_45S	PCH_15MTTL	PM_PWRBTN_L
□		PCH_45S	PCH_15MTTL	XDP_CPU_PWRBTN_L
□		PCH_45S	PCH_15MTTL	PCIE_WAKE_L
□		PCH_45S	PCH_15MTTL	AP_PCIE_WAKE_L
□		PCH_45S	PCH_15MTTL	CAM_PCIE_WAKE_L
□		PCH_45S	PCH_15MTTL	TBT_CIO_PLUG_EVENT_L
□	PCH_CLK24M_XTAL	PCH_45S	PCH_20MTTL	PCH_CLK24M_XTALIN
□	PCH_CLK24M_XTAL	PCH_45S	PCH_20MTTL	PCH_CLK24M_XTALOUT
□	PCH_CLK24M_XTAL	PCH_45S	PCH_20MTTL	PCH_CLK24M_XTALOUT_R

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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

































Memory to Power Spacing


NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

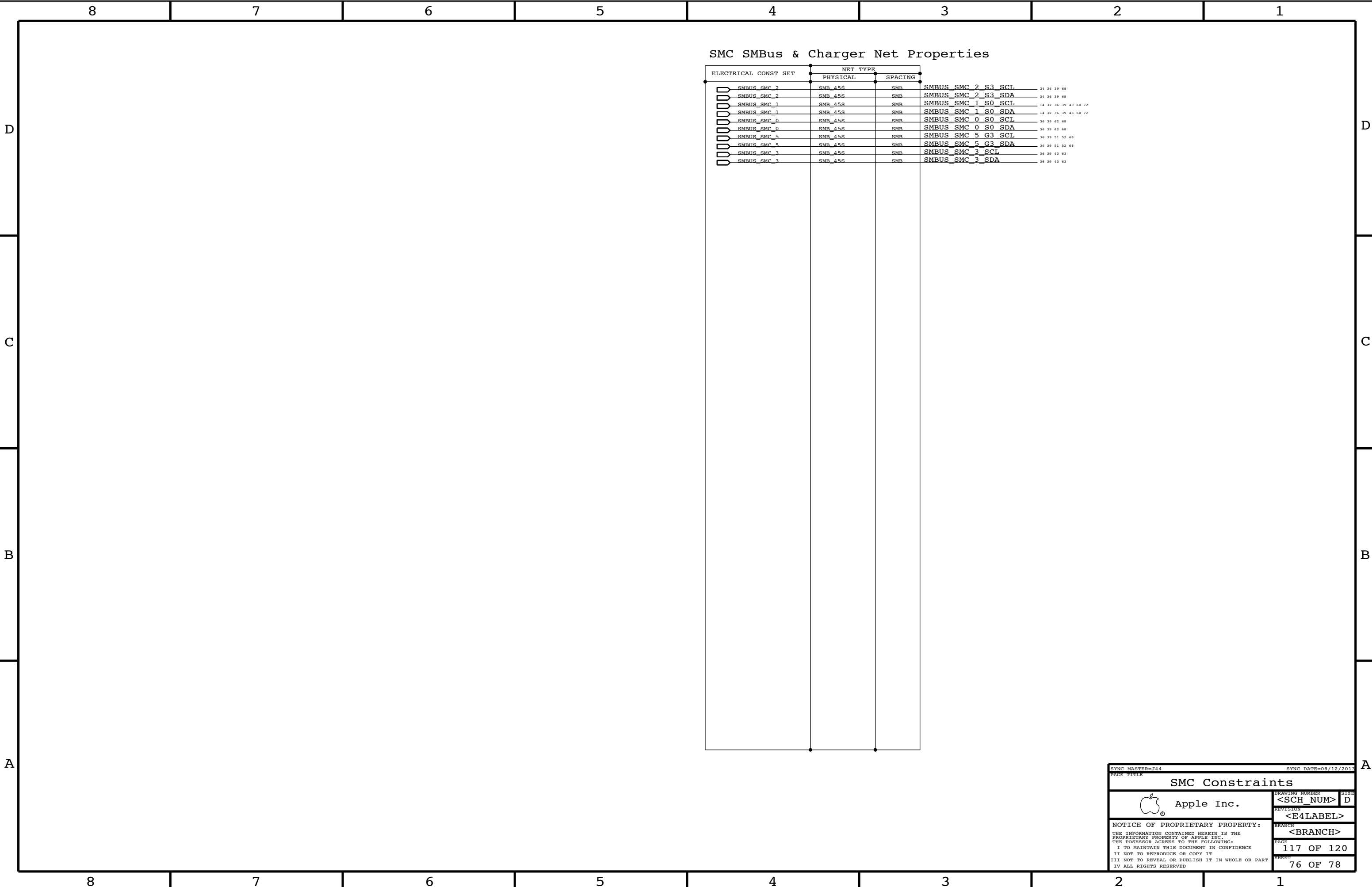
Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

ELECTRICAL CONST SET		NET TYPE			
		PHYSICAL	SPACING		
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P	31 32
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N	31 32
	S2_MEM_CKE	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE	31 32
	S2_MEM_CS	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L	31 32
	S2_MEM_CS	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT	32
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L	31 32
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L	31 32
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L	31 32
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0>	31 32
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1>	31 32
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2>	31 32
	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0>	31 32
	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0>	31 32
	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1>	31 32
	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1>	31 32
	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0>	31 32
	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1>	31 32
	S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0>	31 32
	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0>	31 32
	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8>	31 32
	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P	31 32 68
	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N	31 32 68
	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P	32 68
	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N	32 68
	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P	31 32 68
	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N	31 32 68
	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P	32 68
	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N	32 68
			S2_MEM_PWR	PP1V35_CAM	31 32
			S2_MEM_PWR	PP0V675_CAM_VREF	31 32
			S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA	32
			S2_MEM_PWR	PP0V675_MEM_CAM_VREFDO	32

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.1 MM	0.1 MM
THERM_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.1 MM	0.1 MM
DIG_AUDIO	*	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	0.1 MM	0.1 MM
ANL_AUDIO	*	=1TO1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
ANL_AUDIO_WIDE	*	=1TO1_DIFFPAIR	0.3 MM	0.3 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2X_DIELECTRIC	?
THERM	*	=2X_DIELECTRIC	?
AUDIO	*	=2X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
GND	PCIE_*	*	GND_P2MM
GND	SATA_*	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SB_POWER	SATA_*	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.070 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	10 MM OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.100 MM	500 MIL		
CPU_27P4S	BOTTOM			0.230 MM	100 MIL		
USB3_85D	TOP			0.100 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

DDR3 Loaded Segment Constraint Relaxations

Alternate single ended and differential impedances between devices.

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_40S	BGA_MEM	MEM_45S
MEM_72D	BGA_MEM	MEM_85D

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.100 MM	6.35 MM		

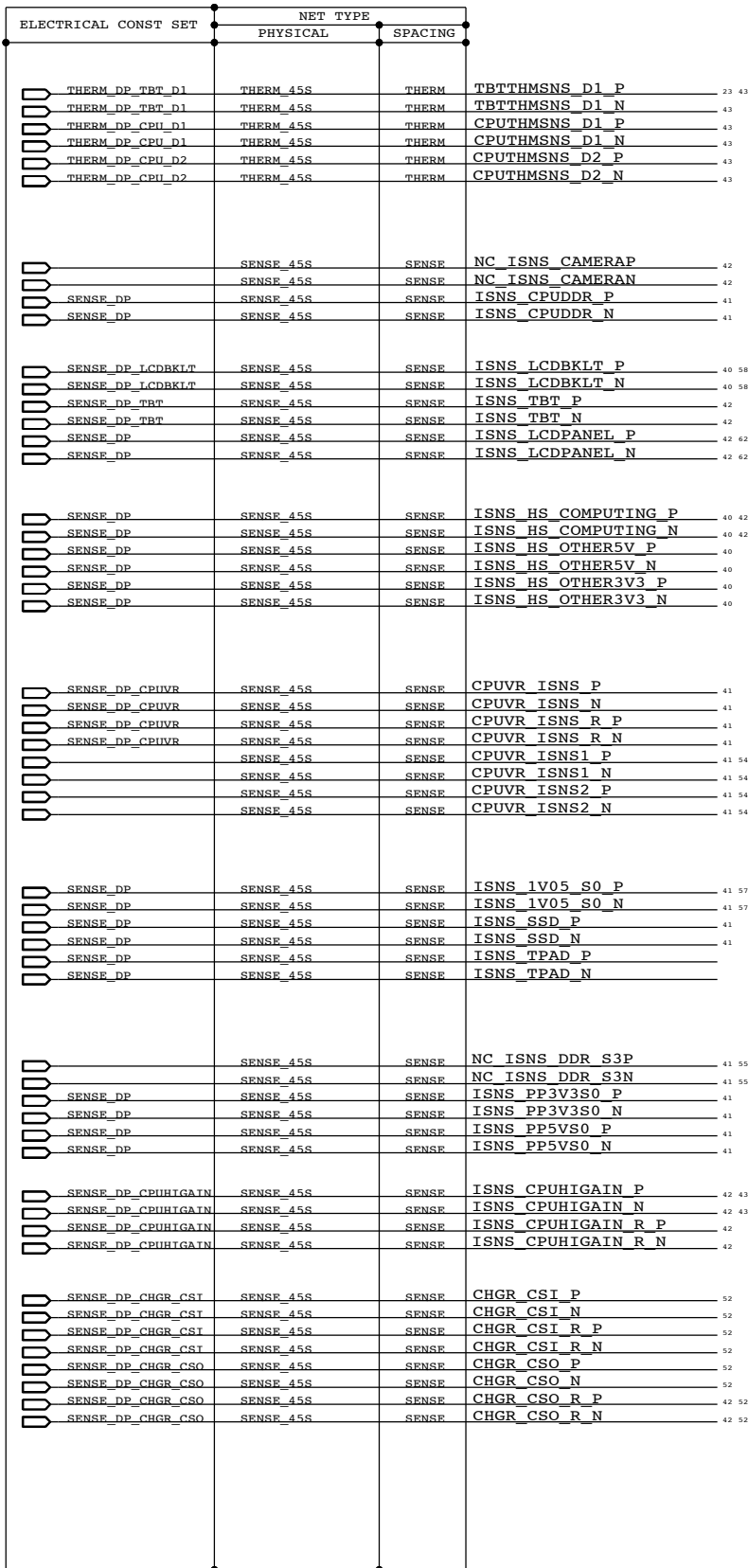
DP, SATA, HDMI, PCIE CONSTRAINT RELAXATIONS

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

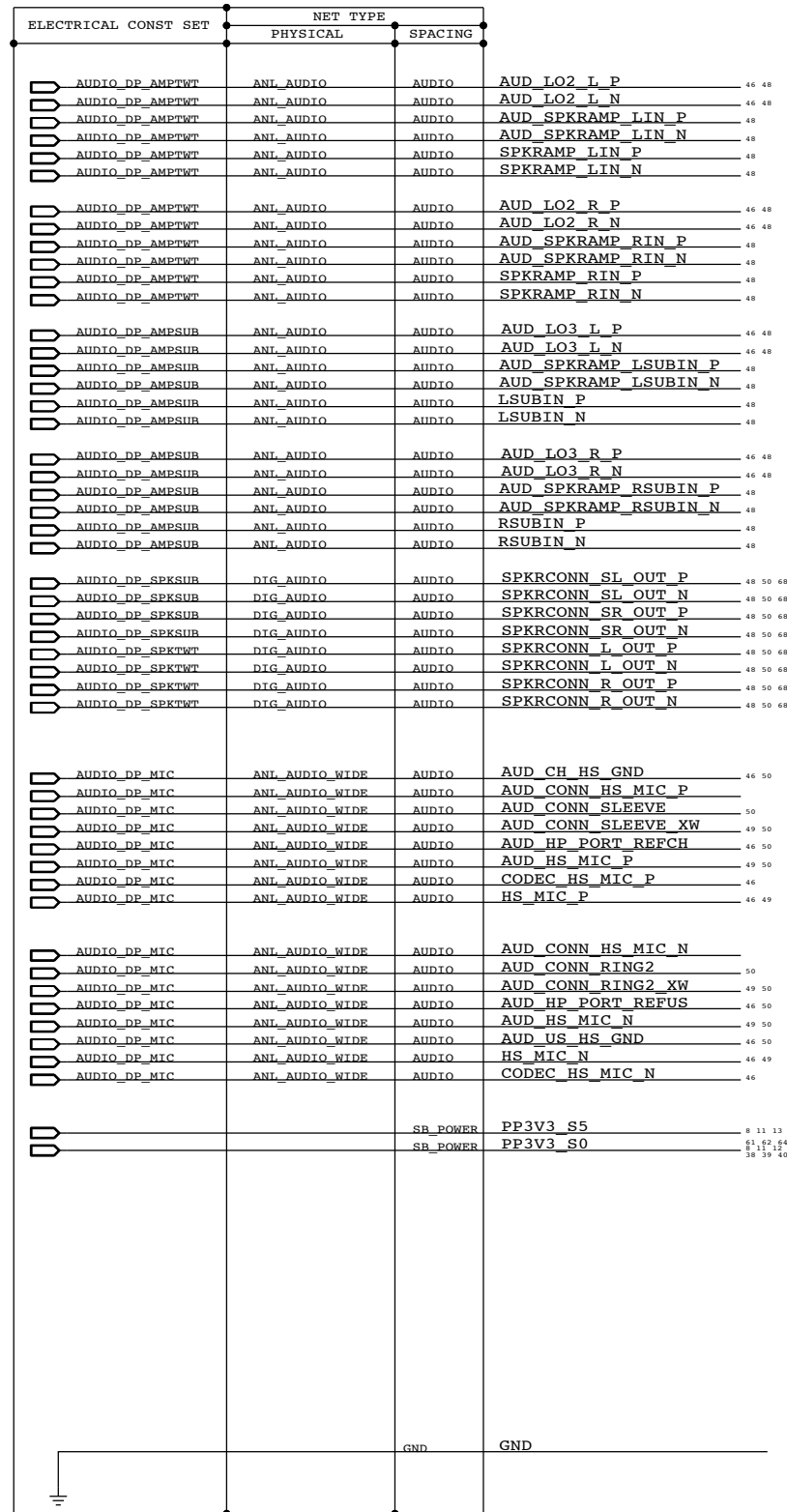
NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_85D	BGA	P65_BGA
PCIE_85D	BGA	P65_BGA
CLK_PCIE_85D	BGA	P65_BGA
HDMI_85D	BGA	P65_BGA


NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SENSE_45S	*	SENSE_45S
THERM_45S	*	THERM_45S
DIG_AUDIO	*	DIG_AUDIO
ANL_AUDIO	*	ANL_AUDIO
1TO1_DIFFPAIR	*	1TO1_DIFFPAIR

J44 Specific Net Properties



J44 Specific Net Properties



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Other Info:


Page Allocations - <rdar://problem/11791318> 2012 Schematic Page Allocations

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